

NTHS5402T1

Power MOSFET N-Channel ChipFET™

4.9 Amps, 30 Volts

Features

- Low $R_{DS(on)}$ for Higher Efficiency
- Miniature ChipFET Surface Mount Package

Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards



ON Semiconductor™

<http://onsemi.com>

4.9 AMPS

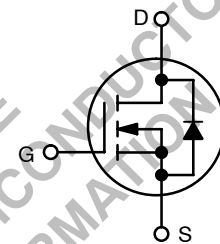
30 VOLTS

$R_{DS(on)} = 35 \text{ m}\Omega$

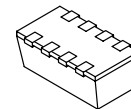
MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	5 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	± 20		V
Continuous Drain Current ($T_J = 150^\circ\text{C}$) (Note 1.) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	I_D	± 6.7	± 4.9	A
		± 4.8	± 3.5	
Pulsed Drain Current	I_{DM}	± 20		A
Continuous Source Current (Diode Conduction) (Note 1.)	I_S	2.1	1.1	A
Maximum Power Dissipation (Note 1.) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	P_D	2.5	1.3	W
		1.3	0.7	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150		$^\circ\text{C}$

1. Surface Mounted on 1" x 1" FR4 Board.

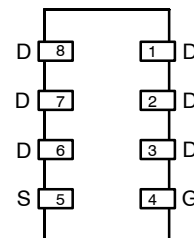


N-Channel MOSFET

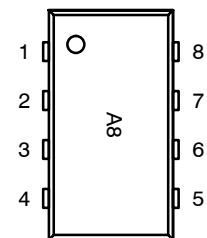


ChipFET
CASE 1206A
STYLE 1

PIN CONNECTIONS



MARKING DIAGRAM



A8 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NTHS5402T1	ChipFET	3000/Tape & Reel

NTHS5402T1

THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 2.) $t \leq 5$ sec Steady State	R_{thJA}	40 80	50 95	$^{\circ}\text{C}/\text{W}$
Maximum Junction-to-Foot (Drain) Steady State	R_{thJF}	15	20	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
----------------	--------	----------------	-----	-----	-----	------

Static

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.0	-	-	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1.0	μA
		$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^{\circ}\text{C}$	-	-	5.0	
On-State Drain Current (Note 3.)	$I_{D(on)}$	$V_{DS} \geq 5.0 \text{ V}, V_{GS} = 10 \text{ V}$	20	-	-	A
Drain-Source On-State Resistance (Note 3.)	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 4.9 \text{ A}$	-	0.030	0.035	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 3.9 \text{ A}$	-	0.045	0.055	
Forward Transconductance (Note 3.)	g_{fs}	$V_{DS} = 10 \text{ V}, I_D = 4.9 \text{ A}$	-	15	-	S
Diode Forward Voltage (Note 3.)	V_{SD}	$I_S = 1.1 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.8	1.2	V

Dynamic (Note 4.)

Total Gate Charge	Q_g	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4.9 \text{ A}$	-	13	20	nC
Gate-Source Charge	Q_{gs}		-	1.3	-	
Gate-Drain Charge	Q_{gd}		-	3.1	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15 \text{ V}, R_L = 15 \Omega, I_D = 1.0 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 6 \Omega$	-	10	15	ns
Rise Time	t_r		-	10	15	
Turn-Off Delay Time	$t_{d(off)}$		-	25	40	
Fall Time	t_f		-	10	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.1 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	-	30	60	

2. Surface Mounted on 1" x 1" FR4 Board.

3. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Guaranteed by design, not subject to production testing.

NTHS5402T1

TYPICAL CHARACTERISTICS

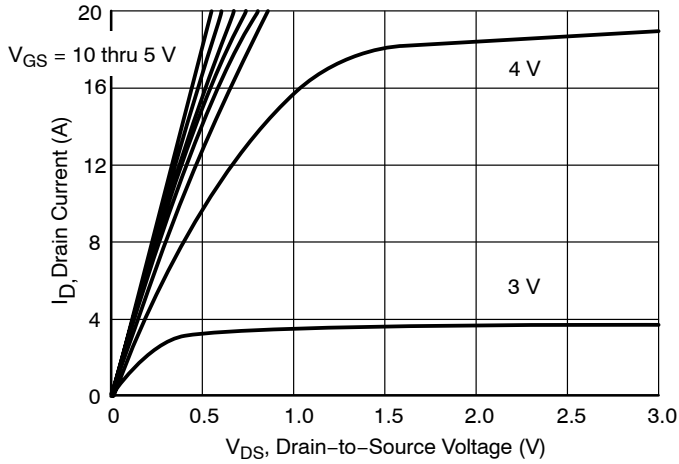


Figure 1. Output Characteristics

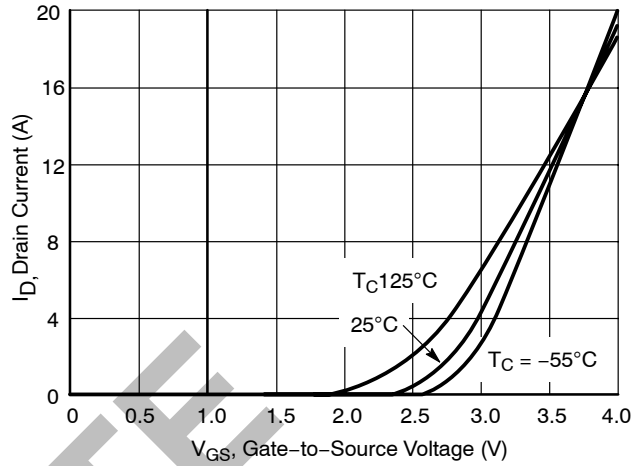


Figure 2. Transfer Characteristics

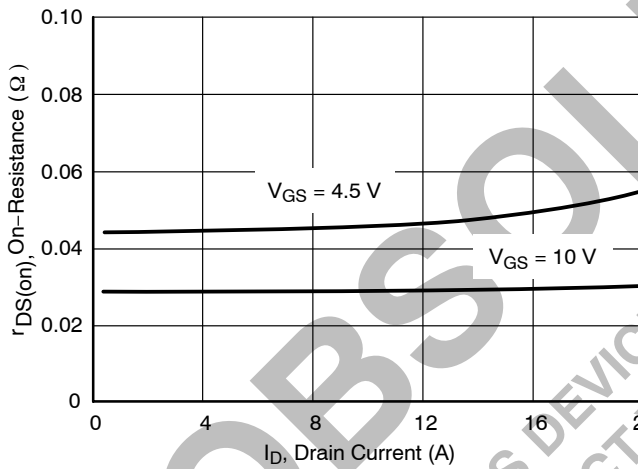


Figure 3. On-Resistance vs. Drain Current

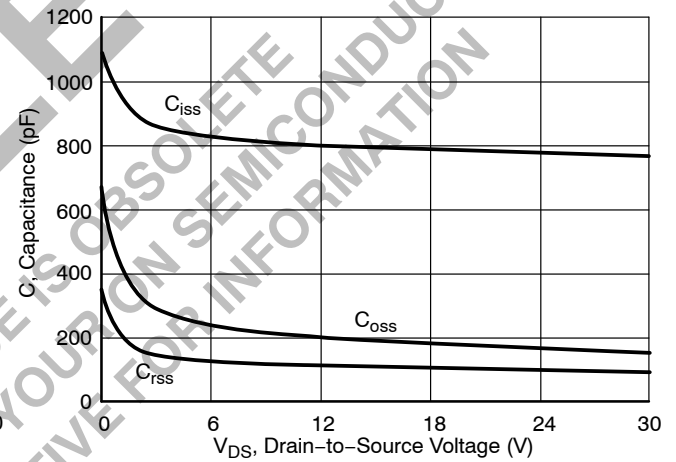


Figure 4. Capacitance

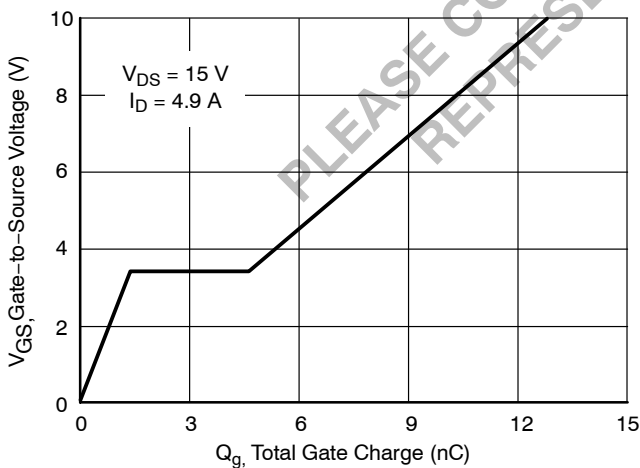


Figure 5. Gate Charge

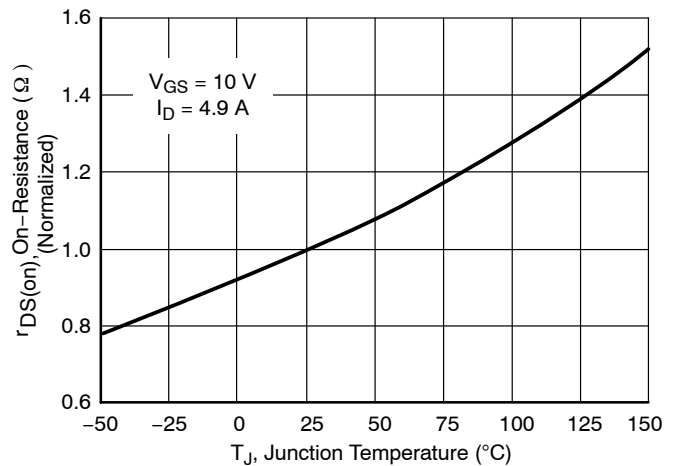


Figure 6. On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

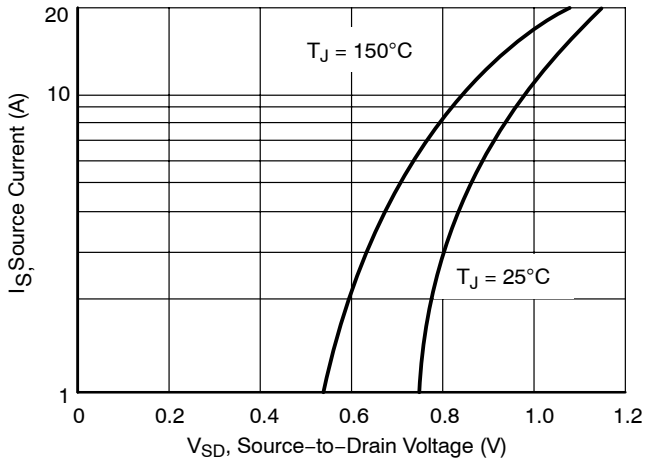


Figure 7. Source-Drain Diode Forward Voltage

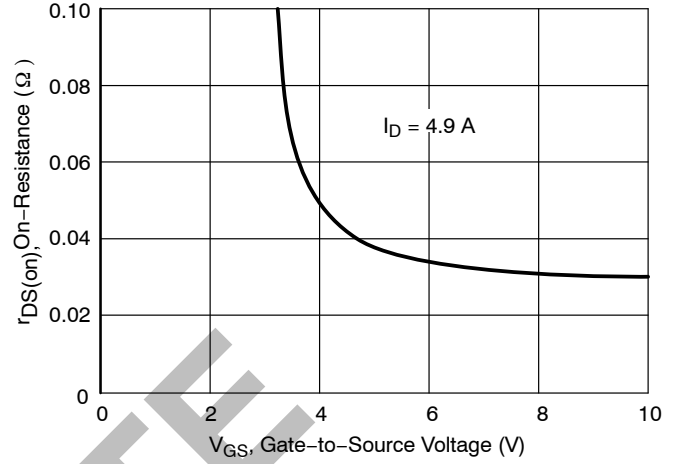


Figure 8. On-Resistance vs. Gate-to-Source Voltage

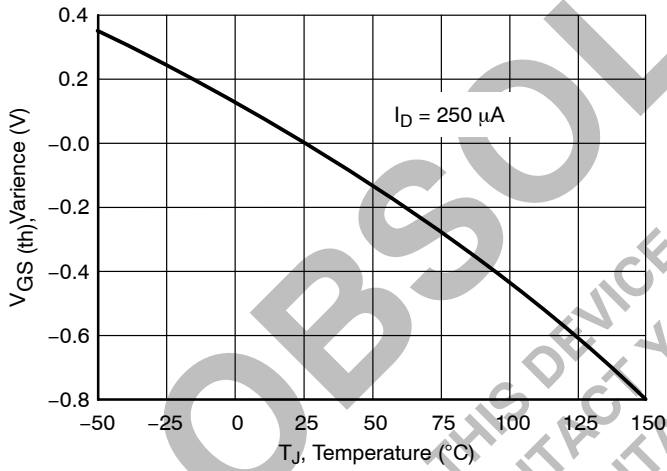


Figure 9. Threshold Voltage

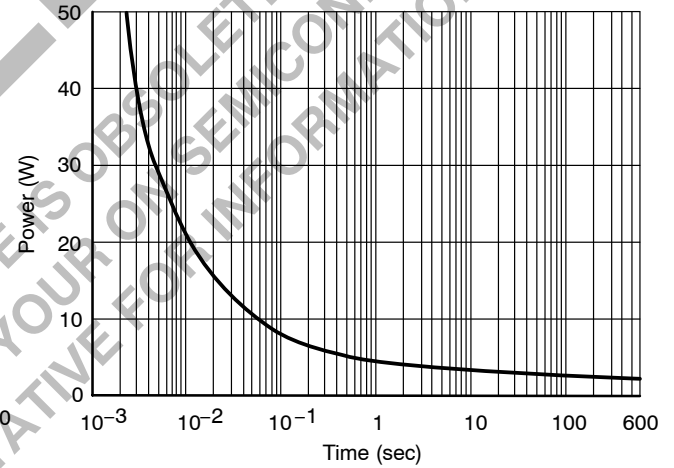


Figure 10. Single Pulse Power

TYPICAL CHARACTERISTICS

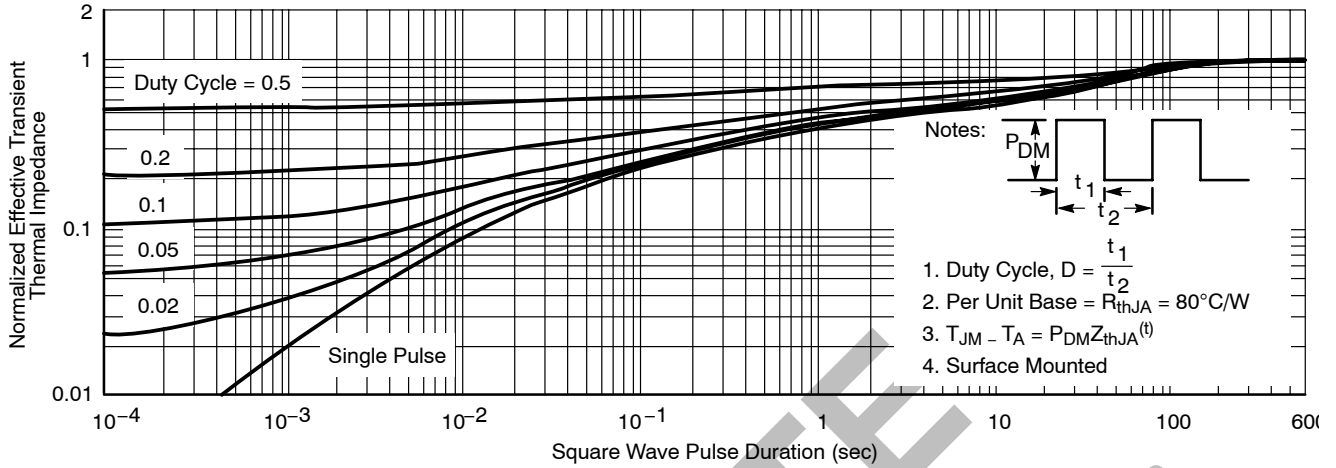


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

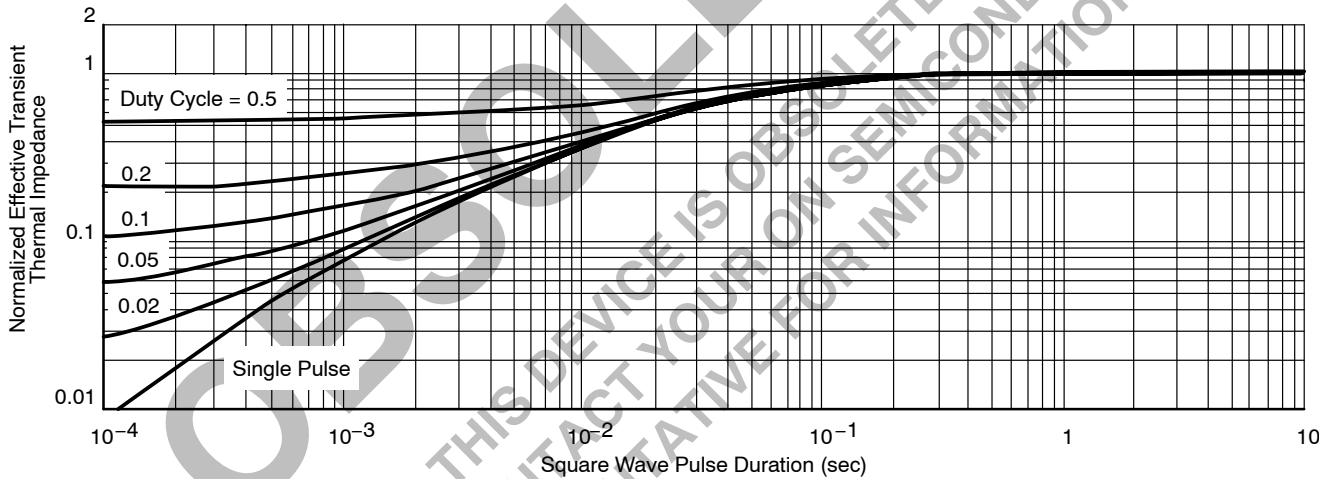


Figure 12. Normalized Thermal Transient Impedance, Junction-to-Foot

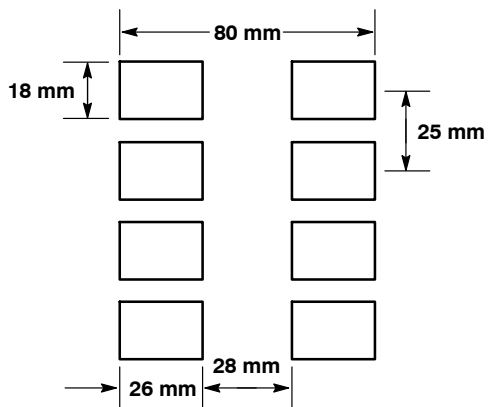


Figure 13.

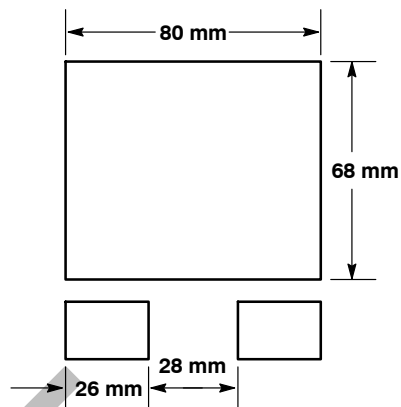


Figure 14.

BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 13. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 14 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the

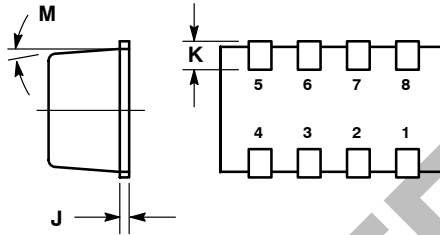
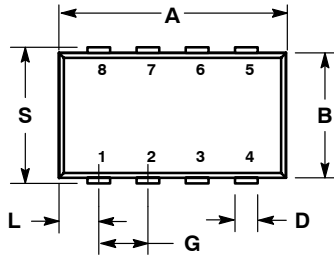
confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

OBSOLETE
THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMI SALES
REPRESENTATIVE FOR INFORMATION

NTHS5402T1

PACKAGE DIMENSIONS

ChipFET
CASE 1206A-03
ISSUE C



0.05 (0.002)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5° NOM		5° NOM	
S	1.80	2.00	0.072	0.080

STYLE 1:


1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

OBSOLETE

THIS DEVICE IS OBSOLETE
PLEASE CONTACT YOUR ON SEMICONDUCTOR
REPRESENTATIVE FOR INFORMATION

OBSOLETE
 THIS DEVICE IS OBSOLETE
 PLEASE CONTACT YOUR ON SEMICONDUCTOR
 REPRESENTATIVE FOR INFORMATION

ChipFET is a trademark of Vishay Siliconix

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
 P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
 4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.