19-1404; Rev 1; 4/99

MAXIM

Serially Controlled, Clickless Audio/Video Switches

General Description

The MAX4571–MAX4574 serial-interface controlled switches are ideal for multimedia applications. Each device features 35Ω max on-resistance, -90dB audio off-isolation at 20kHz, -60dB video off-isolation at 1.0MHz, and "clickless" mode operation for audio applications.

The MAX4571/MAX4573 contain eleven SPST switches, while the MAX4572/MAX4574 contain two SPST switches and six SPDT switches. The MAX4571/MAX4572 feature a 2-wire, I²C™-compatible serial interface. The MAX4573/MAX4574 feature a 3-wire, SPI™/QSPI™/MICROWIRE™-compatible serial interface. All four parts are available in 28-pin QSOP, SSOP, and wide SO packages and operate over the commercial and extended temperature ranges.

Applications

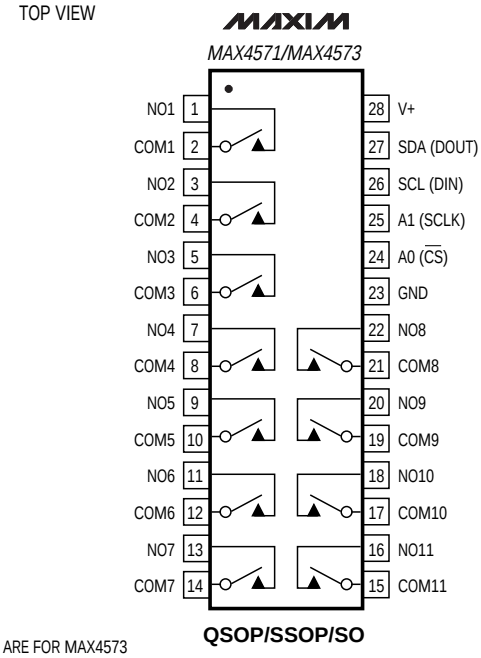
Set-Top Boxes

PC Multimedia Boards

Audio Systems

Video Conferencing Systems

Pin Configurations



Pin Configurations continued at end of data sheet.

Features

- ♦ **Selectable Soft Switching Mode for "Clickless" Audio Operation**
- ♦ **35Ω max On-Resistance**
- ♦ **-90dB Audio Off-Isolation at 20kHz**
  -50dB Video Off-Isolation at 10MHz
- ♦ **-90dB Audio Crosstalk at 20kHz**
  -52dB Video Crosstalk at 10MHz
- ♦ **Serial Interface**
  2-Wire, Fast-Mode, I²C-Compatible (MAX4571/72)
  3-Wire, SPI/QSPI/MICROWIRE-Compatible (MAX4573/74)
- ♦ **Single-Supply Operation from +2.7V to +5.25V**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4571CEI	0°C to +70°C	28 QSOP
MAX4571CAI	0°C to +70°C	28 SSOP
MAX4571CWI	0°C to +70°C	28 Wide SO
MAX4571EEI	-40°C to +85°C	28 QSOP
MAX4571EAI	-40°C to +85°C	28 SSOP
MAX4571EWI	-40°C to +85°C	28 Wide SO
MAX4572CEI	0°C to +70°C	28 QSOP
MAX4572CAI	0°C to +70°C	28 SSOP
MAX4572CWI	0°C to +70°C	28 Wide SO
MAX4572EEI	-40°C to +85°C	28 QSOP
MAX4572EAI	-40°C to +85°C	28 SSOP
MAX4572EWI	-40°C to +85°C	28 Wide SO
MAX4573CEI	0°C to +70°C	28 QSOP
MAX4573CAI	0°C to +70°C	28 SSOP
MAX4573CWI	0°C to +70°C	28 Wide SO
MAX4573EEI	-40°C to +85°C	28 QSOP
MAX4573EAI	-40°C to +85°C	28 SSOP
MAX4573EWI	-40°C to +85°C	28 Wide SO
MAX4574CEI	0°C to +70°C	28 QSOP
MAX4574CAI	0°C to +70°C	28 SSOP
MAX4574CWI	0°C to +70°C	28 Wide SO
MAX4574EEI	-40°C to +85°C	28 QSOP
MAX4574EAI	-40°C to +85°C	28 SSOP
MAX4574EWI	-40°C to +85°C	28 Wide SO

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SPI/QSPI are trademarks of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

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Serially Controlled, Clickless Audio/Video Switches

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to +6V
NO_ _, COM_, DOUT to GND (Note 1) .....-0.3V to (V+ + 0.3V)
SCL, SDA, $\overline{CS}$, SCLK, DIN, A0, A1 to GND.....-0.3V to +6V
Continuous Current into Any Terminal.....±10mA
Peak Current (pulsed at 1ms, 10% duty cycle).....±50mA
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 10.8mW/°C above +70°C).....860mW
SSOP (derate 9.5mW/°C above +70°C) 762mW
Wide SO (derate 12.5mW/°C above +70°C).....1000mW
Operating Temperature Ranges
MAX457_C_ _ .....0°C to +70°C
MAX457_E_ _.....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NO_ _ or COM_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCHES							
Analog Signal Range (Note 3)	$V_{NO__}$, $V_{COM_}$			0		V+	V
On-Resistance	R_{ON}	$I_{COM_}$ = 4mA, $V_{NO__}$ = 3V, V+ = 4.75V	T_A = +25°C		25	35	Ω
			T_A = T_{MIN} to T_{MAX}			45	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$I_{COM_}$ = 4mA, $V_{NO__}$ = 3V, V+ = 4.75V	T_A = +25°C		0.8	3	Ω
			T_A = T_{MIN} to T_{MAX}			3	
On-Resistance Flatness (Note 5)	R_{FLAT}	$I_{COM_}$ = 4mA; V+ = 4.75V; $V_{NO__}$ = 1V, 2V, 3V	T_A = +25°C		2	6	Ω
			T_A = T_{MIN} to T_{MAX}			6	
NO_ _ Off-Leakage Current (Note 6)	$I_{NO__ (OFF)}$	$V_{NO__}$ = 4.5V, 1V; $V_{COM_}$ = 1V, 4.5V; V+ = 5.25V	T_A = +25°C	-0.2	0.01	0.2	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM_ Off-Leakage Current (Note 6)	$I_{COM_ (OFF)}$	$V_{NO__}$ = 4.5V, 1V; $V_{COM_}$ = 1V, 4.5V; V+ = 5.25V	T_A = +25°C	-0.2	0.01	0.2	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
COM _ On-Leakage Current (Note 6)	$I_{COM_ (ON)}$	$V_{COM_}$ = 4.5V, 1V; $V_{NO__}$ = 4.5V, 1V, or floating; V+ = 5.25V	T_A = +25°C	-0.2	0.01	0.2	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	
AUDIO PERFORMANCE							
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 1kHz, R_L = 600Ω, $V_{NO__}$ = $1V_{RMS}$, $V_{NO__}$ = 2.5V			0.07		%
Off-Isolation (Note 7)	$V_{ISO(A)}$	$V_{NO__}$ = $1V_{RMS}$, f_{IN} = 20kHz, R_L = 600Ω, Figure 1			-90		dB
Channel-to-Channel Crosstalk	$V_{CT(A)}$	$V_{NO__}$ = $1V_{RMS}$, f_{IN} = 20kHz, R_S = 600Ω, Figure 1			-90		dB

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = 5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VIDEO PERFORMANCE							
Off-Isolation (Note 7)	$V_{ISO(V)}$	$V_{NO__}$ = 1V_{RMS}, f_{IN} = 1.0MHz, R_L = 50Ω, Figure 1			-50		dB
Channel-to-Channel Crosstalk	$V_{CT(V)}$	$V_{NO__}$ = 1V_{RMS}, f_{IN} = 1.0MHz, R_S = 50Ω, Figure 1			-52		dB
-3dB Bandwidth	BW	R_{SOURCE} = 50Ω, R_L = 50Ω			>150		MHz
Off-Capacitance	$C_{OFF(NO)}$	f_{IN} = 1MHz			9		pF
DYNAMIC TIMING WITH CLICKLESS MODE DISABLED (Notes 8 and 12, Figure 2)							
Turn-On Time	t_{ONSD}	$V_{NO__}$ = 1.5V, R_L = 5kΩ, C_L = 35pF	T_A = +25°C		200	500	ns
			T_A = T_{MIN} to T_{MAX}			700	
Turn-Off Time	t_{OFFSD}	$V_{NO__}$ = 1.5V, R_L = 300Ω, C_L = 35pF	T_A = +25°C		75	300	ns
			T_A = T_{MIN} to T_{MAX}			400	
Break-Before-Make Time	t_{BBM}	MAX4572/MAX4574, $V_{NO__}$ = 1.5V, T_A = T_{MIN} to T_{MAX}		10	125		ns
DYNAMIC TIMING WITH CLICKLESS MODE ENABLED (Note 8, Figure 2)							
Turn-On Time	t_{ONSE}	$V_{NO__}$ = 1.5V, R_L = 5kΩ, C_L = 35pF, T_A = +25°C			8		ms
Turn-Off Time	t_{OFFSE}	$V_{NO__}$ or = 1.5V, R_L = 300Ω, C_L = 35pF, T_A = +25°C			3		ms
POWER SUPPLY							
Supply Voltage Range	V+	T_A = T_{MIN} to T_{MAX}		+2.7		+5.25	V
Supply Current (Note 9)	I+	All logic inputs = 0 or V+, T_A = T_{MIN} to T_{MAX}			6	10	µA

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = 3V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG SWITCHES							
Analog Signal Range (Note 3)	$V_{NO__}$, $V_{COM_}$			0		V+	V
On-Resistance	R_{ON}	$I_{COM_}$ = 4mA, $V_{NO__}$ =2V, V+ = 2.7V	T_A = +25°C		43	90	Ω
			T_A = T_{MIN} to T_{MAX}			110	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	$I_{COM_}$ = 4mA, $V_{NO__}$ = 2V, V+ = 2.7V	T_A = +25°C		1	5	Ω
			T_A = T_{MIN} to T_{MAX}			5	

ELECTRICAL CHARACTERISTICS—Single +3V Supply (continued)

(V+ = +3V ±10%, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Resistance Flatness (Note 5)	R_{FLAT}	$I_{COM_}$ = 4mA; V+ = 2.7V; $V_{NO__}$ = 1V, 5V, 2V	T_A = +25°C		4	10	Ω
			$T_A = T_{MIN}$ to T_{MAX}			10	
NO_ _Off-Leakage Current (Notes 6 and 10)	$I_{NO__(OFF)}$	$V_{NO__}$ = 3V, 0.5V; $V_{COM_}$ = 0.5V, 3V; V+ = 3.6V	T_A = +25°C	-0.2	0.01	0.2	nA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
COM_ Off-Leakage Current (Notes 6 and 10)	$I_{COM_(OFF)}$	$V_{NO__}$ = 3V, 0.5V; $V_{COM_}$ = 0.5V, 3V; V+ = 3.6V	T_A = +25°C	-0.2	0.01	0.2	nA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
COM _ On-Leakage Current (Notes 6 and 10)	$I_{COM_(ON)}$	$V_{COM_}$ = 3V, 0.5V; $V_{NO__}$ = 3V, 0.5V, or floating; V+ = 3.6V	T_A = +25°C	-0.2	0.01	0.2	nA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
AUDIO PERFORMANCE							
Total Harmonic Distortion plus Noise	THD+N	f_{IN} = 1kHz, R_L = 600Ω, $V_{NO_}$ = 0.5V_{RMS}, $V_{NO__}$ = 1.5V			0.07		%
Off-Isolation (Note 7)	$V_{ISO(A)}$	$V_{NO__}$ = 0.5V_{RMS}, f_{IN} = 20kHz, R_L = 600Ω, Figure 1			-90		dB
Channel-to-Channel Crosstalk	$V_{CT(A)}$	$V_{NO__}$ = 0.5V_{RMS}, f_{IN} = 20kHz, R_S = 600Ω, Figure 1			-90		dB
VIDEO PERFORMANCE							
Off-Isolation (Note 7)	$V_{ISO(V)}$	$V_{NO__}$ = 0.5V_{RMS}, f_{IN} = 10MHz, R_L = 50Ω, Figure 1			-50		dB
Channel-to-Channel Crosstalk	$V_{CT(V)}$	$V_{NO__}$ = 0.5V_{RMS}, f_{IN} = 10MHz, R_S = 50Ω, Figure 1			-52		dB
-3dB Bandwidth	BW	R_{SOURCE} = 50Ω, R_L = 50Ω, C_L = 35pF			>150		MHz
Off Capacitance	$C_{OFF(NO)}$	f_{IN} = 1MHz			9		pF
DYNAMIC TIMING WITH CLICKLESS MODE DISABLED (Notes 8 and 12, Figure 2)							
Turn-On Time	t_{ONSD}	$V_{NO__}$ = 1.5V, R_L = 5kΩ, C_L = 35pF	T_A = +25°C		300	900	ns
			$T_A = T_{MIN}$ to T_{MAX}			1000	
Turn-Off Time	t_{OFFSD}	$V_{NO__}$ = 1.5V, R_L = 300Ω, C_L = 35pF	T_A = +25°C		100	300	ns
			$T_A = T_{MIN}$ to T_{MAX}			400	
Break-Before-Make Time	t_{BBM}	$V_{NO__}$ = 1.5V, $T_A = T_{MIN}$ to T_{MAX}		10	200		ns
DYNAMIC TIMING WITH CLICKLESS MODE ENABLED (Notes 8 and 12, Figure 2)							
Turn-On Time	t_{ONSE}	$V_{NO__}$ = 1.5V, R_L = 5kΩ, C_L = 35pF, T_A = +25°C			8		ms
Turn-Off Time	t_{OFFSE}	$V_{NO__}$ = 1.5V, R_L = 300Ω, C_L = 35pF, T_A = +25°C			3		ms

I/O INTERFACE CHARACTERISTICS

(V+ = +2.7V to +5.25V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, SCL, SDA, A0, A1)						
Input Low Voltage	V_{IL}	V+ = 5V			0.8	V
		V+ = 3V			0.6	
Input High Voltage	V_{IH}	V+ = 5V	3			V
		V+ = 3V	2			
Input Hysteresis	V_{HYST}			0.2		V
Input Leakage Current	I_{LEAK}	Digital inputs = 0 or V+	-1	0.01	1	µA
Input Capacitance	C_{IN}			5		pF
DIGITAL OUTPUTS (DOUT, SDA)						
Output Low Voltage	V_{OL}	I_{SINK} = 6mA			0.4	V
DOUT Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V+ - 0.5			V
2-WIRE INTERFACE TIMING (Figure 3)						
SCL Clock Frequency	f_{SCL}		DC		400	kHz
Bus Free Time between Stop and Start Condition	t_{BUF}		1.3			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
SCL/SDA Rise Time	t_R	(Note 11)	$20 + 0.1C_b$		300	ns
SCL/SDA Fall Time	t_F	(Note 11)	$20 + 0.1C_b$		300	ns
3-WIRE TIMING (Figure 5)						
Operating Frequency	f_{OP}		DC		2.1	MHz
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 50pF	20		200	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Pulse Width High	t_{CH}		200			ns
Rise Time (SCLK, DIN, $\overline{CS}$)	t_R				2	µs
Fall Time (SCLK, DIN, $\overline{CS}$)	t_F				2	µs

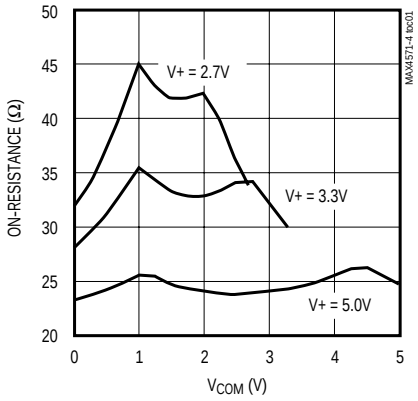
Serially Controlled, Clickless Audio/Video Switches

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design. Not subject to production testing.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and minimum on-resistance values, as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum rated temperature, and guaranteed by correlation at T_A = +25°C.
Note 7: Off-isolation = 20 log [$V_{COM_}$ / $V_{NO__}$], $V_{COM_}$ = output, $V_{NO__}$ = input to off switch.
Note 8: All timing is measured from the rising clock edge of the ACK bit for 2-wire, and from the rising edge of $\overline{CS}$ for 3-wire. Turn-off time is defined at the output of the switch for a 0.5V change, tested with a 300Ω load to ground. Turn-on time is measured with a 5kΩ load resistor to GND. All timing is shown with respect to 20% V+ and 70% V+, unless otherwise noted.
Note 9: Supply current can be as high as 2mA per switch during switch transitions in the clickless mode, corresponding to a 28mA total supply transient current requirement.
Note 10: Leakage testing for single-supply operation is guaranteed by testing with a single +5.25V supply.
Note 11: C_b = capacitance of one bus line in pF. Tested with C_b = 400pF.
Note 12: Typical values are for MAX4573/MAX4574 devices.

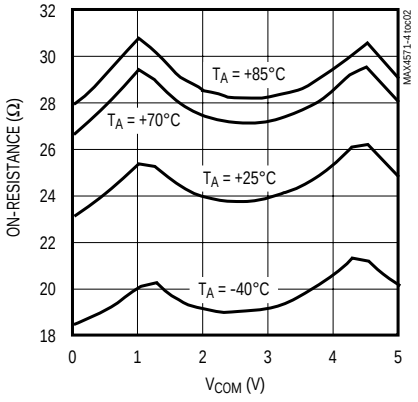
Typical Operating Characteristics

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

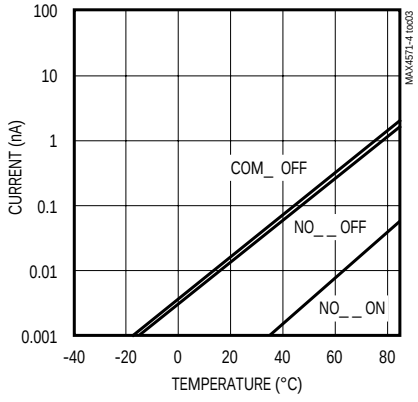
ON-RESISTANCE vs. V_{COM}



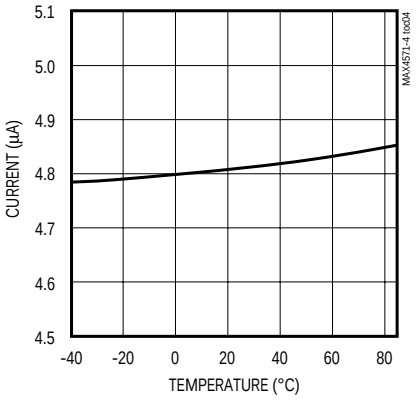
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE



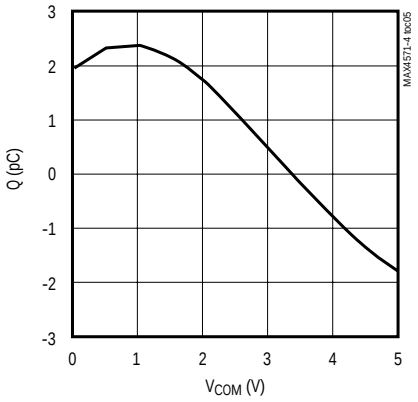
LEAKAGE CURRENT vs. TEMPERATURE



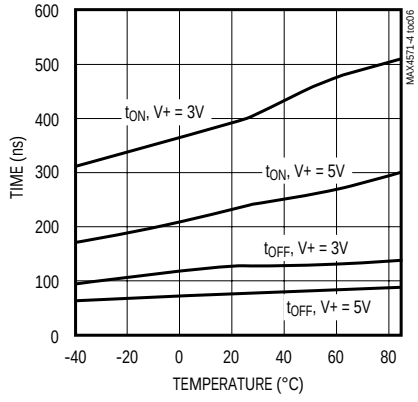
SUPPLY CURRENT vs. TEMPERATURE



CHARGE INJECTION vs. V_{COM}



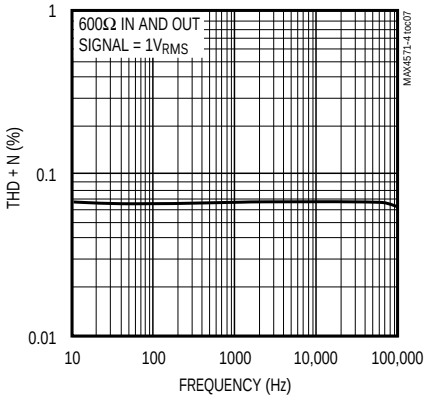
ON/OFF TIME vs. TEMPERATURE (HARD MODE)



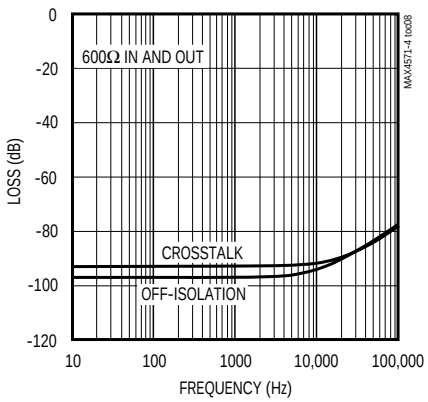
Typical Operating Characteristics (continued)

(V+ = 5V, T_A = +25°C, unless otherwise noted.)

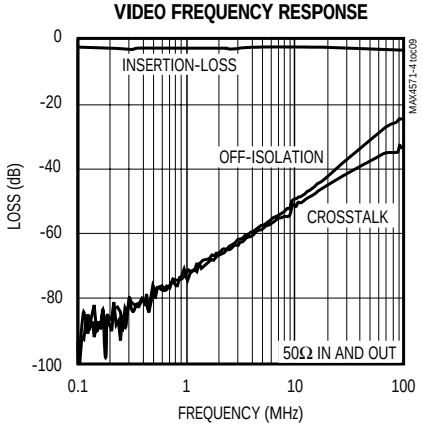
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY



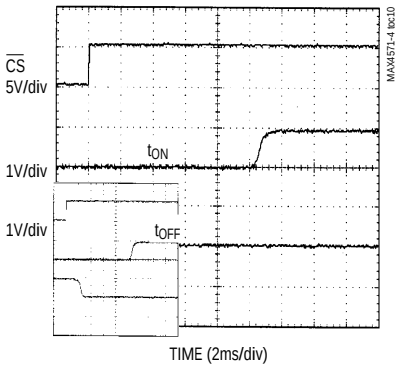
AUDIO FREQUENCY RESPONSE



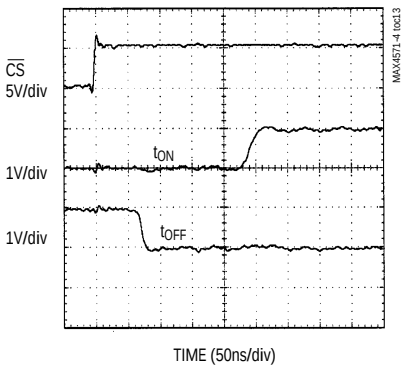
VIDEO FREQUENCY RESPONSE



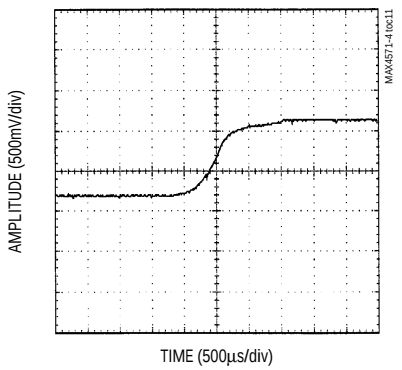
ON/OFF TIMES (SOFT MODE)



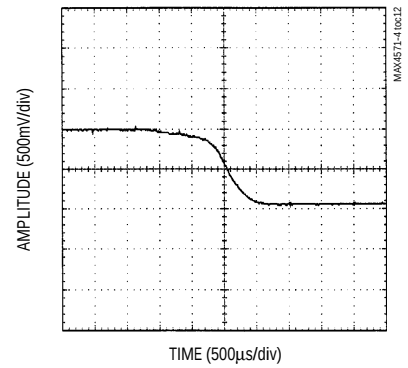
ON/OFF TIMES (HARD MODE)



SOFT MODE RISE TIME



SOFT MODE FALL TIME



Pin Descriptions

PIN		NAME		FUNCTION
MAX4571	MAX4572	MAX4571	MAX4572	
1, 3, 5, 7, 9, 11, 13, 22, 20, 18, 16	–	NO1–NO11	–	Normally Open Terminals
–	1, 4, 7, 10	–	NO1A–NO4A	Normally Open Terminals
–	3, 6, 9, 12	–	NO1B–NO4B	Normally Open Terminals
–	13, 16	–	NO5, NO8	Normally Open Terminals
–	22, 19, 20, 17	–	NO6A, NO7A, NO6B, NO7B	Normally Open Terminals
2, 4, 6, 8, 10, 12, 14, 21, 19, 17, 15	2, 5, 8, 11, 14, 21, 18, 15	COM1–COM11	COM1–COM8	Common Terminals
23	23	GND	GND	Ground
24	24	A0	A0	LSB + 1 of 2-Wire Serial Interface Address Field
25	25	A1	A1	LSB + 2 of 2-Wire Serial Interface Address Field
26	26	SCL	SCL	Clock Input of 2-Wire Serial Interface
27	27	SDA	SDA	Data Input of 2-Wire Serial Interface
28	28	V+	V+	Positive Supply Voltage

PIN		NAME		FUNCTION
MAX4573	MAX4574	MAX4573	MAX4574	
1, 3, 5, 7, 9, 11, 13, 22, 20, 18, 16	–	NO1–NO11	–	Normally Open Terminals
–	1, 4, 7, 10	–	NO1A–NO4A	Normally Open Terminals
–	3, 6, 9, 12	–	NO1B–NO4B	Normally Open Terminals
–	13, 16	–	NO5, NO8	Normally Open Terminals
–	22, 19, 20, 17	–	NO6A, NO7A, NO6B, NO7B	Normally Open Terminals
2, 4, 6, 8, 10, 12, 14, 21, 19, 17, 15	2, 5, 8, 11, 14, 21, 18, 15	COM1–COM11	COM1–COM8	Common Terminals
23	23	GND	GND	Ground
24	24	$\overline{CS}$	$\overline{CS}$	Chip Select of 3-Wire Serial Interface
25	25	SCLK	SCLK	Clock Input of 3-Wire Serial Interface
26	26	DIN	DIN	Clock Input of 3-Wire Serial Interface
27	27	DOUT	DOUT	Data Output of 3-Wire Serial Interface
28	28	V+	V+	Positive Supply Voltage

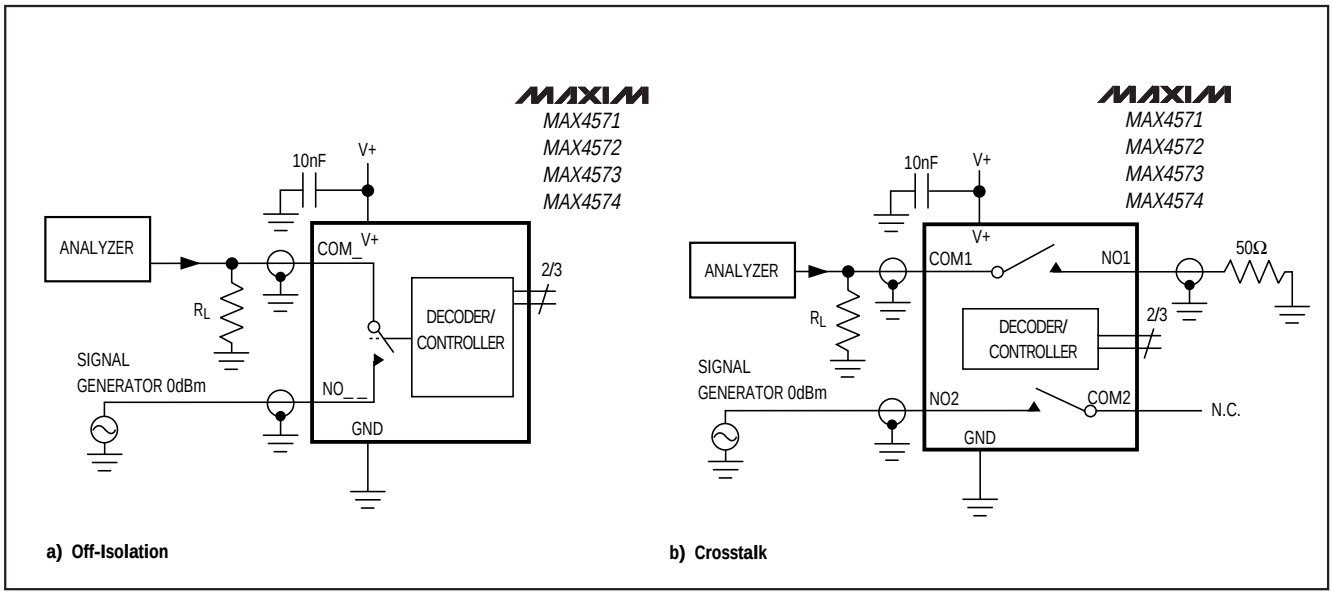


Figure 1. Off-Isolation and Crosstalk

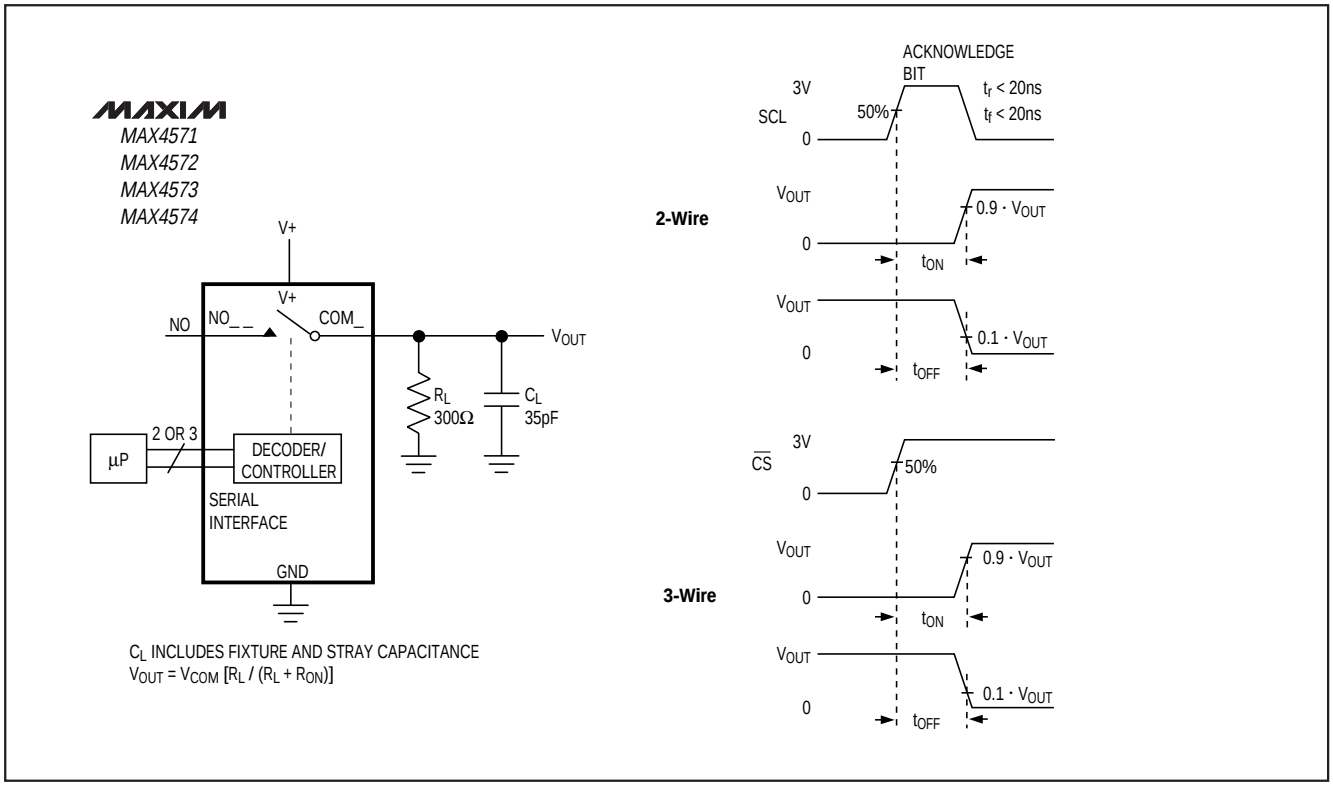


Figure 2. Switching Time

Serially Controlled, Clickless Audio/Video Switches

Detailed Description

The MAX4571–MAX4574 are serial-interface controlled switches with soft-mode "clickless" and hard-mode operating capability. The MAX4571/MAX4573 contain 11 SPST switches, while the MAX4572/MAX4574 contain two SPST switches and six SPDT switches. The SPDT switches are actually 2-to-1 multiplexers, in that each SPDT is really two independent SPST switches with a common node, as shown in the *Pin Configurations*. Each switch is controlled independently by either the SPI or I²C interface.

Audio off-isolation is -90dB at 20kHz, crosstalk is at least -90dB at 20kHz, and video off-isolation is at least -50dB at 10MHz.

Each switch of any device may be set to operate in either soft or hard mode. In soft mode, the switching transition is slowed to avoid the audible "clicking" that can occur when switches are used to route audio signals. In hard mode, the switches are not slowed down, making this mode useful when a faster response is required. If a new command is issued while any soft-mode switch is transitioning, the switch transition time is decreased so it reaches its final state before the new command is executed. Soft mode is the power-up default state for all switches. Switches in the same mode are guaranteed to be break-before-make relative to each other. Break-before-make does not apply between switches operating in different modes.

These devices operate from a single supply of +2.7V to +5.25V. The MAX4571/MAX4572 feature a 2-wire, I²C-compatible serial interface, and the MAX4573/MAX4574 feature a 3-wire, SPI/QSPI/MICROWIRE-compatible serial interface.

Applications Information

Switch Control

The MAX4571–MAX4574 have a common command and control-bit structure, the differences being only in the interface type (2-wire or 3-wire) and in the switch configurations.

The SWITCHSET command controls the open/closed states of the various switches. MODESET controls soft/hard-mode states of the switches. There are also NO_OP and RESET commands. The NO_OP command is useful for daisy-chaining multiple 3-wire parts. The RESET command places a device in a state identical to its power-up state, with all switches open and in soft switching mode.

Table 1 shows the configuration of the command bits and their related commands. Table 2 shows the configuration of the data bits and their related switches. The arrangement of the command bits and the data bits depends on the interface type (2-wire or 3-wire). After a SWITCHSET command is issued, a logic 1 in any data-bit location closes the associated switch, while a logic 0 opens it. After a MODESET command, a logic 1 in any data-bit location sets the associated switch into hard mode, while a logic 0 sets it into soft mode.

2-Wire Serial Interface

The MAX4571/MAX4572 use a 2-wire, I²C-compatible serial interface requiring only two I/O lines of a standard microprocessor port for communication. These devices use the SendByte™ and WriteWord™ protocols. The SendByte protocol is used only for the RESET command. The WriteWord protocol is used for the MODESET and SWITCHSET commands.

The first byte of any 2-wire serial-interface transaction is always the address byte. To address a given chip, the A0 and A1 bits in the address byte (Table 3) must duplicate the values present at the A0 and A1 pins of that chip, and the rest of the address bits must be configured as shown in Table 3. Connect the A0 and A1 pins to V+ or to GND, or drive them with CMOS logic levels.

The second byte is the command byte. The possible commands are RESET, MODESET, and SWITCHSET. RESET sets all switches to the initial power-up state (open and in soft switching mode). The RESET command is executed on the rising clock edge of the acknowledge bit after the command byte. The MODESET and SWITCHSET commands are each followed by two data bytes. The first data byte is buffered so all the data latches switch together. MODESET and SWITCHSET are executed on the rising clock edge of the acknowledge bit after the second data byte. Table 3 details the 2-wire interface data structure. Figures 3 and 4 and the *I/O Interface Characteristics* detail the timing of the 2-wire serial-interface protocol. All bytes of the transmission, whether address, command, or data, are sent MSB first.

The MAX4571/MAX4572 are receive-only devices and must be controlled by a bus master device. A bus master signals the beginning of a transmission with a start condition by transitioning SDA from high to low while SCL is high. The slave devices monitor the serial bus continuously, waiting for a start condition followed by an address byte. When a device recognizes its address byte, it acknowledges by pulling the SDA line low for one clock period; it is then ready to accept command and data bytes. The device then issues a similar acknowledgment after the command byte, and again after each data byte. When the master has finished

SendByte and WriteWord are trademarks of Philips Corp.

Table 1. Command Bit Mapping

MSB	MSB - 1	COMMAND	DESCRIPTION
0	0	RESET	Sets all switches open and in soft switching mode.
0	1	MODESET	Sets specified switches to soft or hard mode.
1	0	NO_OP	No Operation.
1	1	SWITCHSET	Sets specified switches open or closed.

Table 2. Data-Bit Switch Control

DATA BIT	MAX4571/MAX4573		MAX4572/MAX4574	
	SWITCH	SWITCH TERMINALS	SWITCH	SWITCH TERMINALS
D13	X	X	SW8	15, 16
D12	X	X	SW5	13, 14
D11	X	X	SW7B	17, 18
D10	SW11	15, 16	SW7A	18, 19
D9	SW10	17, 18	SW6B	20, 21
D8	SW9	19, 20	SW6A	21, 22
D7	SW8	21, 22	SW4B	11, 12
D6	SW7	13, 14	SW4A	10, 11
D5	SW6	11, 12	SW3B	8, 9
D4	SW5	9, 10	SW3A	7, 8
D3	SW4	7, 8	SW2B	5, 6
D2	SW3	5, 6	SW2A	4, 5
D1	SW2	3, 4	SW1B	2, 3
D0 (LSB)	SW1	1, 2	SW1A	1, 2

X = Don't care

communicating with the slave, it issues a stop condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

3-Wire Serial Interface

The MAX4573/MAX4574 use a 3-wire SPI/QSPI/MICROWIRE-compatible serial interface. An active-low chip-select pin, $\overline{CS}$, enables the device to receive data from the serial input pin, DIN. Command and data information are clocked in on the rising edge of the serial-clock signal (SCLK) MSB first. A total of 16 bits are needed in each write cycle. The write cycle allows two 8-bit-wide transfers if $\overline{CS}$ remains low for the entire 16 bits. The command code is contained in the two MSBs of the 16-bit word. The remaining bits control the switches as shown in Table 4. While shifting in the serial data, the device remains in its original configuration. A rising edge on $\overline{CS}$ latches the data into the MAX4573/MAX4574 internal registers, initiating the device's change of state. Table 4 shows the details of the 3-wire interface data structure.

Figures 5 and 6 and the *I/O Interface Characteristics* show the timing details of the 3-wire interface. If the two command bits initiate a SWITCHSET command, a logic 1 in a switch control location closes the associated switch, while a logic 0 opens it. If the command bits initiate a MODESET command, a logic 1 in a switch control location sets the associated switch into hard mode, while a logic 0 sets it into soft, "clickless" mode. For command-bit configurations, see Table 1.

Using Multiple Devices

There are two ways to connect multiple devices to the same 3-wire serial interface. The first involves using the DOUT pin. DOUT presents a copy of the last bit of the internal shift register, useful for daisy-chaining multiple devices. Data at DOUT are simply the input data delayed by 16 clock cycles, appearing synchronous with SCLK's falling edge. After $\overline{CS}$ goes high, DOUT holds the last bit in the shift register until new data are shifted into DIN. For a simple interface using several MAX4573/MAX4574 devices, daisy-chain the shift reg-

Table 3. 2-Wire Serial-Interface Data Format

RESET Command

	Address Byte									Command Byte (RESET)									
	MSB							LSB		MSB							LSB		
SRT	0	1	1	0	1	A1	A0	0	ACK	0	0	X	X	X	X	X	X	ACK	STP

SWITCHSET Command

	Address Byte									Command Byte (SWITCHSET)									
	MSB							LSB		MSB							LSB		
SRT	0	1	1	0	1	A1	A0	0	ACK	1	1	X	X	X	X	X	X	ACK	

MAX4571

First Data Byte									Second Data Byte										
MSB							LSB		MSB								LSB		
X	X	X	X	X	SW11	SW10	SW9	ACK	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	ACK	STP

MAX4572

First Data Byte									Second Data Byte										
MSB							LSB		MSB								LSB		
X	X	SW8	SW5	SW7B	SW7A	SW6B	SW6A	ACK	SW4B	SW4A	SW3B	SW3A	SW2B	SW2A	SW1B	SW1A	ACK	STP

MODESET Command

	Address Byte									Command Byte (MODESET)									
	MSB									MSB							LSB		
SRT	0	1	1	0	1	A1	A0	0	ACK	0	1	X	X	X	X	X	X	ACK	

MAX4571

First Data Byte									Second Data Byte										
MSB							LSB		MSB								LSB		
X	X	X	X	X	SW11	SW10	SW9	ACK	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1	ACK	STP

MAX4572

First Data Byte									Second Data Byte										
MSB							LSB		MSB								LSB		
X	X	SW8	SW5	SW7B	SW7A	SW6B	SW6A	ACK	SW4B	SW4A	SW3B	SW3A	SW2B	SW2A	SW1B	SW1A	ACK	STP

X = Don't Care
SRT = Start Condition
ACK = Acknowledge Condition
STP = Stop Condition
Logic "0" in any data bit location places the associated switch open or in soft (clickless) switching mode.
Logic "1" in any data bit location places the associated switch closed or in hard switching mode.
For command bit configuration see Table 1.

Table 4. 3-Wire Serial-Interface Data Format

MAX4573 (11 SPST)															
MSB															**LSB**
COMMAND		**SWITCH CONTROL**													
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
C1	C0	X	X	X	SW11	SW10	SW9	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1

MAX4574 (6 SPDT + 2 SPST)															
MSB															**LSB**
COMMAND		**SWITCH CONTROL**													
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
C1	C0	SW8	SW5	SW7B	SW7A	SW6B	SW6A	SW4B	SW4A	SW3B	SW3A	SW2B	SW2A	SW1B	SW1A

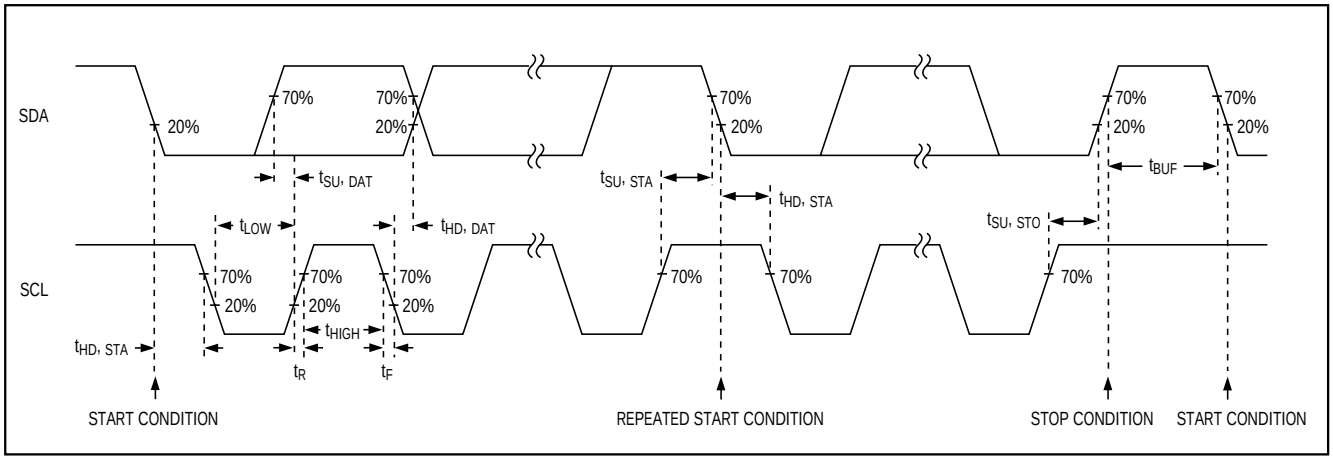


Figure 3. 2-Wire Serial-Interface Timing Diagram

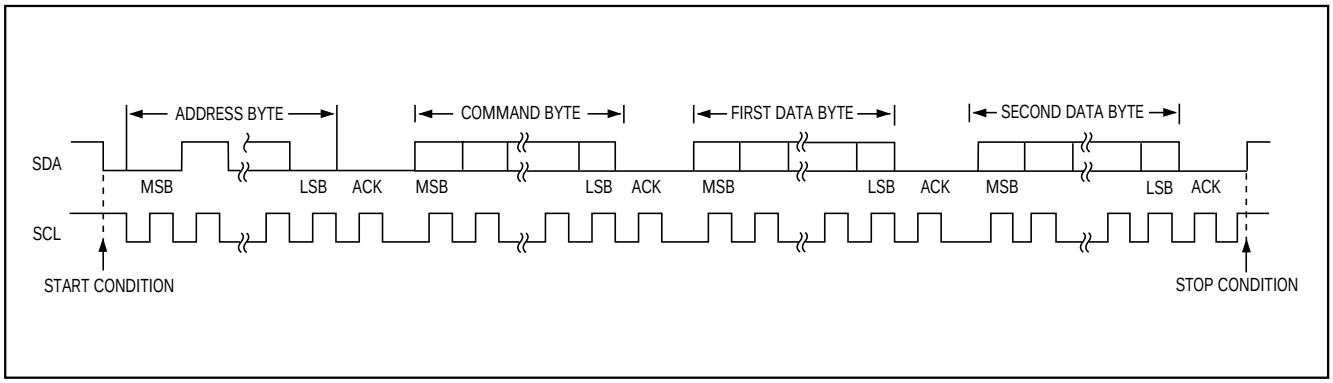


Figure 4. A Complete 2-Wire Serial-Interface Transmission

isters by connecting DOUT of the first device to DIN of the second, etc. Connect the $\overline{CS}$ pins of all devices together. Data are shifted through the MAX4573/MAX4574s in series. When $\overline{CS}$ is brought high, all devices are updated simultaneously. If any of the devices in the chain are to be left unchanged, use a NO_OP command for that device, as shown in Table 1.

An alternate way of connecting multiple devices is to decode the $\overline{CS}$ line. In this case the DOUT pin is not used and the DIN pins of all devices are connected together. Address decode logic individually controls the $\overline{CS}$ line of each device. When a device is to be selected its $\overline{CS}$ line is brought low, data are shifted in, and its $\overline{CS}$ is then brought high to execute the command.

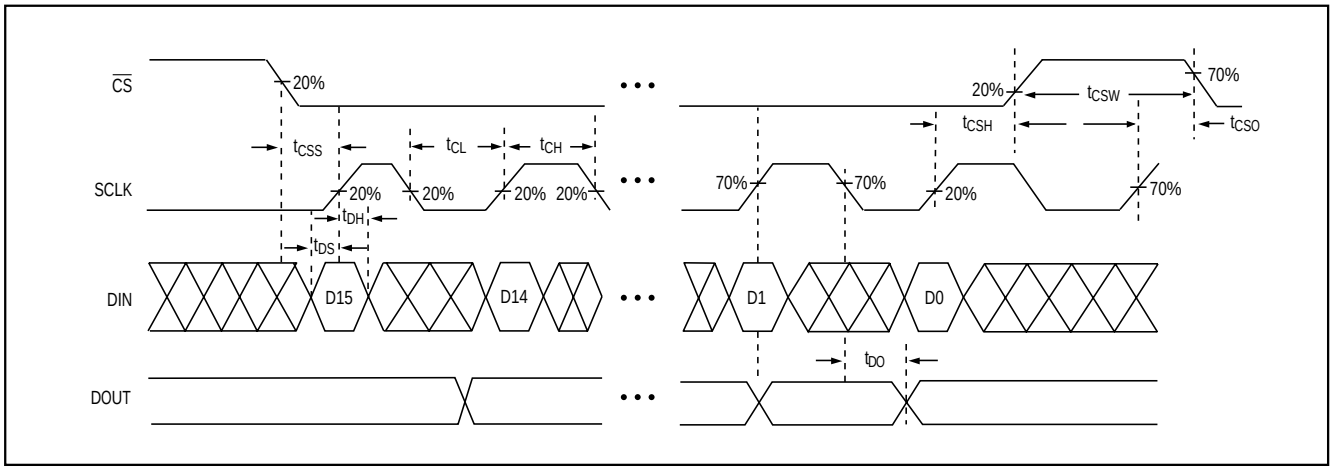


Figure 5. 3-Wire Serial-Interface Timing Diagram

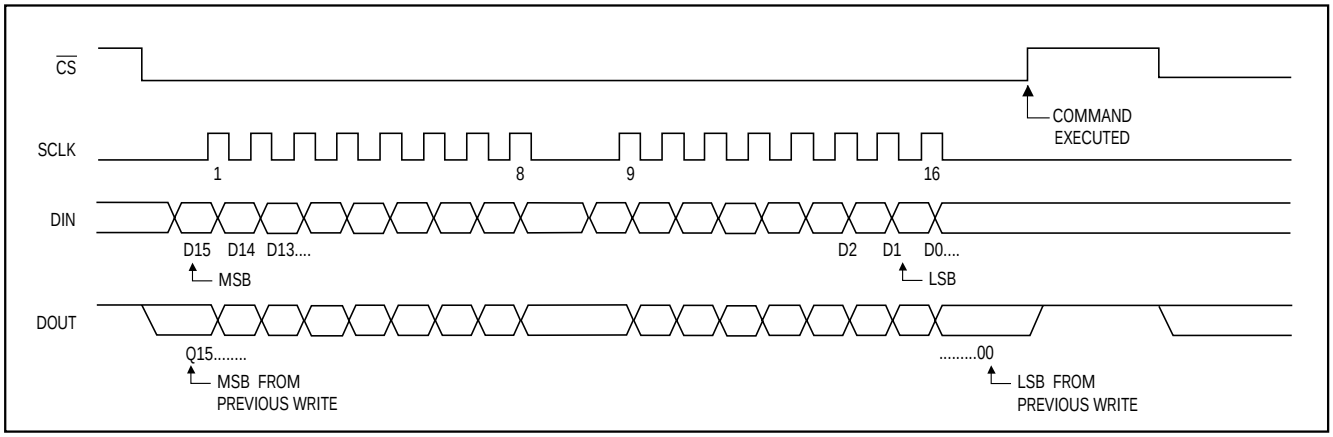
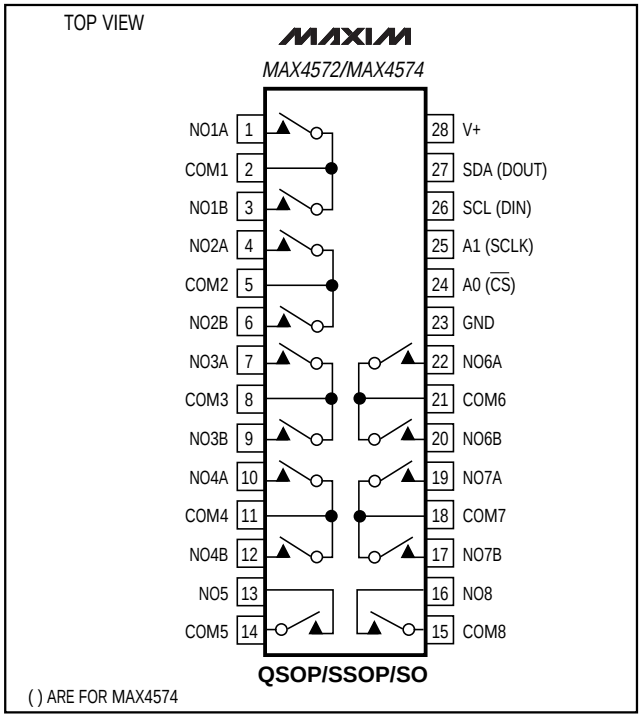


Figure 6. A Complete 3-Wire Serial-Interface Transmission

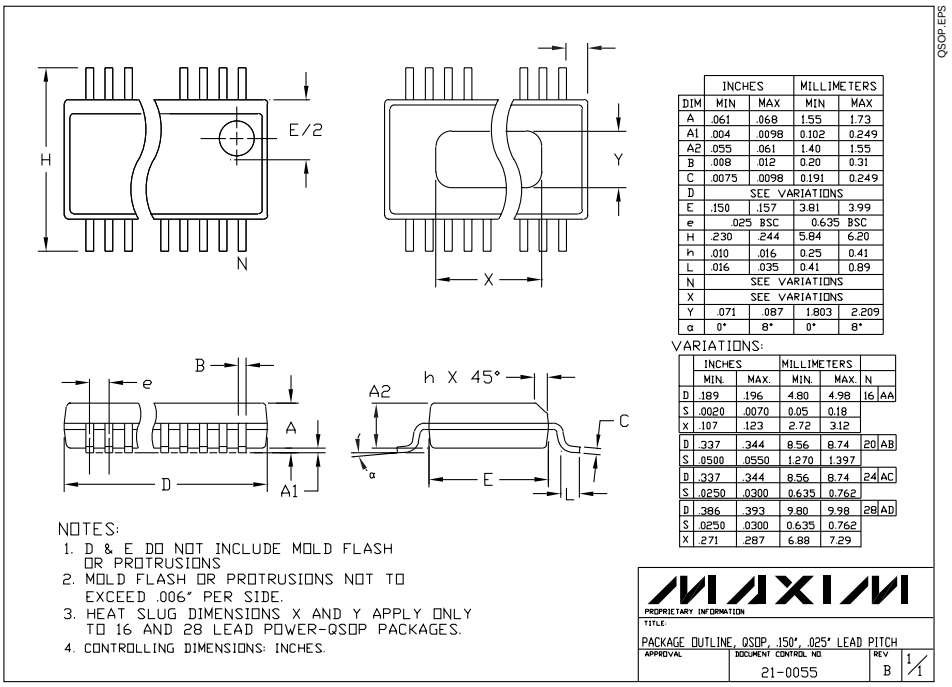
Pin Configurations (continued)



Chip Information

TRANSISTOR COUNT: 5397

Package Information



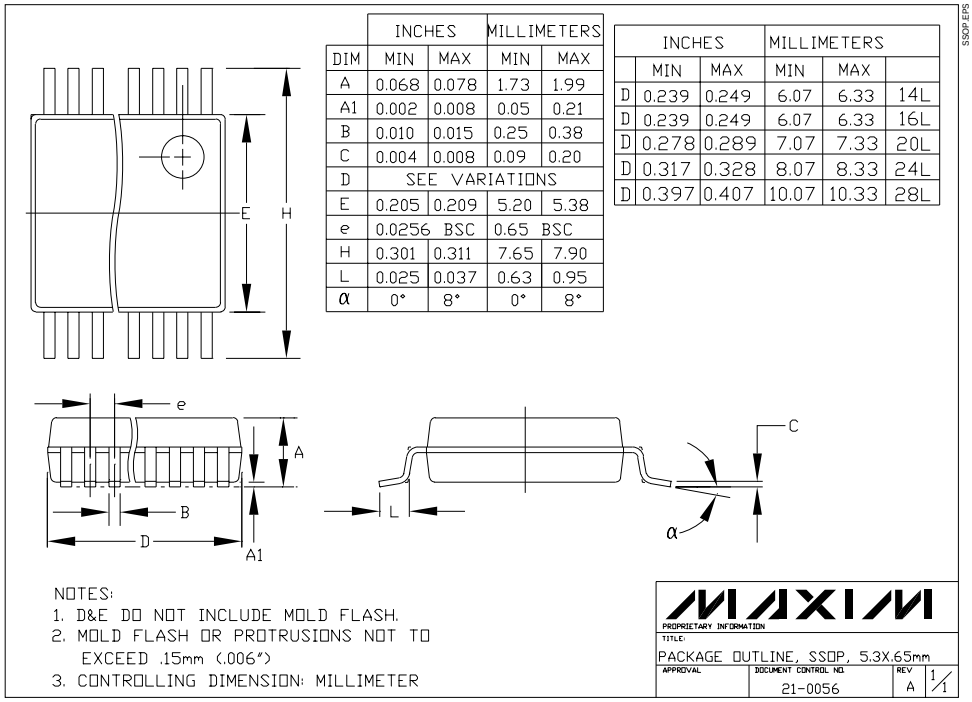
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

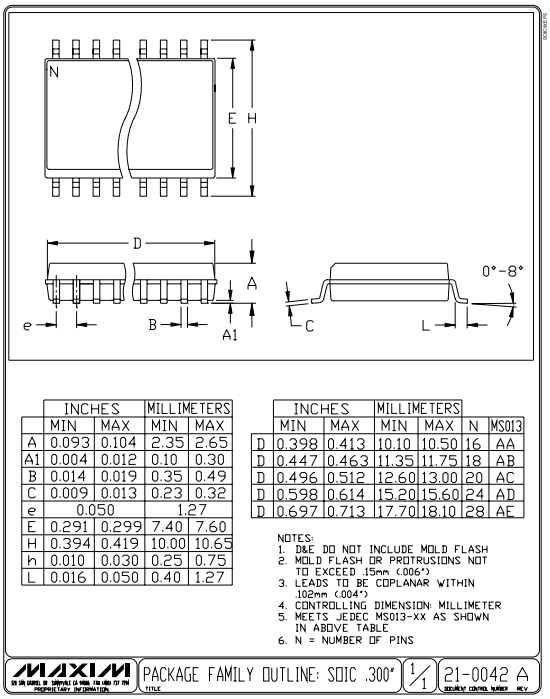
Serially Controlled, Clickless Audio/Video Switches

Package Information (continued)



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.004	0.008	0.09	0.20
D	SEE VARIATIONS			
E	0.205	0.209	5.20	5.38
e	0.0256 BSC		0.65 BSC	
H	0.301	0.311	7.65	7.90
L	0.025	0.037	0.63	0.95
α	0°	8°	0°	8°

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	
D	0.239	0.249	6.07	6.33	14L
D	0.239	0.249	6.07	6.33	16L
D	0.278	0.289	7.07	7.33	20L
D	0.317	0.328	8.07	8.33	24L
D	0.397	0.407	10.07	10.33	28L



	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

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