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FAIRCHILD SEMICONDUCTOR®

February 2013

KA78L05AI
3-Terminal 0.1 A 5 V Positive Voltage Regulator

Features

- Maximum Output Current of 100 mA
- Output Voltage of 5 V
- Thermal Overload Protection
- Short-Circuit Current Limiting
- Output Voltage Offered in ±5% Tolerance

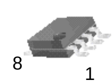
Description

The KA78L05AI of fixed-voltage monolithic integrated circuit voltage regulators are suitable for applications that required supply current up to 100 mA.

SOT-89

1. Output 2. GND 3. Input

8-SOIC



1. Output 2. GND 3. GND 4. NC
5. NC 6. GND 7. GND 8. Input

Ordering Information

Product Number	Package	Packing Method	Output Voltage Tolerance	Operating Temperature
KA78L05AIDTF	8-SOIC	Tape and Reel	±5%	-40 to +125°C
KA78L05AIMTF	SOT-89	Tape and Reel		

Block Diagram

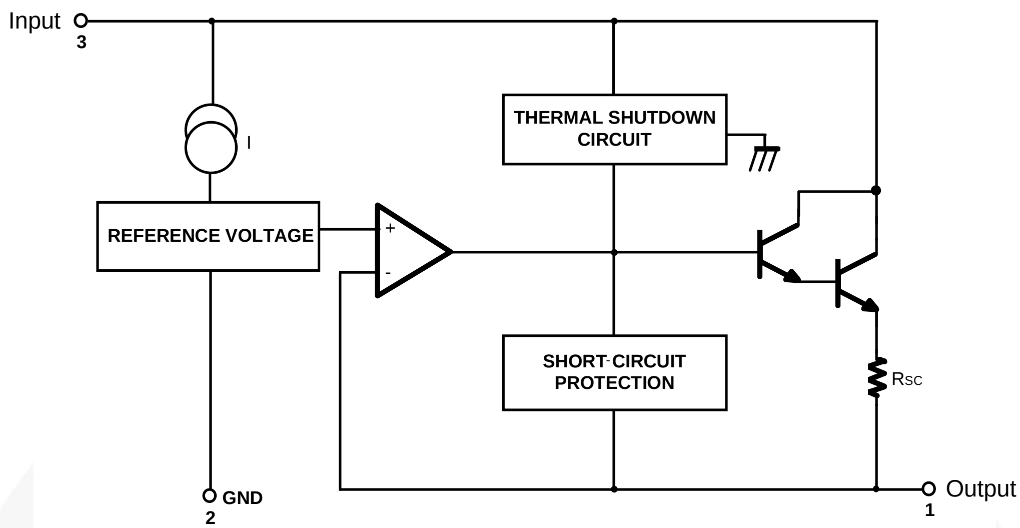


Figure 1. Block Diagram

Absolute Maximum Ratings[1]

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter		Value	Unit
V_I	Input Voltage		30	V
T_J	Maximum Operating Junction Temperature		150	°C
T_{OPR}	Operating Temperature Range		-40 to +125	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C
$R_{\theta JA}$	Thermal Resistance Junction-Air	SOT-89	225	°C/W
		8-SOIC	160	°C/W

Note:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.
   Electrical specifications do not apply when operating the device outside of its stated operating conditions.

Electrical Characteristics

V_I = 10 V, I_O = 40 mA, -40°C ≤ T_J ≤ 125°C, C_I = 0.33 μF, C_O = 0.1 μF, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_O	Output Voltage	T_J = 25°C		4.8	5.0	5.2	V
ΔV_O	Line Regulation(2)	T_J = 25°C	7 V ≤ V_I ≤ 20 V		8	150	mV
			8 V ≤ V_I ≤ 20 V		6	100	mV
ΔV_O	Load Regulation(2)	T_J = 25°C	1 mA ≤ I_O ≤ 100 mA		11	60	mV
			1 mA ≤ I_O ≤ 40 mA		5.0	30.0	mV
V_O	Output Voltage	7 V ≤ V_I ≤ 20 V	1 mA ≤ I_O ≤ 40 mA	4.75		5.25	V
		7 V ≤ V_I ≤ V_{MAX}(3)	1 mA ≤ I_O ≤ 70 mA	4.75		5.25	V
I_Q	Quiescent Current	T_J = 25°C			2.0	5.5	mA
ΔI_Q	Quiescent Current Change — With Line	8 V ≤ V_I ≤ 20 V				1.5	mA
ΔI_Q	Quiescent Current Change — With Load	1 mA ≤ I_O ≤ 40 mA(4)				0.5	mA
V_N	Output Noise Voltage(4)	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz			40		μV/Vo
$\Delta V_O/\Delta T$	Temperature Coefficient of V_O (4)	I_O = 5 mA			-0.65		mV/°C
RR	Ripple Rejection(4), (5)	f = 120 Hz, 8 V ≤ V_I ≤ 18 V, T_J = 25°C		41	80		dB
V_D	Dropout Voltage	T_J = 25°C			1.7		V

Notes:

2. The maximum steady-state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represents pulse test conditions with junction temperature as indicated at the initiation of tests.
3. Power dissipation P_D ≤ 0.75 W.
4. These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.
5. Recommend minimum load capacitance of 0.01 μF to limit high-frequency noise.

Typical Application[6]

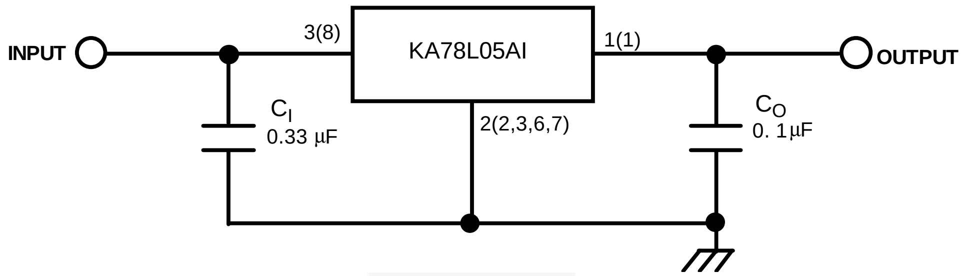


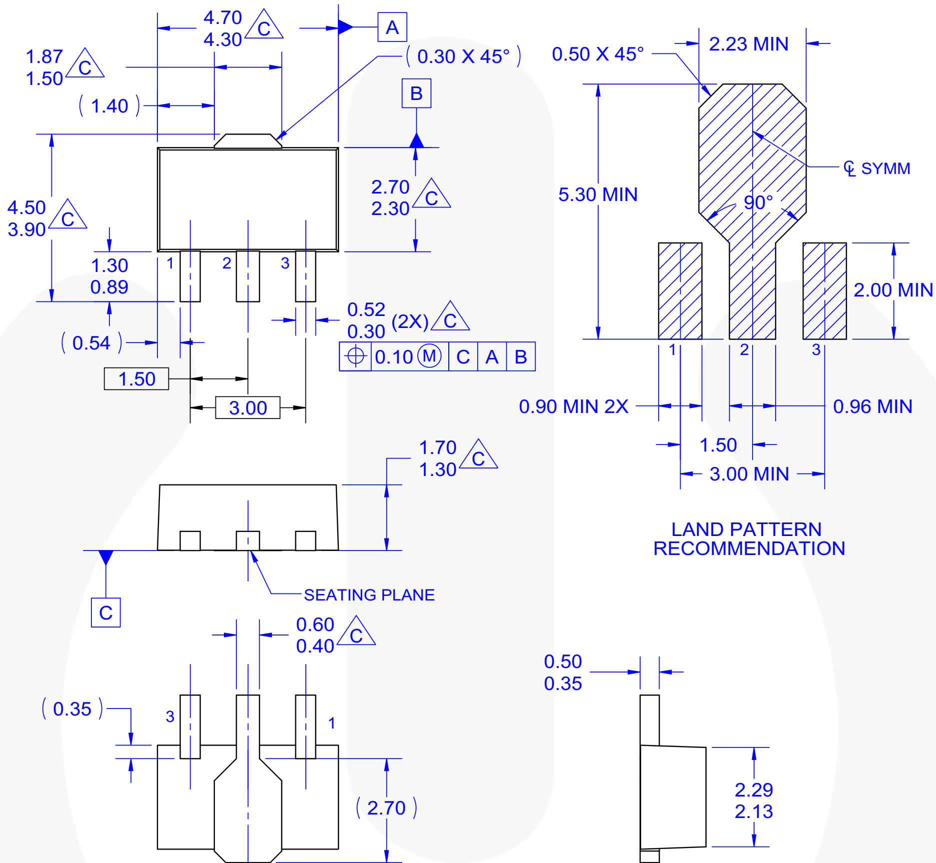
Figure 2. Typical Application

Note:

6. C_I is required if the regulator is located an appreciable distance from the power supply filter. Though C_O is not needed for stability, it improves transient response. Bypass capacitors are recommended for optimum stability and transient response and should be located as close as possible to the regulator.

Physical Dimensions

SOT-89



NOTES: UNLESS OTHERWISE SPECIFIED.

A. REFERENCE TO JEDEC TO-243 VARIATION AA.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DOES NOT COMPLY JEDEC STANDARD VALUE.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSION.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. DRAWING FILE NAME: MA03CREV2

Figure 3. 3-Lead, SOT-89, JEDEC TO-243, Option AA

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Physical Dimensions (Continued)

8-SOIC

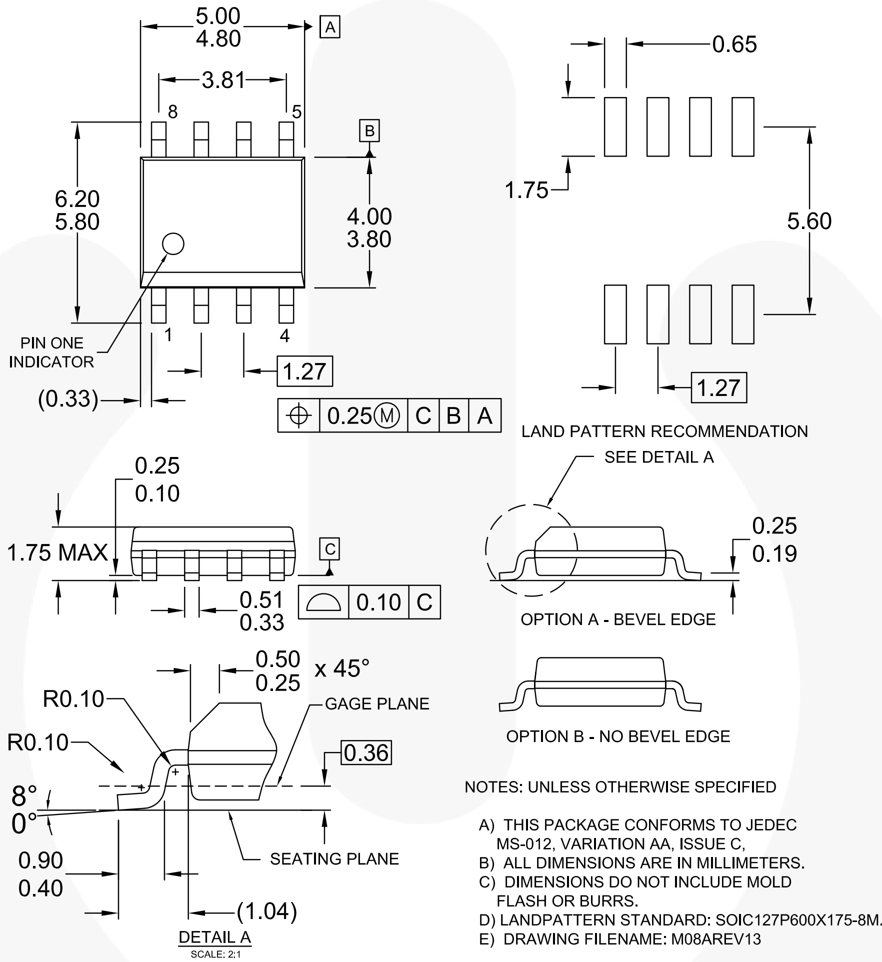

Figure 4. 8LD, SOIC, JEDEC MS-012, 0.150" NARROW BODY

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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