ConnectCore®

for i.MX51

Hardware Reference Manual

Revision history—90001128

Revision	Date	Description
L	September, 2013	Changed storage temperature to -40ºC to +85ºC (-40ºF to +185ºF) on page 129. Revised Bottom View image on page 149. Revised Side View image on page 150.
M	May, 2014	Correct inaccuracy and sharpen clarity on the high temp start up issue.
N	November, 2014	Miscellaneous editorial updates. Updated the voltages for the table in Coin cell input (VCC_COINCELL). Added a table of related publications.
P	June, 2017	Updated branding and added statements for RED compliance.
R	April, 2018	Added coin cell input topic.

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About the module

The network-enabled ConnectCore for i.MX51 is a highly integrated System-on-Module (SOM) solution based on the new Freescale® i.MX51X application processor with a high-performance ARM® Cortex-A8® core, powerful multimedia options, and a complete set of peripherals.

The module combines the fast integration, reliability and design flexibility of an off-the-shelf SOM with complete out-of-the-box software development support for platforms such as Microsoft® Windows® Embedded CE 6.0, Windows Embedded Compact 7Digi® Embedded Linux® and Timesys® LinuxLink®.

With industry-leading performance and key features like a dual-display interface and a hardware encryption engine, the module is the ideal choice for a broad range of target markets including medical, digital signage, security/access control, retail, industrial/building automation, transportation and more.

Complete and cost-efficient Digi JumpStart Kits™ for Microsoft Windows Embedded CE 6.0 and Linux allow immediate and professional embedded product development with dramatically reduced design risk and time-to-market.

Features and functionality

The ConnectCore for i.MX51 module is based on the i.MX51 processor from Freescale. This processor offers a high number of interfaces. Most of these interfaces are multiplexed and are not available simultaneously. The module has the following features:

- High-end, low-power 32-bit System-on-Module
- 600/800 MHZ ARM Cortex-A8 core
  - 32 kB L1 instruction and 32 kB L1 data cache
  - 256 kB L2 cache
  - NEON co-processor
  - Vector Floating Point (VFP) unit
- SLC and MLC NAND flash support on module
- Up to 512 MB 32-bit/200 MHZ DDR2-400 memory
- Debug interfaces
  - Joint Test Action Group (JTAG)
  - Embedded Trace Macrocell™ (ETM) / Embedded Trace Buffer (ETB)
- Real Time Clock (RTC)
- Security co-processor
  - Encryption: Advanced Encryption Standard (AES), Data Encryption Standard (DES), 3DES and RC4
  - Hashing algorithms: Message Digest (MD)5, Secure Hash Algorithm (SHA)-1, SHA-224 and SHA-256
- Timer
- Watchdog
- Up to three universal asynchronous receiver/transmitter (UART) ports, up to 4 Mb/s each
- Up to three Serial Peripheral Interface (SPI), two of them up to 54 Mb/s each
- Two Inter-Integrated Circuit (I2C) (up to 400 kb/s)
- Three memory card interfaces (two for the wireless version of the module)
  - SD/Secure Digital Input Output (SDIO) - 1 and 4-bits (up to 200 Mb/s)
  - MultiMediaCard (MMC) - 1, 4 and 8-bits (up to 416 Mb/s)
- USB
- Up to 3x USB 2.0 High-Speed USB Host ports
- One USB 2.0 On-The-Go USB port with integrated Physical Layer (PHY) on the module

- 1-wire
- Keypad 6x4
- Two independent pulse-width modulation (PWM) interfaces
- 8, 16-bit External Memory interface
- General-purpose input/output (GPIO) with interrupt capabilities
- Up to 3x 10-bit analog-to-digital converter (ADC) channels
- Multimedia
  - 2x Camera ports
  - 2x Display ports
  - 4-wire touch screen
- Sony/Philips Digital Interface Forma (SPDIF) output
- Three I2S / Audio Codec '97 (AC'97) / Synchronous Serial Interfaces (SSI), up to 1.4Mb/s each
- On-module three axis accelerometer (optional)
- On-module 10/100 Ethernet controller (optional)
- Second on-module 10/100Mb Ethernet interface (optional)
- 2.4 GHz and 5 GHz Institute of Electrical and Electronics Engineers (IEEE) 802.11a/b/g/n wireless local area network (LAN) interface (optional)
- Complete Microsoft Windows Embedded CE 6.0 and Linux platform support with full source code

Module variant

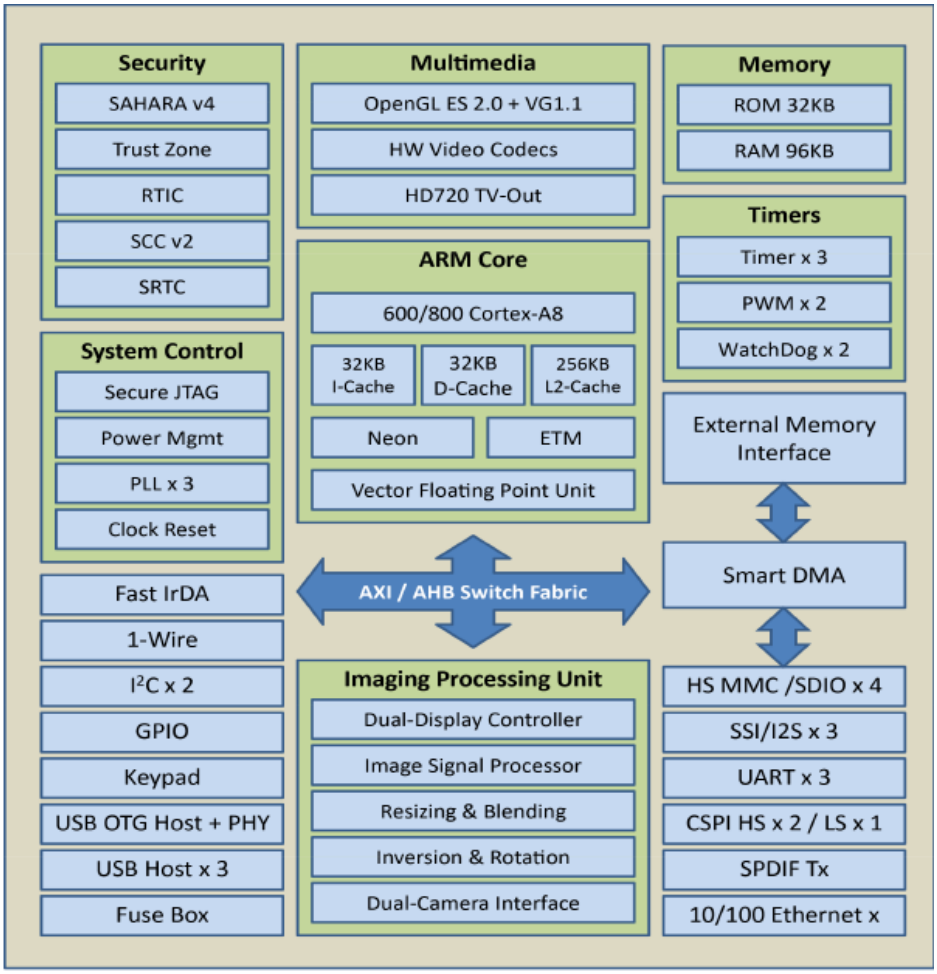
The ConnectCore for i.MX51 module is available with various population options such as network interfaces (Ethernet, wireless local area network [WLAN]), memory (flash, random-access memory [RAM]), processor (speed grade/operating temperature) and others.

Block diagram

The next figures show the block diagram of the Freescale i.MX515 central processing unit (CPU) and the block diagram of the ConnectCore for i.MX51 module.

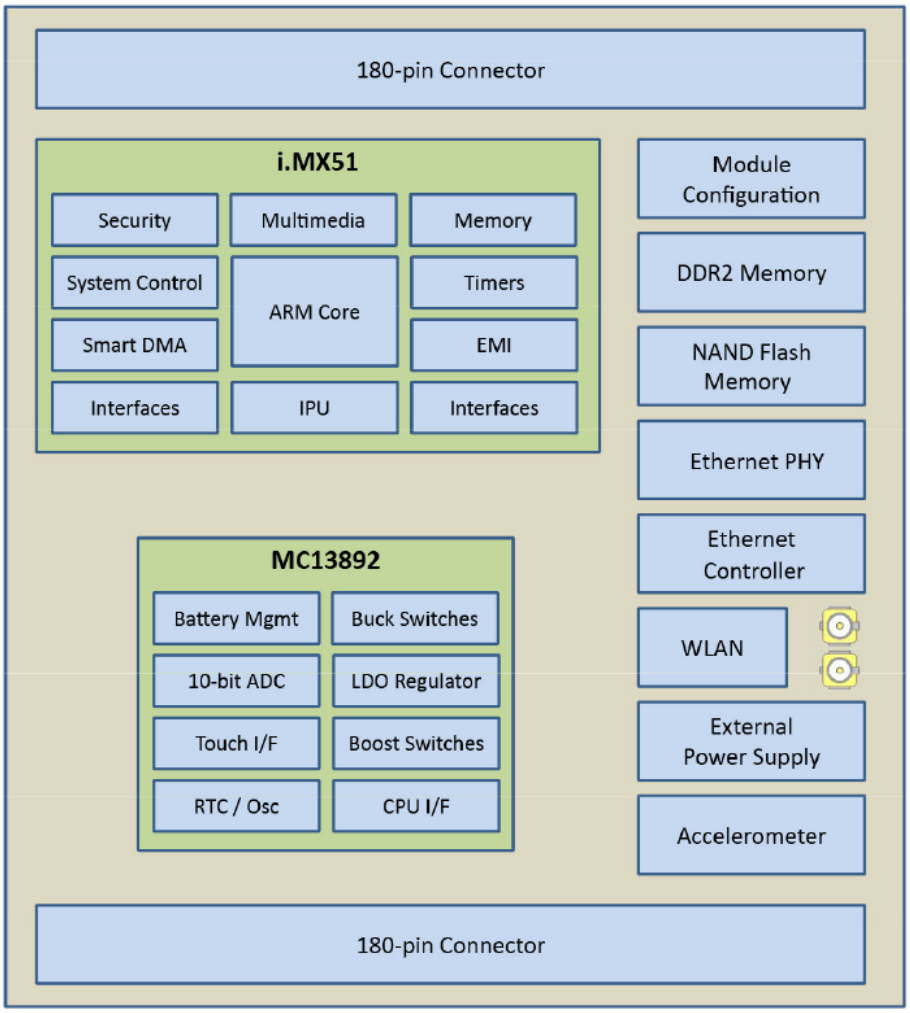
CPU

Freescale i.MX515



Module

ConnectCore I.MX51


180-pin Connector
i.MX51
Security
Multimedia
Memory
System Control
ARM Core
Timers
Smart DMA
EMI
Interfaces
IPU
Interfaces
MC13892
Battery Mgmt
Buck Switches
10-bit ADC
LDO Regulator
Touch I/F
Boost Switches
RTC / Osc
CPU I/F
Module Configuration
DDR2 Memory
NAND Flash Memory
Ethernet PHY
Ethernet Controller
WLAN
External Power Supply
Accelerometer
180-pin Connector

Module pinout

The module has two 180-pin connectors, J1 and J2. The following tables describe each pin, its properties, and its use on the module and development board. The DC parameters for each I/O type are defined in the I/O DC parameters.

The “Use on module” column shows the connection of the signals on the module. The format of this column is “component: pad_name,” where “component” is the chip where the signals are connected, and “pad_name” is the name of the pad where the signals are connected as they are defined in the component’s datasheet.

Pinout legend

I	Input
O	Output
IO	Input or output
P	Power
#	Low level active signal

Pinout definitions

GPIO - General Purpose IO

UHVIO - Ultra High Voltage IO

HSGPIO - High Speed GPIO

LVIO - Low Voltage IO (meaning 1.8V)

The I/O Type descriptions can be read as follows:

- 18 - 1.8V logic level switching (for example, GPIO18)
- 27 - 2.775V logic level switching (for example, GPIO27)
- 31 - 3.15V logic level switching (for example, UHVIO31)
- 33 - 3.3V logic level switching (for example, UHVIO33)

J1 pinout

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:1	GPIO27	CSI1_D8/GPIO3_12	i.MX51: CSI1_D8	Not used	
J1:2	GPIO27	CSI1_D9/GPIO3_13	i.MX51: CSI1_D9	Camera 1 reset	
J1:3	HSGPIO27	CSI1_D10	i.MX51: CSI1_D10	Camera 1 data	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:4	HSGPIO27	CSI1_D11	i.MX51: CSI1_D11	Camera 1 data	
J1:5	HSGPIO27	CSI1_D12	i.MX51: CSI1_D12	Camera 1 data	
J1:6	HSGPIO27	CSI1_D13	i.MX51: CSI1_D13	Camera 1 data	
J1:7	HSGPIO27	CSI1_D14	i.MX51: CSI1_D14	Camera 1 data	
J1:8	HSGPIO27	CSI1_D15	i.MX51: CSI1_D15	Camera 1 data	
J1:9	HSGPIO27	CSI1_D16	i.MX51: CSI1_D16	Camera 1 data	
J1:10	HSGPIO27	CSI1_D17	i.MX51: CSI1_D17	Camera 1 data	
J1:11	HSGPIO27	CSI1_D18	i.MX51: CSI1_D18	Camera 1 data	
J1:12	HSGPIO27	CSI1_D19	i.MX51: CSI1_D19	Camera 1 data	
J1:13	GPIO27	CSI1_VSYNC/GPIO3_14	i.MX51: CSI1_VSYNC	Camera 1 vertical synchronization	
J1:14	GPIO27	CSI1_HSYNC/GPIO3_15	i.MX51: CSI1_HSYNC	Camera 1 horizontal synchronization	
J1:15	GPIO27	CSI1_PIXCLK	i.MX51: CSI1_PIXCLK	Camera 1 pixel clock	
J1:16	GPIO27	CSI1_MCLK	i.MX51: CSI1_MCLK	Camera 1 and 2 Master clock	
J1:17	-	GND	-	-	
J1:18	-	GND	-	-	
J1:19	WLAN	WLAN_TDO	WLAN: TDO	Not used	
J1:20	WLAN	WLAN_TCK	WLAN: TCK	Not used	
J1:21	WLAN	WLAN_TDI	WLAN: TDI	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:22	WLAN	WLAN_TMS	WLAN: TMS	Not used	
J1:23	WLAN	WLAN_LED	WLAN: LED_ON	WLAN light-emitting diode (LED)	
J1:24	WLAN	RS_BT_PRIORITY	WLAN: BT_ PRIORITY	Not used	
J1:25	WLAN	RS_WLAN_ACTIVE	WLAN: WLAN_ ACTIVE	Not used	
J1:26	WLAN	RS_BT_ACTIVE	WLAN: BT_ACTIVE	Not used	
J1:27	LVIO	BOOT_MODE0	i.MX51: BOOT_ MODE0	Boot Mode selection	Boot configuratio n not available in EA Kit
J1:28	GPIO33	WLAN_DISABLE#	WLAN Power Supply Switch	WLAN Disable Jumper (J17)	This signal switch ON/OFF the supply of WLAN
J1:29	LVIO	BOOT_MODE1	i.MX51: BOOT_ MODE1	Boot Mode selection	Boot configuratio n not available in EA Kit
J1:30	-	VLIO	MC13892: BATT	Battery supply	
J1:31	-	VLIO	MC13892: BATT	Battery supply	
J1:32	-	VCHRG	MC13892: CHRGRAW	Charger supply	
J1:33	-	+2.775V	-	-	
J1:34	-	VCHRG	MC13892: CHRGRAW	Charger supply	
J1:35	-	+2.775V	-	-	
J1:36	-	+2.775V	-	-	
J1:37	PMIC_ GPO	MC13892_GPO1	MC13892: GPO1	Reserved	
J1:38	-	+2.775V	-	-	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:39	PMIC_ PWRON	PMIC_PWRON1	MC13892: PWRON1	Connected to Power Button (S11)	Suspend / Wake-up button
J1:40	PMIC_ STDBY	PMIC_STDBY_REQ	i.MX51: PMIC_ STBY_REQ MC13892: STANDBY	Reserved	Output from i.MX51 to put MC13892 in low power mode
J1:41	PMIC_ INT	PMIC_INT_REQ	i.MX51: PMIC_INT_ REQ	Reserved	This high-priority interrupt input on i.MX51 is not used. The output interrupt from PMIC is connected to standard interrupt GPIO_5 on i.MX51.
J1:42	PMIC_ PWGTDRV	PWRGTDRV1	MC13892: PWRGTDRV1	Not used	
J1:43	PMIC_ LED	CHRGLED	MC13892: CHRGLED	Battery Charging LED	
J1:44	PMIC_ PWGTDRV	PWRGTDRV2	MC13892: PWRGTDRV2 +3.3V_REG: ENABLE	Not used	Used on module to enable / disable the +3.3V supply
J1:45	PMIC_SE	CHRGSE1#	MC13892: CHRGSE1#	Charger detection circuit	This circuit is needed to boot from charger
J1:46	-	VCC_COINCELL	MC13892: LICELL	Coincell voltage	
J1:47	-	VLIO	MC13892: BATT	Battery supply	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:48	-	VCHRG	MC13892: CHRGRAW	Charger supply	
J1:49	-	VLIO	MC13892: BATT	Battery supply	
J1:50	-	VCHRG	MC13892:CHRGRAW	Charger supply	
J1:51	-	VLIO	MC13892: BATT	Battery supply	
J1:52	-	VCHRG	MC13892:CHRGRAW	Charger supply	
J1:53	ETH	ETH1_TX+	ETH_PHY: TXP	Ethernet 1 Tx+	
J1:54	ETH	ETH1_RX+	ETH_PHY: RXP	Ethernet 1 Rx+	
J1:55	ETH	ETH1_TX-	ETH_PHY: TXN	Ethernet 1 Tx-	
J1:56	ETH	ETH1_RX-	ETH_PHY: RXN	Ethernet 1 Rx-	
J1:57	-	GND	-	-	
J1:58	GPIO33	ETH1_LINK	ETH_PHY: LED1	Ethernet 1 Link LED	
J1:59	GPIO27	DISPB2_SER_DIN/GPIO3_5	i.MX51: DISPB_2_SER_DIN	GPIO1 signal to LCD connectors	
J1:60	GPIO33	ETH1_ACTIVITY	ETH_PHY: LED2	Ethernet 1 Activity LED	
J1:61	GPIO27	DISPB2_SER_RS/GPIO3_8	i.MX51: DISPB2_SER_RS	USB Host Reset	In Early Availability Kit USB host and Digital IO interface cannot be used at the same time.
J1:62	GPIO27	DISPB2_SER_DIO/GPIO3_6	i.MX51: DISPB2_SER_DIO	User button 1 & Digital IO 7	
J1:63	GPIO27	DISP2_DATA0/MII_RXD3/USBH3_CLK	i.MX51: DISP2_DATA0 ETH_PHY: RXD3	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:64	GPIO27	DISPB2_SER_CLK_ GPIO3_7	i.MX51: DISPB2_ SER_CLK	Camera 2 Reset	
J1:65	HSGPIO2 7	DISP2_DATA2	i.MX51: DISP2_ DATA2	LCD2 Data	
J1:66	GPIO27	DISP2_DATA1/MII_RX_ ER/USBH3_DIR	i.MX51: DISP2_ DATA1 ETH_PHY: RXD4	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:67	HSGPIO2 7	DISP2_DATA4	i.MX51: DISP2_ DATA4	LCD2 Data	
J1:68	HSGPIO2 7	DISP2_DATA3	i.MX51: DISP2_ DATA3	LCD2 Data	
J1:69	GPIO27	DISP2_DATA6/MII_ TXD1/USBH3_STP	i.MX51: DISP2_ DATA6 ETH_PHY: TXD1	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:70	HSGPIO2 7	DISP2_DATA5	i.MX51: DISP2_ DATA5	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:71	GPIO27	DISP2_DATA8/MII_ TXD3/USBH3_DATA0	i.MX51: DISP2_ DATA8 ETH_PHY: TDX3	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:72	GPIO27	DISP2_DATA7/MII_ TXD2/UBH3_NXT	i.MX51: DISP2_ DATA7 ETH_PHY: TDX2	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:73	GPIO27	DISP2_DATA10/MII_ COL/USBH3_DATA2	i.MX51: DISP2_ DATA10 ETH_PHY: COL	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:74	GPIO27	DISP2_DATA9/MII_TXEN/USBH3_DATA1	i.MX51: DISP2_DATA9 ETH_PHY: TXEN	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:75	GPIO27	DISP2_DAT12/MII_RX_DV/USBH3_DATA4	i.MX51: DISP2_DATA12 ETH_PHY: RXDV	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:76	GPIO27	DISP2_DAT11/MII_RX_CLK/USBH3_DATA3	i.MX51: DISP2_DATA11 ETH_PHY: RXCLK	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:77	GPIO27	DISP2_DATA14/MII_RXD0/USBH3_DATA6	i.MX51: DISP2_DATA14 ETH_PHY: RXD0	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:78	GPIO27	DISP2_DAT13/MII_TX_CLK/USBH3_DATA5	i.MX51: DISP2_DATA13 ETH_PHY: TXCLK	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:79	GPIO27	DI2_PIN2/MII_MDC	i.MX51: DI2_PIN2 ETH_PHY: MDC	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:80	GPIO27	DISP2_DAT15/MII_TXD0/USBH3_DATA7	i.MX51: DISP2_DATA15 ETH_PHY: TXD0	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:81	GPIO27	DI2_PIN4/MII_CRS	i.MX51: DI2_PIN4 ETH_PHY: CRS	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:82	-	GND	-	-	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:83	RGB	IOR	i.MX51: IOR	Not used	
J1:84	GPIO27	DI2_DISP_CLK/MII_RXD1	i.MX51: DI2_DISP_CLK ETH_PHY: RXD1	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:85	RGB	IOR_BACK	i.MX51: IOR_BACK	Not used	
J1:86	GPIO27	DI2_PIN3/MII_MDIO	i.MX51: DI2_PIN3 ETH_PHY: MDIO	LCD2 Data	Ethernet 1 and LCD2 cannot be used at the same time.
J1:87	RGB	IOB	i.MX51: IOB	Not useD	
J1:88	IOG	IOG	i.MX51: IOG	Not used	
J1:89	RGB	IOB_BACK	i.MX51: IOB_BACK	Not used	
J1:90	RGB	IOG_BACK	i.MX51: IOG_BACK	Not used	
J1:91	GPIO18	JTAG_TCK	i.MX51: JTAG_TCK	JTAG Connector	
J1:92	GPIO18	JTAG_TRST#	i.MX51: JTAG_TRST#	JTAG Connector	
J1:93	GPIO18	JTAG_TMS	i.MX51: JTAG_TMS	JTAG Connector	
J1:94	GPIO18	JTAG_MOD#	i.MX51: JTAG_MOD#	JTAG Mod Selection	
J1:95	GPIO18	JTAG_TDI	i.MX51: JTAG_TDI	JTAG Connector	
J1:96	GPIO18	JTAG_DE#	i.MX51: JTAG_DE_B	JTAG Connector	
J1:97	GPIO18	JTAG_TDO	i.MX51: JTAG_TDO	JTAG Connector	
J1:98	LVIO	RESET_IN#	i.MX51: RESET_IN_B MC13892: RESETB	Not used	Warm reset input to i.MX51.

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:99	LVIO	POR#	i.MX51: POR_B MC13892: RESETBMCU	LCD 1 & 2 Reset, JTAG Connector and Reset Button (S4)	Cold reset input to i.MX51. Used to reset the module and peripherals on the Dev. Kit.
J1:100	-	+1.8V		-	
J1:101	-	GND		-	
J1:102	-	GND		-	
J1:103	ETH	ETH2_TX+/ETH2_DA+	ETH_CTRL: TPO+	Ethernet 2 Tx+	
J1:104	ETH	ETH2_RX+/ETH2_DB+	ETH_CTRL: TPI+	Ethernet 2 Rx+	
J1:105	ETH	ETH2_TX-/ETH2_DA-	ETH_CTRL: TPO-	Ethernet 2 Tx-	
J1:106	ETH	ETH2_RX-/ETH2_DB-	ETH_CTRL: TPI-	Ethernet 2 Rx-	
J1:107	-	-	-	-	-
J1:108	-	-	-	-	-
J1:109	-	-	-	-	-
J1:110	-	-	-	-	-
J1:111	GPIO33	ETH2_ACTIVITY#	ETH_CTRL: GPIO1/LED2#	Ethernet 2 Activity LED	
J1:112	GPIO33	ETH2_LINK#	ETH_CTRL: GPIO0/LED1#	Ethernet 2 Link LED	
J1:113	GPIO18	EIM_CS0/GPIO2_25	i.MX51: EIM_CS0	Peripheral Application Chip Select	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:114	GPIO18	EIM_CS1/GPIO2_26	i.MX51: EIM_CS1	Not used	
J1:115	GPIO18	EIM_CS2/GPIO2_27/FEC_RDATA2/SISG5/CSI1_D4/AUD5_TXD	i.MX51: EIM_CS2	Not used	
J1:116	GPIO18	EIM_CS3/GPIO2_28/FEC_RDATA3/SSI_EXT2_CLK/CSI1_D5/AUD5_RXD	i.MX51: EIM_CS3	Not used	
J1:117	GPIO18	EIM_CS4/GPIO2_29/FEC_RX_ER/SSI_EXT1_CLK/CSI1_D6/AUD5_TXC	i.MX51: EIM_CS4	Not used	
J1:118	GPIO18	EIM_CS5/GPIO2_30/FEC_CRS/DI1_EXT_CLK/CSI1_D7/AUD5_TXFS	i.MX51: EIM_CS4 EHT_CTRL: CS#	Reserved	
J1:119	GPIO18	EIM_DTACK/GPIO2_31	i.MX51: EIM_DTACK	Not used	
J1:120	GPIO18	EIM_LBA/GPIO3_1	i.MX51: EIM_LBA	Not used	
J1:121	GPIO18	EIM_DA0/TRACE16	i.MX51: EIM_DA0 ETH_CTRL: A1	Peripheral Application Data / Address	
J1:122	GPIO18	EIM_DA1/TRACE17	i.MX51: EIM_DA1 ETH_CTRL: A2	Peripheral Application Data / Address	
J1:123	GPIO18	EIM_DA2/TRACE18	i.MX51: EIM_DA2 ETH_CTRL: A3	Peripheral Application Data / Address	
J1:124	GPIO18	EIM_DA3/TRACE19	i.MX51: EIM_DA3 ETH_CTRL: A4	Peripheral Application Data / Address	
J1:125	-	GND	-	-	
J1:126	GPIO18	EIM_DA5/TRACE21	i.MX51: EIM_DA5 ETH_CTRL: A6	Peripheral Application Data / Address	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:127	GPIO18	EIM_DA4/TRACE20	i.MX51: EIM_DA4 ETH_CTRL: A5	Peripheral Application Data / Address	
J1:128	GPIO18	EIM_DA7/TRACE23	i.MX51: EIM_DA7 ETH_CTRL: FIFO_SEL	Peripheral Application Data / Address	
J1:129	GPIO18	EIM_DA6/TRACE22	i.MX51: EIM_DA6 ETH_CTRL: A7	Peripheral Application Data / Address	
J1:130	-	GND	-	-	
J1:131	GPIO18	EIM_DA8/TRACE24	i.MX51: EIM_DA8	Peripheral Application Data / Address	
J1:132	GPIO18	EIM_DA9/TRACE25	i.MX51: EIM_DA9	Peripheral Application Data / Address	
J1:133	GPIO18	EIM_DA10/TRACE26	i.MX51: EIM_DA10	Not used	
J1:134	GPIO18	EIM_DA11/TRACE27	i.MX51: EIM_DA11	Not used	
J1:135	-	GND	-	-	
J1:136	GPIO18	EIM_DA13/TRACE29	i.MX51: EIM_DA13	Not used	
J1:137	GPIO18	EIM_DA12/TRACE28	i.MX51: EIM_DA12	Not used	
J1:138	GPIO18	EIM_DA15/TRACE31	i.MX51: EIM_DA15	Not used	
J1:139	GPIO18	EIM_DA14/TRACE30	i.MX51: EIM_DA14	Not used	
J1:140	-	GND	-	-	
J1:141	GPIO18	EIM_D16/GPIO2_0/USBH2_DATA0/UART2_CTS#/I2C1_SDA/AUD4_RXFS/TRACE0/AUD5_TXD	i.MX51: EIM_D16 ETH_CTRL: D0	Peripheral Application Data	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:142	GPIO18	EIM_D17/GPIO2_1/USBH2_DATA1/UART2_RXD/UART3_CTS#/SISG4/TRACE1/AUD5_RXD	i.MX51: EIM_D17 ETH_CTRL: D1	Peripheral Application Data	
J1:143	GPIO18	EIM_D18/GPIO2_2/USBH2_DATA2/UART2_TXD/UART3_RTS#/SISG5/TRACE2/AUD5_TXC	i.MX51: EIM_D18 ETH_CTRL: D2	Peripheral Application Data	
J1:144	GPIO18	EIM_D19/GPIO2_3/USBH2_DATA3/UART2_RTS#/I2C1_SCL/AUD4_RXC/TRACE3/AUD5_TXFS	i.MX51: EIM_D19 ETH_CTRL: D3	Peripheral Application Data	
J1:145	-	+3.15V	-	-	
J1:146	GPIO18	EIM_D21/GPIO2_5/USBH2_DATA5/AUD4_RXD/TRACE5	i.MX51: EIM_D21 ETH_CTRL: D5	Peripheral Application Data	
J1:147	GPIO18	EIM_D20/GPIO2_4/USBH2_DATA4/AUD4_TXD/TRACE4	i.MX51: EIM_D20 ETH_CTRL: D4	Peripheral Application Data	
J1:148	GPIO18	EIM_D23/GPIO2_7/USBH2_DATA7/SPDIF_OUT1/AUD4_TXFS/TRACE7	i.MX51: EIM_D23 ETH_CTRL: D7	Peripheral Application Data	
J1:149	GPIO18	EIM_D22/GPIO2_6/USBH2_DATA6/AUD4_TXC/TRACE6	i.MX51: EIM_D22 ETH_CTRL: D8	Peripheral Application Data	
J1:150	-	GND	-	-	
J1:151	GPIO18	EIM_D24/GPIO2_8/UART3_CTS#/I2C2_SDA/AUD6_RXFS/TRACE8	i.MX51: EIM_D24 ETH_CTRL: D8	Peripheral Application Data	
J1:152	GPIO18	EIM_D25/KEY_COL6/UART3_RXD/UART2_CTS#/CMPOUT1/TRACE9	i.MX51: EIM_D25 ETH_CTRL: D9	Peripheral Application Data	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:153	GPIO18	EIM_D26/KEY_COL7/UART3_TXD/UART2_RTS#/CMPOUT2/TRACE10	i.MX51: EIM_D26 ETH_CTRL: D10	Peripheral Application Data	
J1:154	GPIO18	EIM_D27/GPIO2_9/UART3_RTS#/I2C2_SCL/AUD6_RXC/TRACE11	i.MX51: EIM_D27 ETH_CTRL: D11	Peripheral Application Data	
J1:155	-	GND	-	-	
J1:156	GPIO18	EIM_D29/KEY_ROW5/SISG1/AUD6_RXD/TRACE13	i.MX51: EIM_D29 ETH_CTRL: D13	Peripheral Application Data	
J1:157	GPIO18	EIM_D28/KEY_ROW4/SISG0/AUD6_TXD/TRACE12	i.MX51: EIM_D28 ETH_CTRL: D12	Peripheral Application Data	
J1:158	GPIO18	EIM_D31/KEY_ROW7/SISG03/AUD6_TXFS/TRACE15	i.MX51: EIM_D31 ETH_CTRL: D15	Peripheral Application Data	
J1:159	GPIO18	EIM_D30/KEY_ROW6/SISG2/AUD6_TXC/TRACE14	i.MX51: EIM_D30 ETH_CTRL: D14	Peripheral Application Data	
J1:160	GPIO18	EIM_A17/GPIO2_11	i.MX51: EIM_A17	Not used	
J1:161	GPIO18	EIM_A16/GPIO2_10	i.MX51: EIM_A16	Not used	
J1:162	GPIO18	EIM_A19/GPIO2_13	i.MX51: EIM_A19	Not used	
J1:163	GPIO18	EIM_A18/GPIO2_12	i.MX51: EIM_A18	Not used	
J1:164	GPIO18	EIM_A21/GPIO2_15	i.MX51: EIM_A21	Boot Configuration Switch	
J1:165	GPIO18	EIM_A20/GPIO2_14	i.MX51: EIM_A20	Boot Configuration Switch	
J1:166	GPIO18	EIM_A23/GPIO2_17	i.MX51: EIM_A23	Not used	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:167	GPIO18	EIM_A22/GPIO2_16	i.MX51: EIM_A22	Not used	
J1:168	GPIO18	EIM_A25/GPIO2_19/USBH2_DIR/DI1_PIN4	i.MX51: EIM_A25	Not used	
J1:169	GPIO18	EIM_A24/GPIO2_18/USBH2_CLK	i.MX51: EIM_A24	Not used	
J1:170	GPIO18	EIM_A27/GPIO2_21/USBH2_NXT/SISG1/CSI2_DATA_EN/DI1_PIN1	i.MX51: EIM_A27	XBEE_SLEEP_RQ	
J1:171	GPIO18	EIM_A26/GPIO2_20/USBH2_STP/SISG0/CSI1_DATA_EN/DI2_EXT_CLK	i.MX51: EIM_A26	Not used	
J1:172	GPIO18	EIM_OE#/GPIO2_24	i.MX51: EIM_OE ETH_CTRL: RD#	Peripheral Application Output Enable	
J1:173	GPIO18	EIM_EB0	i.MX51: EIM_EB0	Not used	
J1:174	GPIO18	EIM_RW#	i.MX51: EIM_RW ETH_CTRL: WR#	Peripheral Application Read / Write	
J1:175	GPIO18	EIM_EB1	i.MX51: EIM_EB1	Not used	
J1:176	GPIO18	EIM_CRE/GPIO3_2	i.MX51: EIM_CRE	Peripheral Application Interrupt input	
J1:177	GPIO18	EIM_EB2/GPIO2_22/TRCTL/FEC_MDIO/SISG2/CSI1_D2/AUD5_RXFS/CMPOUT1	i.MX51: EIM_EB2	Peripheral Application Byte Enable 2	
J1:178	GPIO18	EIM_WAIT	i.MX51: EIM_WAIT	Not used	
J1:179	GPIO18	EIM_EB3/GPIO2_23/TRCLK/FEC_RDATA1/SISG3/CSI1_D3/AUD5_RXC/CMPOUT2	i.MX51: EIM_EB3	Peripheral Application Byte Enable 3	

Pin	I/O Type	Signal name	Use on module	Use on development board	Comments
J1:180	GPIO18	EIM_BCLK	i.MX51: EIM_BCLK	Peripheral Application Clock Burst	By default not connected on Development Board.

J2 pinout

CAUTION! Do not connect signals marked NANDF_* to GND during boot time if you want to boot from NAND flash.

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:1	HSGPIO27	DISP1_DAT0	i.MX51: DISP1_DAT0	HDMI, VGA and LCD1 Data	On the Development Kit, DISP1 and DISP2 are configured at 18-bit, and connected to 24-bit LCDs. On the Development Kit, some DISP1 signals are used to configure the boot process. On the Early Availability Kit, DISP1 and DISP2 are configured at 24-bit, and connected to 24-bit LCDs.
J2:2	HSGPIO27	DISP1_DAT1	i.MX51: DISP1_DAT1	HDMI, VGA and LCD1 Data	
J2:3	HSGPIO27	DISP1_DAT2	i.MX51: DISP1_DAT2	HDMI, VGA and LCD1 Data	
J2:4	HSGPIO27	DISP1_DAT3	i.MX51: DISP1_DAT3	HDMI, VGA and LCD1 Data	
J2:5	HSGPIO27	DISP1_DAT4	i.MX51: DISP1_DAT4	HDMI, VGA and LCD1 Data	
J2:6	HSGPIO27	DISP1_DAT5	i.MX51: DISP1_DAT5	HDMI, VGA and LCD1 Data	
J2:7	GPIO27	DISP1_DAT6	i.MX51: DISP1_DAT6	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:8	GPIO27	DISP1_DAT7	i.MX51: DISP1_DAT7	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:9	GPIO27	DISP1_DAT8	i.MX51: DISP1_DAT8	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:10	GPIO27	DISP1_DAT9	i.MX51: DISP1_DAT9	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:11	GPIO27	DISP1_DAT10	i.MX51: DISP1_DAT10	HDMI, VGA and LCD1 Data, Boot Configuration	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:12	GPIO27	DISP1_DAT11	i.MX51: DISP1_DAT11	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:13	GPIO27	DISP1_DAT12	i.MX51: DISP1_DAT12	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:14	GPIO27	DISP1_DAT13	i.MX51: DISP1_DAT13	HDMI, VGA and LCD1 Data, Boot Configuration	On the Development Kit, DISP1 and DISP2 are configured at 18-bit, and connected to 24-bit LCDs. On the Development Kit, some DISP1 signals are used to configure the boot process. On the Early Availability Kit, DISP1 and DISP2 are configured at 24-bit, and connected to 24-bit LCDs.
J2:15	GPIO27	DISP1_DAT14	i.MX51: DISP1_DAT14	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:16	GPIO27	DISP1_DAT15	i.MX51: DISP1_DAT15	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:17	GPIO27	DISP1_DAT16	i.MX51: DISP1_DAT16	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:18	GPIO27	DISP1_DAT17	i.MX51: DISP1_DAT17	HDMI, VGA and LCD1 Data, Boot Configuration	
J2:19	GPIO27	DISP1_DAT18	i.MX51: DISP1_DAT18	Not used	
J2:20	GPIO27	DISP1_DAT19	i.MX51: DISP1_DAT19	Not used	
J2:21	GPIO27	DISP1_DAT20	i.MX51: DISP1_DAT20	Boot Configuration	
J2:22	GPIO27	DISP1_DAT21	i.MX51: DISP1_DAT21	Boot Configuration	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:23	GPIO27	DISP1_DAT22	i.MX51: DISP1_DAT22	LCD2 Data	
J2:24	GPIO27	DISP1_DAT23	i.MX51: DISP1_DAT23	LCD2 Data	
J2:25	GPIO27	DI1_PIN2	i.MX51: DI1_PIN2	HDMI, VGA and LCD1 HSYNC	
J2:26	-	GND	-	-	
J2:27	GPIO27	DI1_PIN11/GPIO3_0	i.MX51: DI1_PIN11	LCD1 PWREN#	
J2:28	GPIO27	DI1_DISP_CLK	i.MX51: DI1_DISP_CLK	HDMI, VGA and LCD1 Clock	
J2:29	GPIO27	DI1_PIN13/GPIO3_2	i.MX51: DI1_PIN13	LCD1 and LCD2 GPIO2	
J2:30	GPIO27	DI1_PIN3	i.MX51: DI1_PIN3	HDMI, VGA and LCD1 VSYNC	
J2:31	GPIO27	DI1_PIN15	i.MX51: DI1_PIN15	HDMI, VGA and LCD1 DRDY	
J2:32	GPIO27	DI1_PIN12/GPIO3_1	i.MX51: DI1_PIN12	LCD2 PWREN#	
J2:33	GPIO27	DI_GP2	i.MX51: DI_GP2	Not used	
J2:34	GPIO27	DI_GP1	i.MX51: DI_GP1	Not used	
J2:35	GPIO27	DI_GP4/MII_RXD2	i.MX51: DI_GP4 LAN8710: RXD2	LCD2 DRDY	
J2:36	GPIO27	DI_GP3/MII_TX_ER	i.MX51: DI_GP3 LAN8710: INT#/TXER/TXD4	Not used	
J2:37	GPIO27	DI1_D1_CS/GPIO3_4	i.MX51: DI_D1_CS	LCD1 and LCD2 Touch selection input	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:38	GPIO27	DI1_D0_ CS/GPIO3_3	i.MX51: DI_D0_CS	LCD1 and LCD2 Touch selection input	
J2:39	ADIN	TOUCH_X1	MC13892: TSX1	LCD1 and LCD2 Touch X1	Analog input from Touch Screen
J2:40	ADIN	ADIN5	MC13892: ADIN5	Reserved	
J2:41	ADIN	TOUCH_X2	MC13892: TSX2	LCD1 and LCD2 Touch X2	Analog input from Touch Screen
J2:42	ADIN	ADIN6	MC13892: ADIN6	Not used	Analog input
J2:43	ADIN	TOUCH_Y1	MC13892: TSY1	LCD1 and LCD2 Touch Y1	Analog input from Touch Screen
J2:44	ADIN	ADIN7	MC13892: ADIN7	Not used	Analog input
J2:45	ADIN	TOUCH_Y2	MC13892: TSY2	LCD1 and LCD2 Touch Y2	Analog input from Touch Screen
J2:46	-	ADC_GND	-	-	
J2:47	-	GND	-	-	
J2:48	PMIC_ STDBY	ADTRIG	MC13892: ADTRIG	Not used	
J2:49	-	SWBST	MC13892: SWBST MC13892: VINUSB	-	Used on the module to power USB PHY
J2:50	-	LEDKP	MC13892: LEDKP	Reserved	
J2:51	PMIC_LED	LEDR	MC13892: LEDR	Not used	
J2:52	-	LEDAD	MC13892: LEDAD	Reserved	
J2:53	PMIC_LED	LEDG	MC13892: LEDG	Not used	
J2:54	-	LEDMD	MC13892: LEDMD	Reserved	
J2:55	PMIC_LED	LEDB	MC13892: LEDB	Not used	
J2:56	-	VSWLED	-	-	
J2:57	GPIO27	CSI2_D12/GPIO4_9	i.MX51: CSI2_D12	Camera 2 Data	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:58	GPIO27	CSI2_D13/GPIO4_10	i.MX51: CSI2_D13	Camera 2 Data	
J2:59	HSGPIO27	CSI2_D14	i.MX51: CSI2_D14	Camera 2 Data	
J2:60	HSGPIO27	CSI2_D15	i.MX51: CSI2_D15	Camera 2 Data	
J2:61	HSGPIO27	CSI2_D16	i.MX51: CSI2_D16	Camera 2 Data	
J2:62	HSGPIO27	CSI2_D17	i.MX51: CSI2_D17	Camera 2 Data	
J2:63	GPIO27	CSI2_D18/GPIO4_11	i.MX51: CSI2_D18	Camera 2 Data	
J2:64	GPIO27	CSI2_D19/GPIO4_12	i.MX51: CSI2_D19	Camera 2 Data	
J2:65	GPIO27	CSI2_VSYNC/GPIO4_13	i.MX51: CSI2_VSYNC	Camera 2 VSYNC	
J2:66	GPIO27	CSI2_HSYNC/GPIO4_14	i.MX51: CSI2_HSYNC	Camera 2 HSYNC	
J2:67	GPIO27	CSI2_PIXCLK_GPIO4_15	i.MX51: CSI2_PIXCLK	Camera 2 PIXCLK	
J2:68	-	GND		-	
J2:69	-	GND		-	
J2:70	DIG_USB	USB_OTG_ID	i.MX51: ID	USB OTG ID	
J2:71	AN_USB	USB_OTG_DP	i.MX51: DP	USB OTG DP	
J2:72	-	USB_OTG_VBUS	i.MX51: VBUS	USB OTG VBUS	
J2:73	AN_USB	USB_OTG_DN	i.MX51: DN	USB OTG DN	
J2:74	GPIO27	GPIO1_8/USB_PWR	i.MX51: GPIO_8	Not used	
J2:75	-	GND	-	-	
J2:76	GPIO27	GPIO1_2/PWM1/I2C2_SCL	i.MX51: GPIO1_2 MMA7455LR1:SCL	I^2C Bus Clock	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:77	GPIO27	GPIO1_ 7/MMA7455LR_ INT1	i.MX51: GPIO1_7 MMA7455LR1:INT1	Reserved	Accelerometer interrupt
J2:78	GPIO27	GPIO1_ 3/PWM2/I2C2_SDA	i.MX51: GPIO1_3 MMA7455LR1:SD	I^2C Bus Clock	
J2:79	GPIO27	GPIO1_ 6/MMA7455LR_ INT2	i.MX51: GPIO1_6 MMA7455LR1:INT2	Reserved	Accelerometer Interrupt
J2:80	PMIC_INT	CLK32K_PER	MC13892: CLK32K	Not used	
J2:81	-	GND	-	-	
J2:82	-	GND	-	-	
J2:83	-	CKIH1	i.MX51: CKIH1	Not used	
J2:84	-	CKIH2	i.MX51: CKIH2	Not used	
J2:85	UHVIO33	SD2_DATA0/SD1_ DATA1/CSPI_MISO	i.MX51: SD2_ DATA0 WLAN: SDIO_ DATA0	Reserved	SD bus 2 connected to WLAN. In modules without WLAN this SD bus can be used in the development boards.
J2:86	UHVIO33	SD2_CLK/I2C1_ SDA/SPI_SCLK	i.MX51: SD2_CLK WLAN: SDIO_CLK	Reserved	
J2:87	UHVIO33	SD2_DATA1/SD1_ DATA5	i.MX51: SD2_ DATA1 WLAN: SDIO_ DATA1	Reserved	
J2:88	UHVIO33	SD2_CMD/I2C1_ SCL/SPI_MOSI	i.MX51: SD2_CMD WLAN: SDIO_CMD	Reserved	
J2:89	UHVI0O3	SD2_DATA2/SDI_ DATA6	i.MX51: SD2_ DATA2 WLAN: SDIO_ DATA2	Reserved	
J2:90	GPIO27	KEY_COL0	i.MX51: KEY_COL0	XBee Reset#	
J2:91	UHVIO33	SD2_DATA3/SD1_ DATA7/SPI_SS2	i.MX51: SD2_ DATA3 WLAN: SDIO_ DATA3	Reserved	
J2:92	GPIO27	KEY_COL1	i.MX51: KEY_COL1	Not used	
J2:93	GPIO27	KEY_ROW0	i.MX51: ROW0	Not used	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:94	GPIO27	KEY_COL2	i.MX51: KEY_COL2	Not used	
J2:95	GPIO27	KEY_ROW1	i.MX51: ROW1	Not used	
J2:96	GPIO27	KEY_COL3	i.MX51: KEY_COL3	Not used	
J2:97	GPIO27	KEY_ROW2	i.MX51: ROW2	Not used	
J2:98	GPIO27	KEY_COL5/UART3_CTS#/I2C2_SDA	i.MX51: KEY_COL5	XBee RTS#	
J2:99	GPIO27	KEY_ROW3	i.MX51: KEY_ROW3	Not used	
J2:100	GPIO27	GPIO1_0/SD1_CD#/SPI_SS2	i.MX51: GPIO1_0	HDMI Interrupt	
J2:101	GPIO27	KEY_COL4/UART3_RTS#/I2C2_SCL	i.MX51: KEY_COL4	XBee_CTS#/UART3_RTS selection	
J2:102	GPIO27	GPIO1_1/SD1_WP#/SPI_MISO	i.MX51: GPIO1_1	User Button 2	
J2:103	GPIO27	OWIRE_LINE/GPIO1_24	i.MX51: OWIRE_LINE	One-Wire, HDMI SPDIF	
J2:104	UHVIO31	SD1_DATA0/AUD5_TXD/SPI_MOSI	i.MX51: SD1_DATA0	MicroSD ™ Data	
J2:105	UHVIO31	SD1_CMD/AUD5_RXFS/SPI_MOSI	i.MX51: SD1_CMD	MicroSD ™ Command	
J2:106	UHVIO31	SD1_DATA1/AUD5_RXD	i.MX51: SD1_DATA1	MicroSD ™ Data	
J2:107	UHVIO31	SD1_CLK/AUD5_RXC/SPI_SCLK	i.MX51: SD1_CLK	MicroSD ™ Clock	
J2:108	UHVIO31	SD1_DATA2/AUD5_TXC	i.MX51: SD1_DATA2	MicroSD ™ Data	
J2:109	GPIO27	WDOG1#	i.MX51: GPIO1_4	Reserved	HDMI Interrupt and PMIC Watchdog input cannot be used at the same time.
J2:110	UHVIO31	SD1_DATA3/AUD5_TXFS/SPI_SS1	i.MX51: SD1_DATA3	MicroSD ™ Data	
J2:111	GPIO27	CSPI1_MOSI/I2C1_SDA/GPIO4_22	i.MX51: CSPI1_MOSI MC13892: MOSI	SPI_MOSI	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:112	GPIO27	CSPI1_SS0_ PMIC/AUD4_ TXC/GPIO4_24	i.MX51: CSPI1_SS0 MC13892: CS	Reserved	
J2:113	GPIO27	CSPI1_ MISO/AUD4_ RXD/GPIO4_23	i.MX51: CSPI1_ MISO MC13892: MISO	SPI_MISO	
J2:114	GPIO27	CSPI1_SS1/AUD4_ TXD/GPIO4_25	i.MX51: CSPI1_SS1	SPI_SS1	
J2:115	GPIO27	CSPI1_SCLK/I2C1_ SCL/GPIO4_27	i.MX51: CSPI1_ SCLK MC13892: CLK	SPI_SCLK	
J2:116	GPIO27	CSPI1_RDY/AUD4_ TXFS/GPIO4_26	i.MX51: CSPI1_RDY	LCD1 and LCD2 SPI Chip Select	
J2:117	GPIO27	UART1_ RXD/GPIO4_28	i.MX51: UART1_ RXD	UART1 MEI	
J2:118	GPIO27	UART1_ RTS#/GPIO4_30	i.MX51: UART1_ RTS	UART1 MEI	
J2:119	GPIO27	UART1_ TXD/PWM2/GPIO4_ 29	i.MX51: UART1_ TXD	UART1 MEI	
J2:120	GPIO27	UART1_ CTS#/GPIO4_31	i.MX51: UART1_ CTS	UART1 MEI	
J2:121	GPIO27	UART2_ RXD/GPIO1_20	i.MX51: UART2_ RXD	UART2 Console	
J2:122	GPIO27	UART3_ RXD/UART1_ DTR#/GPIO1_22	i.MX51: UART3_ RXD	UART3/XBee	
J2:123	GPIO27	UART2_ TXD/GPIO1_21	i.MX51: UART2_ TXD	UART2 Console	
J2:124	GPIO27	UART3_ TXD/UART1_ DSR#/GPIO1_23	i.MX51: UART3_ TXD	UART3/XBee	
J2:125	GPIO27	USBH1_ DATA2/UART2_ TXD_GPIO1_13	i.MX51: USBH1_ DATA2	USB Host	
J2:126	-	GND	-	-	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:127	GPIO27	USBH1_ DATA4/CSPI_ SS0/GPIO1_15	i.MX51: USBH1_ DATA4	USB Host	
J2:128	GPIO27	USBH1_ DATA0/UART2_ CTS#/GPIO1_11	i.MX51: USBH1_ DATA0	USB Host (default) and UART2 Console	
J2:129	GPIO27	USBH1_ DATA6/CSPI_ SS3/GPIO1_17	i.MX51: USBH1_ DATA6	USB Host	
J2:130	GPIO27	USBH1_ DATA1/UART2_ RXD/GPIO1_12	i.MX51: USBH1_ DATA1	USB Host	
J2:131	GPIO27	USBH1_DIR/SPI_ MOSI/GPIO1_ 26/I2C2_SDA	i.MX51: USBH1_ DIR	USB Host	
J2:132	GPIO27	USBH1_ DATA3/UART2_ RTS#/GPIO1_14	i.MX51: USBH1_ DATA3	USB Host (default) and UART2 Console	
J2:133	GPIO27	USBH1_STP/SPI_ RDY/GPIO1_27	i.MX51: USBH1_ STP	USB Host	
J2:134	GPIO27	USBH1_ DATA5/CSPI_ SS1/GPIO1_16	i.MX51: USBH1_ DATA5	USB Host	
J2:135	GPIO27	USBH1_NXT/SPI_ MISO/GPIO1_28	i.MX51: USBH1_ NXT	USB Host	
J2:136	GPIO27	USBH1_ DATA7/CSPI1_ SS3/SPI2_ SS3/GPIO1-18	i.MX51: USBH1_ DATA7	USB Host	
J2:137	GPIO27	AUD3_BB_ TXD/GPIO4_18	i.MX51: AUD3_BB_ TXD	Audio CODEC and HDMI Audio	
J2:138	GPIO27	USBH1_CLK/SPI_ SCLK/GPIO1_ 25/I2C2_SCL/	i.MX51: USBH1_ CLK	USB Host	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:139	GPIO27	AUD3_BB_ RXD/UART3_ RXD/GPIO4_19	i.MX51: AUD_BB_ RXD	Audio CODEC	
J2:140	-	HS_I2C_ SCL/GPIO4_16	i.MX51: I2C_SCL	Not used	The HS_I2C interface is not working in i.MX51.
J2:141	GPIO27	AUD3_BB_ CK/GPIO4_20	i.MX51: AUD_BB_ CK	Audio CODEC and HDMI Audio	
J2:142	-	HS_I2C_ SDA/GPIO4_17	i.MX51: I2C_SDA	Not used	The HS_I2C interface is not working in i.MX51.
J2:143	-	+3.3V	-	-	
J2:144	GPIO27	AUD3_BB_ FS/UART3_ TXD/GPIO4_21	i.MX51: AUD_BB_ FS	Audio CODEC and HDMI Audio	
J2:145	UHVIO31	NANDF_D0/PATA_ D0/SD4_ DATA7/GPIO4_8	i.MX51: NANDF_D0 NAND_FLASH: I/O0	Reserved	
J2:146	-	+3.3V	-	-	
J2:147	UHVIO31	NANDF_D2/PATA_ D2/SD4_ DATA5/GPIO4_6	i.MX51: NANDF_D2 NAND_FLASH: I/O2	Reserved	
J2:148	UHVIO31	NANDF_D1/PATA_ D1/SD4_ DATA6/GPIO4_7	i.MX51: NANDF_D1 NAND_FLASH: I/O1	Reserved	
J2:149	UHVIO31	NANDF_D4/PATA_ D4/SD4_ CD/GPIO4_4	i.MX51: NANDF_D4 NAND_FLASH: I/O4	Reserved	
J2:150	UHVIO31	NANDF_D3/PATA_ D3/SD4_ DATA4/GPIO4_5	i.MX51: NANDF_D3 NAND_FLASH: I/O3	Reserved	
J2:151	UHVIO31	NANDF_D6/PATA_ D6/SD4_ LCTL/GPIO4_2	i.MX51: NANDF_D6 NAND_FLASH: I/O6	Reserved	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:152	UHVIO31	NANDF_D5/PATA_D5/SD4_WP/GPIO4_3	i.MX51: NANDF_D5 NAND_FLASH: I/O5	Reserved	
J2:153	UHVIO31	NANDF_D8/PATA_D8/GPIO4_0/SD3_DATA0	i.MX51: NANDF_D8	SD/MMC Data	
J2:154	UHVIO31	NANDF_D7/PATA_D7/GPIO4_1	i.MX51: NANDF_D7 NAND_FLASH: I/O7	Reserved	
J2:155	UHVIO31	NANDF_D10/PATA_D10/GPIO3_30/SD3_D2	i.MX51: NANDF_D10	SD/MMC Data	
J2:156	UHVIO31	NANDF_D9/PATA_D9/GPIO3_31/SD3_D1	i.MX51: NANDF_D9	SD/MMC Data	
J2:157	UHVIO31	NANDF_D12/PATA_D12/GPIO3_28/SD3_D4	i.MX51: NANDF_D12	Reserved	
J2:158	UHVIO31	NANDF_D11/PATA_D11/GPIO3_29/SD3_D3	i.MX51: NANDF_D11	SD/MMC Data	
J2:159	UHVIO31	NANDF_D14/PATA_D14/GPIO3_26/SD3_D6	i.MX51: NANDF_D14	Reserved	
J2:160	UHVIO31	NANDF_D13/PATA_D13/GPIO3_27/SD3_D5	i.MX51: NANDF_D13	Reserved	
J2:161	UHVIO31	NANDF_CS0#/GPIO3_16	i.MX51: NANDF_CS0 NAND_FLASH: CE#	Reserved	
J2:162	UHVIO31	NANDF_D15/PATA_D15/GPIO3_25/SD3_D7	i.MX51: NANDF_D15	Reserved	
J2:163	UHVIO31	NANDF_CS2#/PATA_CS0#/GPIO3_18	i.MX51: NANDF_CS2 NAND_FLASH: NC	Digital I/O Connector	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:164	UHVIO31	NANDF_ CS1#/GPIO3_17	i.MX51: NANDF_ CS1 NAND_FLASH: NC	SD/MMC Write Protect	
J2:165	UHVIO31	NANDF_ CS4#/PATA_ DA0/GPIO3_20	i.MX51: NANDF_ CS4	Digital I/O Connector	
J2:166	UHVIO31	NANDF_ CS3#/PATA_ CS1#/GPIO3_19	i.MX51: NANDF_ CS3 NAND_FLASH: NC	HDMI audio clock enable	
J2:167	UHVIO31	NANDF_ CS6#/PATA_ DA2/GPIO3_22	i.MX51: NANDF_ CS6	Digital I/O Connector	
J2:168	UHVIO31	NANDF_ CS5#/PATA_ DA1/GPIO3_21	i.MX51: NANDF_ CS5	Digital I/O Connector	
J2:169	UHVIO31	NANDF_RDY_ INT/GPIO3_24	i.MX51: NANDF_ RDY_INT	SD/MMC Command	
J2:170	UHVIO31	NANDF_ CS7#/GPIO3_23	i.MX51: NANDF_ CS7	SD/MMC Clock	SD clock and Digital IO cannot be used at the same time.
J2:171	UHVIO31	NANDF_ WE#/PATA_ DIOW/GPIO3_3	i.MX51: NANDF_ WE_B NAND_FLASH: WE#	Reserved	
J2:172	UHVIO31	GPIO_NAND/PATA_ INTRQ/GPIO3_12	i.MX51: GPIO_ NAND	SD/MMC Card Detect	
J2:173	UHVIO31	NANDF_ALE/PATA_ BUFFER_ EN/GPIO3_5	i.MX51: NANDF_ ALE NAND_FLASH: ALE	Reserved	
J2:174	UHVIO31	NANDF_RE#/PATA_ DIOR/GPIO3_4	i.MX51: NANDF_ RE_B NAND_FLASH: RE#	Reserved	
J2:175	UHVIO31	NANDF_ WP#/PATA_ DMACK/GPIO3_7	i.MX51: NANDF_ WP_B NAND_FLASH: WP#	Reserved	
J2:176	UHVIO31	NANDF_CLE/PATA_ RESET/GPIO3_6	i.MX51: NANDF_ CLE NAND_FLASH: CLE	Reserved	

Pin	Type	Signal name	Use on module	Use on development board	Comments
J2:177	UHVIO31	NANDF_ RB1/PATA_ IORDY/GPIO3_9	i.MX51: NANDF_ RB1 NAND_FLASH: NC	User LED2 and Digital I/O Connector	Must not be low during NAND Boot
J2:178	UHVIO31	NANDF_ RB0/PATA_ DMARQ/GPIO3_8	i.MX51: NANDF_ RB0 NAND_FLASH: R/B#	Reserved	Must not be low during NAND Boot
J2:179	UHVIO31	NANDF_ RB3/GPIO3_11	i.MX51: NANDF_ RB3 NAND_FLASH: NC	Digital I/O Connector	Must not be low during NAND Boot
J2:180	UHVIO31	NANDF_ RB2/GPIO3_10	i.MX51: NANDF_ RB2 NAND_FLASH: NC	User LED1 and Digital I/O Connector	Must not be low during NAND Boot

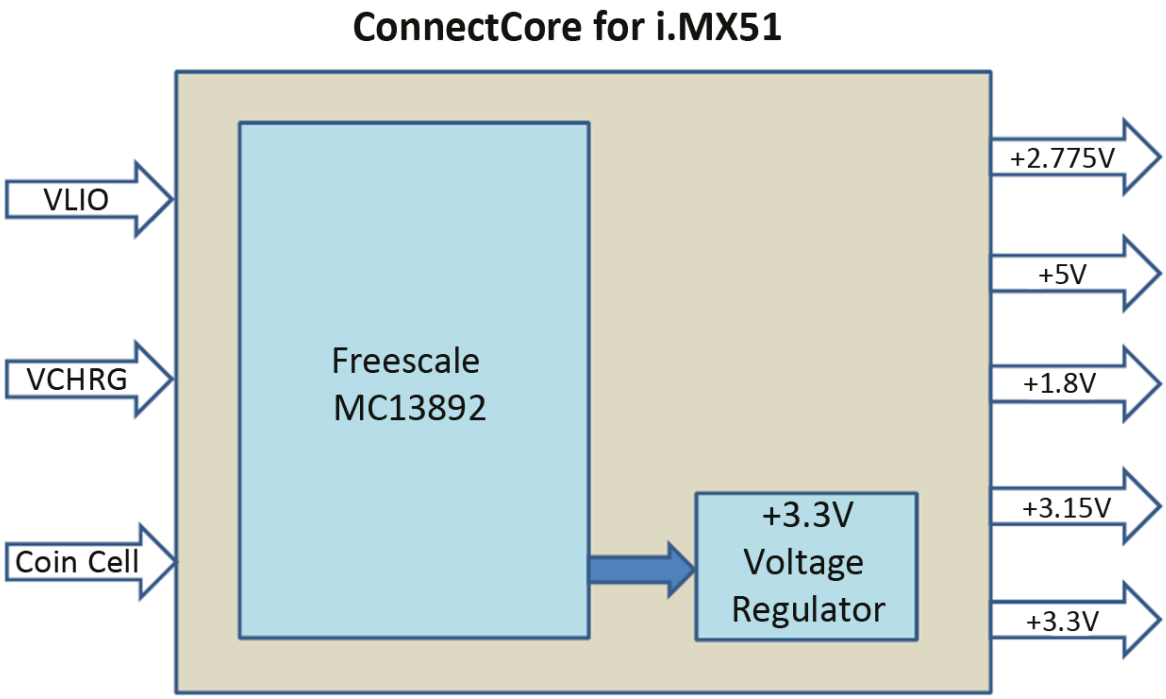
Notes:

- Many of the i.MX51 pins above have more functions than those shown in the reference names. For a complete list of pin multiplexing see Chapter 4 - External Signals and Pin Multiplexing of the *Freescale i.MX51 Multimedia Applications Processor Reference Manual*, Rev. 1 (or later).
- The signal name value listed for pins 85 and 115 (above) does not match what is listed in the schematics. This is simply a documentation error, functionality of these pins works according to what is listed in this guide.

Power

Module power supplies

The following figure shows the power supply scheme of the ConnectCore for i.MX51 module.



Supply inputs

The ConnectCore for i.MX51module has the following supply inputs:

- Battery input (VLIO)
- Charger input (VCHRG)
- Coin Cell input (VCC_COINCELL)

Coin cell input (VCC_COINCELL)

The VCC_COINCELL pin allows connection to either a coin cell or a supercap. This permits the RTC to keep running when the VLIO and VCHRG are at 0 volts. You can program the PMIC to allow current to be output from this pin while VLIO or VCHRG are present to charge the supercap (or Secondary Lithium Manganese coin cell). When in charge mode, this pin can output 60uA and the PMIC can be configured for a charge termination voltage in the range +2.5V to +3.3V.

The following table shows the current draw from the coin cell when there is no main battery attached:

Mode	Description	Typ	Max	Unit
RTC	All blocks disabled, no main battery attached, coin cell is attached.	36	50	uA

There are three types of components that can be connected to this pin: Lithium coin cells (Primary cell: non-rechargeable), Lithium coin cells (Secondary cell: rechargeable), and Supercaps. When a Primary Lithium coin cell is connected, the charger must be turned off and this pin is used strictly as an input. It is hazardous to attempt to charge Primary Lithium cells as they may vent or explode. Secondary Lithium coin cells are only made available directly to manufacturers of equipment that could use them, in that case they are normally required to design their product to prevent the user gaining access to this part since there is a danger to the user if by replacing it, they fit a primary type (the only sort that they are likely to be able to source) into the charging circuit. When a Secondary Lithium coin cell is used, the charge termination voltage is programmable. When a Supercap is used, the charge termination voltage should be set to the maximum value.

The advantage of using a Primary Lithium coin cell is that the energy density usually allows years of service since the self discharge rate is low. The advantage of using a Secondary Lithium coin cell is that the self discharge rate is usually sufficient to allow a few months of support for the RTC before it will need recharging. The advantage of the Supercap is that it is intrinsically safe and can out-last the Primary Lithium coin cell option, however the self discharge rate is high meaning that a 1F capacitor at +25° C is likely to support the RTC for approximately 5 to 10 days.

The minimum voltage of the coin cell supply is +2.5V. The maximum voltage of the coin cell supply is +3.6V.

Supply outputs

The ConnectCore for i.MX51 module provides the following supply outputs:

- +3.3 V
- +2.775 V
- SWBT (+5 V)
- +1.8 V
- +3.15 V

+3.3 V

The ConnectCore for i.MX51 module has a DC/DC converter to generate a +3.3V supply. This supply is used on the module to power the WLAN interface, the Ethernet PHY and the Ethernet Controller.

This power regulator can be enabled/disabled by the software to save power when the module is in the low power modes. The maximum current provided by this regulator is 1.2A.

The current available to supply off-module components is 400mA for the wireless variants of the ConnectCore for i.MX51, and 800mA for the wired variant of the ConnectCore for i.MX51.

+2.775 V

This supply is used on the module to power the i.MX51 peripherals, the accelerometer and the i.MX51 image processing unit. The maximum current provided by this supply is 100mA.

The current available to supply off-module components is 50mA.

SWBT (+5 V)

The voltage level of the SWBT supply is +5V. The maximum current provided by this supply is 300mA.

+1.8 V

This supply is generated on the internal regulator of the PMIC. The maximum current provided by this supply is 250mA.

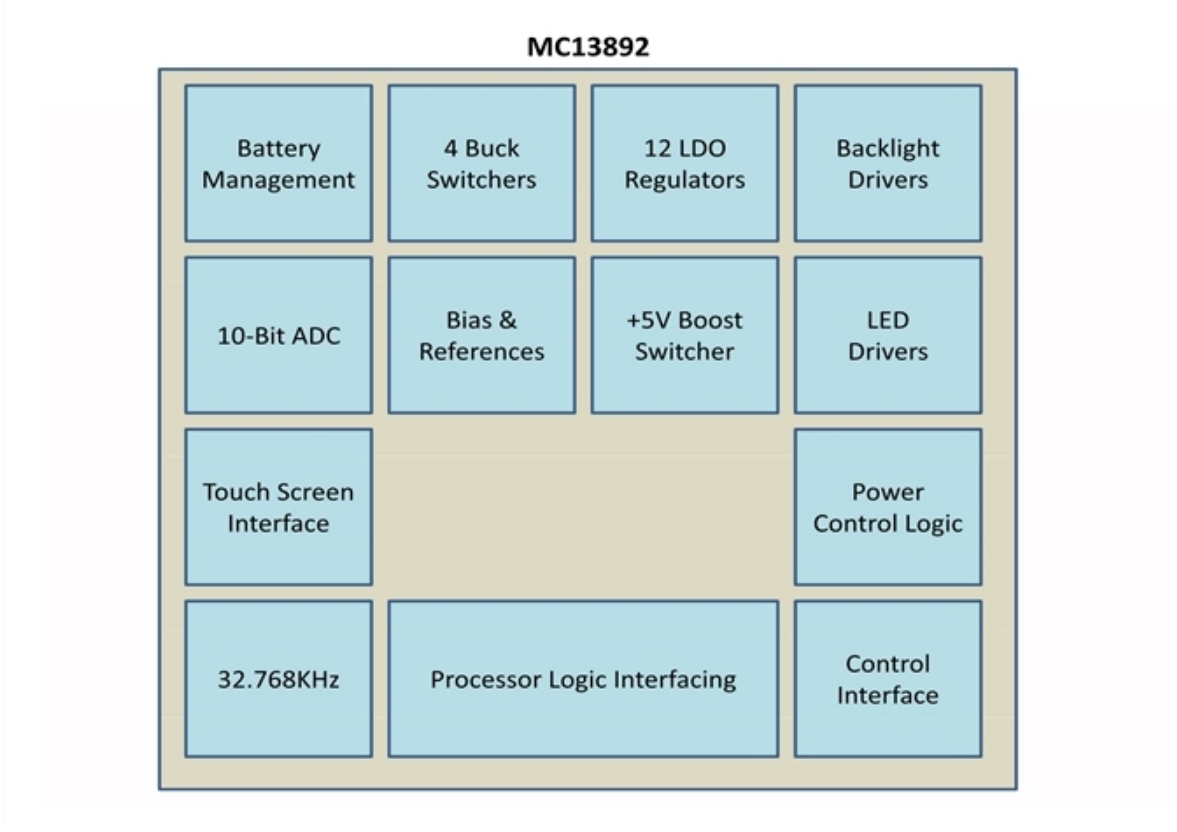
+3.15 V

This supply is used on the module to power the NAND Flash interface and the SD-card 1 interface. The maximum current provided by this supply is 350mA.

The current available to supply off-module components is 300mA.

MC13892 power management

The ConnectCore for i.MX51 module is designed with Freescale MC13892 Power Management chip. This chip provides reference and supply voltages for the i.MX51 as well as for the peripheral devices. The MC13892 has four buck switchers, one +5V boost switcher and twelve low dropout regulators as well as other user interfaces. The following figure shows the block diagram of the MC13892.



Memory

DDR2 SDRAM memory

The ConnectCore for i.MX51 module provides up to 512 MB of DDR2-400 Synchronous dynamic random access memory (SDRAM) memory.

The module can support up to four 16-bit, 128Mb, DDR2-400 chips, configured as two banks of 32-bits of 128 Mb double data rate (DDR)2-400 memory.

NAND flash memory

The ConnectCore for i.MX51 module provides 512 MB of Negated AND (NAND)-Flash memory. On the module a 512 MB, 2Kbyte page, NAND-Flash chip is used.

Options for other densities NAND Flash devices are available depending on the module variant.

Chip selects

Chip select memory map

The ConnectCore for i.MX51 has eight chip select signals, two for dynamic memory and six for static memory. The table below shows the memory map of these chip select signals.

Name	Pin	Address range	Sixe [Mb]	Usage	Comments
DRAM_ CS0#	Y4	0x9000_000-0x9FFF_ FFFF	256M	DDR2 bank 0	First bank on module
DRAM_ CS1#	Y3	0xA000_0000- 0xAFFF_FFFF	256M	DDR2 bank 1	Second bank on module
EIM_CS0	W6	0xB000_000- 0xB7FF_FFFF	128M	External CS0#	
EIM_CS1	Y6	0xB800_000- 0xBFFF_FFFF	128M	External CS1#	
EIM_CS2	Y7	0xC000_000- 0xC7FF_FFFF	128M	External CS2#	
EIM_CS3	AC3	0xC800_000- 0xCBFF_FFFF	64M	External CS3#	
EIM_CS4	AA6	0xCC00_000- 0xCDFF_FFFF	32M	External CS4#	
EIM_CS5	AA5	0xCE00_000- 0xCFFE_FFFF	32M (minus 64K)	External CS5#	Used for Ethernet Controller on module

Multiplexed GPIO

GPIO multiplexing table

The ConnectCore for i.MX51 has four GPIO banks. Each bank provides 32 bidirectional general purpose input and output signals.

The GPIO pins are multiplexed with other functions on the module. For each pin there are up to 8 muxing options (called ALT modes). By default all GPIO pins are configured to their respective GPIO signals. Since different modules require different pin settings (like pull up, keeper, etc) the i.MX51 has an IOMUX controller to configure the pin settings.

The table below shows the ALT mode for each GPIO signal, the name of the Pad and the default use on the module. For a detailed description of all the muxing options for each pin, refer to the i.MX51 Hardware Reference Manual.

WARNING! Do not connect signals marked NANDF_* to GND during boot time if you want to boot from NAND flash.

GPIO	Mode	Pad	On module default as
GPIO1_0	ALT1	GPIO1_0	HDMI Interrupt
GPIO1_1	ALT1	GPIO1_1	User Button 2
GPIO1_2	ALT0	GPIO1_2	I2C2_SCL
GPIO1_3	ALT0	GPIO1_3	I2C2_SDA
GPIO1_4	ALT0	GPIO1_4	Watchdog reset
GPIO1_5	ALT0	GPIO1_5	MC13892 Interrupt
GPIO1_6	ALT0	GPIO1_6	Accelerometer Interrupt 2
GPIO1_7	ALT0	GPIO1_7	Accelerometer Interrupt 1
GPIO1_8	ALT0	GPIO1_8	USB Power enable
GPIO1_9	ALT0	GPIO1_9	Ethernet 2 Interrupt
GPIO1_10	ALT7	DISP2_DAT11	Ethernet 1
GPIO1_11	ALT2	USBH1_DATA0	USB Host
GPIO1_12	ALT2	USBH1_DATA1	USB Host
GPIO1_13	ALT2	USBH1_DATA2	USB Host
GPIO1_14	ALT2	USBH1_DATA3	USB Host
GPIO1_15	ALT2	USBH1_DATA4	USB Host

GPIO	Mode	Pad	On module default as
GPIO1_16	ALT2	USBH1_DATA5	USB Host
GPIO1_17	ALT2	USBH1_DATA6	USB Host
GPIO1_18	ALT2	USBH1_DATA7	USB Host
GPIO1_19	ALT5	DISP2_DAT6	Ethernet 1
GPIO1_20	ALT3	UART2_RXD	UART2_RXD
GPIO1_21	ALT3	UART2_TXD	UART2_TXD
GPIO1_22	ALT3	UART3_RXD	UART3_RXD
GPIO1_23	ALT3	UART3_TXD	UART3_TXD
GPIO1_24	ALT3	OWIRE_LINE	S/PDIF Output
GPIO1_25	ALT2	USBH1_CLK	USB Host
GPIO1_26	ALT2	USBH1_DIR	USB Host
GPIO1_27	ALT2	USBH1_STP	USB Host
GPIO1_28	ALT2	USBH1_NXT	USB Host
GPIO1_29	ALT5	DISP2_DAT7	Ethernet 1
GPIO1_30	ALT5	DISP2_DAT8	Ethernet 1
GPIO1_31	ALT5	DISP2_DAT9	Ethernet 1
GPIO2_0	ALT1	EIM_D16	EIM_D16
GPIO2_1	ALT1	EIM_D17	EIM_D17
GPIO2_2	ALT1	EIM_D18	EIM_D18
GPIO2_3	ALT1	EIM_D19	EIM_D19
GPIO2_4	ALT1	EIM_D20	EIM_D20
GPIO2_5	ALT1	EIM_D21	EIM_D21
GPIO2_6	ALT1	EIM_D22	EIM_D22
GPIO2_7	ALT1	EIM_D23	EIM_D23
GPIO2_8	ALT1	EIM_D24	EIM_D24
GPIO2_9	ALT1	EIM_D27	EIM_D27
GPIO2_10	ALT1	EIM_A16	GPIO
GPIO2_11	ALT1	EIM_A17	GPIO
GPIO2_12	ALT1	EIM_A18	GPIO
GPIO2_13	ALT1	EIM_A19	GPIO

GPIO	Mode	Pad	On module default as
GPIO2_14	ALT1	EIM_A20	GPIO
GPIO2_15	ALT1	EIM_A21	GPIO
GPIO2_16	ALT1	EIM_A22	GPIO
GPIO2_17	ALT1	EIM_A23	GPIO
GPIO2_18	ALT1	EIM_A24	GPIO
GPIO2_19	ALT1	EIM_A25	GPIO
GPIO2_20	ALT1	EIM_A26	GPIO
GPIO2_21	ALT1	EIM_A27	XBEE_SLEEP_RQ
GPIO2_22	ALT1	EIM_EB2	EIM_EB2
GPIO2_23	ALT1	EIM_EB3	EIM_EB3
GPIO2_24	ALT1	EIM_OE	EIM_OE
GPIO2_25	ALT1	EIM_CS0	EIM_CS0
GPIO2_26	ALT1	EIM_CS1	GPIO
GPIO2_27	ALT1	EIM_CS2	GPIO
GPIO2_28	ALT1	EIM_CS3	GPIO
GPIO2_29	ALT1	EIM_CS4	GPIO
GPIO2_30	ALT1	EIM_CS5	Ethernet 2 Controller chip select
GPIO2_31	ALT1	EIM_DTACK	GPIO
GPIO3_0	ALT4	DI1_PIN11	LCD1 PWREN
GPIO3_1	ALT4	DI1_PIN12	LCD2 PWREN
	ALT1	EIM_LBA	GPIO
GPIO3_2	ALT4	DI1_PIN13	GPIO
	ALT1	EIM_CRE	GPIO
GPIO3_3	ALT4	DI1_D0_CS	LCD Touch Screen interrupt
	ALT3	NANDF_WE_B	NANDF_WE_B
GPIO3_4	ALT4	DI1_D1_CS	LCD1_TCH_INT/TCH_EXT#
	ALT3	NANDF_RE_B	NANDF_RE_B
GPIO3_5	ALT4	DISPB2_SER_DIN	GPIO
	ALT3	NANDF_ALE	NANDF_ALE

GPIO	Mode	Pad	On module default as
GPIO3_6	ALT4	DISPB2_SER_DIO	User Button 1 / GPIO
	ALT3	NANDF_CLE	NANDF_CLE
GPIO3_7	ALT4	DISPB2_SER_CLK	Camera 2 Reset
	ALT3	NANDF_WP_B	NANDF_WP_B
GPIO3_8	ALT4	DISPB2_SER_RS	USB Host Reset signal
	ALT3	NANDF_RB0	NANDF_RB0
GPIO3_9	ALT3	NANDF_RB1	GPIO / User LED2
GPIO3_10	ALT3	NANDF_RB2	GPIO / User LED1
GPIO3_11	ALT3	NANDF_RB3	GPIO
GPIO3_12	ALT3	CSI1_D8	Not used
	ALT0	GPIO_NAND	Card Detect input SD Card
GPIO3_13	ALT3	CSI1_D9	Camera 1 Reset
GPIO3_14	ALT3	CSI1_VSYNC	CSI1_VSYNC
GPIO3_15	ALT3	CSI1_HSYNC	CSI1_HSYNC
GPIO3_16	ALT3	NANDF_CS0	NANDF_CS0
GPIO3_17	ALT3	NANDF_CS1	SD Card write protect
GPIO3_18	ALT3	NANDF_CS2	GPIO
GPIO3_19	ALT3	NANDF_CS3	Not used
GPIO3_20	ALT3	NANDF_CS4	GPIO
GPIO3_21	ALT3	NANDF_CS5	GPIO
GPIO3_22	ALT3	NANDF_CS6	GPIO
GPIO3_23	ALT3	NANDF_CS7	SD3_CLK
GPIO3_24	ALT3	NANDF_RDY_INT	SD3_CMD#
GPIO3_25	ALT3	NANDF_D15	SD3_DATA7
GPIO3_26	ALT3	NANDF_D14	SD3_DATA6
GPIO3_27	ALT3	NANDF_D13	SD3_DATA5
GPIO3_28	ALT3	NANDF_D12	SD3_DATA4
GPIO3_29	ALT3	NANDF_D11	SD3_DATA3
GPIO3_30	ALT3	NANDF_D10	SD3_DATA2
GPIO3_31	ALT3	NANDF_D9	SD3_DATA1

GPIO	Mode	Pad	On module default as
GPIO4_0	ALT3	NANDF_D8	SD3_DATA0
GPIO4_1	ALT3	NANDF_D7	NANDF_D7
GPIO4_2	ALT3	NANDF_D6	NANDF_D6
GPIO4_3	ALT3	NANDF_D5	NANDF_D5
GPIO4_4	ALT3	NANDF_D4	NANDF_D4
GPIO4_5	ALT3	NANDF_D3	NANDF_D3
GPIO4_6	ALT3	NANDF_D0	NANDF_D0
GPIO4_7	ALT3	NANDF_D1	NANDF_D1
GPIO4_8	ALT3	NANDF_D0	NANDF_D0
GPIO4_9	ALT3	CSI2_D12	CSI2_D12
GPIO4_10	ALT3	CSI2_D13	CSI2_D13
GPIO4_11	ALT3	CSI2_D18	CSI2_D18
GPIO4_12	ALT3	CSI2_D19	CSI2_D19
GPIO4_13	ALT3	CSI2_VSYNC	CSI2_VSYNC
GPIO4_14	ALT3	CSI2_HSYNC	CSI2_HSYNC
GPIO4_15	ALT3	CSI2_PIXCLK	CSI2_PIXCLK
GPIO4_16	ALT3	I2C1_CLK	GPIO
GPIO4_17	ALT3	I2C1_DAT	GPIO
GPIO4_18	ALT3	AUD3_BB_TXD	AUD3_BB_TXD
GPIO4_19	ALT3	AUD3_BB_RXD	AUD3_BB_RXD
GPIO4_20	ALT3	AUD3_BB_CK	AUD3_BB_CK
GPIO4_21	ALT3	AUD3_BB_FS	AUD3_BB_FS
GPIO4_22	ALT3	CSPI1_MOSI	CSPI1_MOSI
GPIO4_23	ALT3	CSPI1_MISO	CSPI1_MISO
GPIO4_24	ALT3	CSPI1_SS0	CSPI1_SS0 (MC13892 Chip select)
GPIO4_25	ALT3	CSPI1_SS1	CSPI1_SS1
GPIO4_26	ALT3	CSPI1_RDY	LCD SPI chip select
GPIO4_27	ALT3	CSPI1_SCLK	CSPI1_SCLK
GPIO4_28	ALT3	UART1_RXD	UART1_RXD
GPIO4_29	ALT3	UART1_TXD	UART1_TXD

GPIO	Mode	Pad	On module default as
GPIO4_30	ALT3	UART1_RTS	UART1_RTS
GPIO4_31	ALT3	UART1_CTS	UART1_CTS

Interfaces

1-Wire

The ConnectCore for i.MX51 provides a 1-Wire communication interface. The module sends or receives one bit at a time. The required protocol for accessing the generic 1-Wire device is defined by Maxim.

The main features of the 1-Wire interface are the following:

- Performs the 1-Wire bus protocol to communicate with an external 1-Wire device
- Provides a clock divider to generate a 1-Wire bus reference clock

Accelerometer

The module provides a three axis digital output accelerometer. This device is connected to the i.MX51 through the I^2C bus. The I^2C device address of the accelerometer is the following:

Interface	I2C Address (7 bits)
Accelerometer (MMA7455L)	0 x 1D

The main features of the accelerometer device are the following:

- User assigned registers for offset calibration
- Programmable threshold interrupt output
- Level detection for motion recognition (shock, vibration, freefall)
- Pulse detection for single or double pulse recognition
- Selectable sensitivity (±2g, ±4g, ±8g) for 8-bit mode

ADC and touch screen

The module provides an eight channel 10-bit ADC. The ADC/Touch interface is integrated in the MC13892 power management device. You can use this ADC as a standard ADC or as a touch screen interface.

The ADC runs at approximately 2MHz, and it has an auto calibration circuit which reduces the offset and gain errors.

The main features of the ADC are the following:

- Resolution: 10-bit
- Differential linearity error: 1 LSB
- Integral linearity error: 3 LSB
- Conversion time per channel: 10 us
- Low power consumption (1 mA of conversion current)

- Analog input range: 0 ~ 2.4V
- Five channels pre-assigned to battery interface measurements
- Internal voltage scaling for pre-assigned measurements
- Normal conversion mode and touch screen mode
- The following table shows the ADC channel assignment in ADC and touch screen modes:

Channel	ADC Mode	Touch Screen Mode	Touch Screen Inactive Mode
0	Battery Voltage	Touch_X1	-
1	Battery Current	Touch_X2	-
2	Application voltage (VBP)	-	-
3	Charger Voltage	Touch_Y1	-
4	Charger Current	Touch_Y2	General Purpose via TOUCH_X1
5	Battery Temperature Monitoring	-	General Purpose via TOUCH_X2
6	General Purpose ADIN6	Contact resistance	General Purpose via TOUCH_Y1
7	General Purpose ADIN7	Contact resistance	General Purpose via TOUCH_Y2

The ADC Mode, Touch Screen Mode and Touch Screen Inactive Mode are selected using the ADSEL, TSMOD0, TSMOD1 and TSMOD2 bits in the Freescale MC13892 Power Management chip.

Channel 5 in ADC mode connects via ADIN5 but this is typically where a Thermistor is used to monitor the battery pack temperature. When battery temperature monitoring is not required, this input can be used as a general purpose ADC input but with the following considerations:

1. The power-up default state is for temperature monitoring via the Thermistor. The IMX51 module contains a resistor divider to apply the right bias to the ADIN5 pin to allow the unit to boot correctly (without requiring a Thermistor to be fitted). The software will first need to disable this function after which the analogue input may be connected to ADIN5. Once this is disabled, the real analogue input may be connected via this pin.
2. The presence of the resistor divider appears like a 5kΩ load, it follows that the tri-state buffer used to drive this input will need to have an output impedance of less than 5Ω if the 10-bit resolution is not to be compromised. An alternative approach is to disable the GPO1 pin of the MC13892 in software and use that pin as the input. In that case the input impedance will look like 20kΩ to GND. Therefore the tri-state buffer output impedance now needs to be 20Ω or lower. However this way results in the real input voltage being divided by 2 on the ADC input. When using GPO1 as the input, do not connect anything to ADIN5.

Channel 6 in ADC mode may also monitor the Coin-cell input voltage.

Channel 7 in ADC mode may also monitor the Die Temperature. Please note the UID voltage cannot be read nor is alternative input ADIN7B available.

It is possible to support 7 ADC channels by alternating between the ADC mode and Touch Screen Inactive mode.

For more information refer to the datasheet of the Freescale MC13892 Power Management chip.

Synchronous Serial Interface (SSI)

The ConnectCore for i.MX51 module provides up to three synchronous serial interfaces (SSI) that allows communicating with a variety of serial devices as standard CODECs, audio CODECs implementing the I^2S standard and Intel AC97 standard.

SSI is typically used to transfer samples in a periodic manner. The SSI consists of independent transmitter and receiver sections with independent clock generation and frame synchronization.

The main features of the SSI interface are the following:

- Independent (asynchronous) or shared (synchronous) transmit and receive sections operating in Master or Slave mode
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with as many as 32 time slots
- Two sets of four 15 x 32 bits Transmit and Receive FIFOs.
- Programmable data interface mode such like I^2S, LSB, MSB aligned
- Programmable word length 8, 10, 12, 16, 18, 20, 22 or 24 bits
- Program options for frame sync and clock generation
- Programmable I^2S modes (Master, Slave or Normal)
- AC97 support

External Memory Interface (EMI)

The module provides access to the external memory controller. This memory controller handles the interface to devices external to the chip, including generation of chip selects, clock and control for external peripherals and memory. It provides asynchronous access to devices with SRAM-like interface and synchronous access to devices with NOR Flash like or PSRAM like interfaces.

The following lines of the memory controller are available on the module connectors:

- Support for multiplexed address/data bus operations
  - 16-bit data/28-bit address in non-multiplexed address/data mode
  - 16-bit or 32-bit data/28-bit address in multiplexed address/data mode
- Programmable data port size of each chip select
- 28-bit address bus
- Up to 5 chip selects
- Read and write control lines
- 2 x byte enable signals
- Register/command selection line (CRE)

Note 8-bit devices are supported by the EMI connecting to only one of the following three locations:

- EIM_DA[7:0] pads
- EIM_DA[15:8] pads
- EIM_DA[31:24] pads

Connection to the EIM_D[23:16] pads is not supported.

Ethernet 1

The ConnectCore for i.MX51 provides a Fast Ethernet Controller (FEC) designed to support both 10 and 100 Mb/s Ethernet/IEEE 802.3 networks. A low power consumption 10/100 Ethernet transceiver (LAN8710A) from SMSC is used on the module to complete the interface to the media.

The module does not provide a transformer and Ethernet connector.

The PHY address on the MII bus is 0x7 (0b00111).

The module also provides two status signals for activity and link LEDs.

Ethernet 2

The ConnectCore for i.MX51 module can provide a high-performance 10/100Mb Ethernet controller (LAN9221) with integrated MAC and PHY from SMSC as a second Ethernet port.

The main features of this Ethernet controller are the following:

- Embedded 16 Kbyte FIFO for packet buffers
- Support burst-mode read for highest performance applications
- Configurable interrupt pin with programmable hold-off timer
- Compatible with IEEE 802.3, 802.3u standards
- Integrate Fast Ethernet MAC/PHY transceiver in one chip
- 10Mb/s and 100Mb/s data rate
- Full and half duplex operations
- 10/100Mb/s Auto-negotiation operation
- Twisted pair crossover detection and auto-correction (HP Auto-MDIX)
- IEEE 802.3x flow control for full-duplex operation
- Wake-on-LAN capabilities
- LED pins for various network activity indications

The Ethernet controller is connected to CS5#. Its programmable polarity interrupt output is connected to the signal GPIO1_9.

The module does not have a transformer and Ethernet connector.

The module provides two status signals for activity and link LEDs.

I2C

The module provides two I2C interfaces. The I2C interfaces operate up to 400Kbps, depending on pad loading and timing. The I2C system is a true multiple master bus including arbitration and collision detection.

The I2C port 2 interface is available on the development board (header P22). Two 2K2 pull-up resistors are provided on the module.

The I2C port 1 interface is available through the main module connectors (J1 and J2) as well as on the corresponding signal rail connectors (J25 and J26), multiplexed with other interface functionality. The development board does not provide a dedicated header for access to I2C port 1.

The I2C port 1 signals are available through the main module connectors as outlined below:

- I2C1_SDA:
  - J1.141 - EIM_D16 (used on the module for external Ethernet controller, if present)
  - J2.111 - SPI1_MOSI (used on the module as communication channel for Freescale PMIC)
  - J2.86 - SD2_CLK (used on the module as communication channel for Wireless LAN interface, if present)
- I2C1_SCL:
  - J1.144 - EIM_D19 (used on the module for external Ethernet controller, if present)
  - J2.115 - SPI1_SCLK (used on the module as communication channel with Freescale PMIC)
  - J2.88 - SD2_CMD (used on the module as communication channel for Wireless LAN interface, if present)

The I2C interface provides the following capabilities:

- Compatibility with I2C bus standard
- Multiple-master operation
- Software programmable for one of 64 different serial clock frequencies
- Software selectable acknowledge bit
- Start and stop signal generation detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

Video subsystem

The i.MX51 processor has a video subsystem that includes the following modules:

- Video Processing Unit (VPU): a multi-standard video encoder/decoder
- Image Processing Unit (IPU): providing connectivity to displays, related processing, synchronization and control
- TV encoder (TVE) bride: providing optional translation from the digital display interface supported by the IPU to SDTV analog and some HDTV interfaces

Video Processing Unit (VPU)

The video processing unit of the i.MX51 is a high performance, multistandard video processing unit that can perform H.264 BP/MP/HP, VC-1 SP/MP/AP, MPEG4 SP/ASP, Divx, RV8/9, and MPEG2 MP decoding up to 1920 × 1088 resolution. It supports multiple video codecs simultaneously.

The detailed features of the VPU are as follows:

- Multi-standard video codec
  - H.264/AVC decoder for baseline profile, main profile and high profile
  - VC-1 decoder for simple profile, main profile and advanced profile
  - MPEG-4 decoder for simple profile, advanced simple profile except GMC
  - H.263 decoder for baseline profile

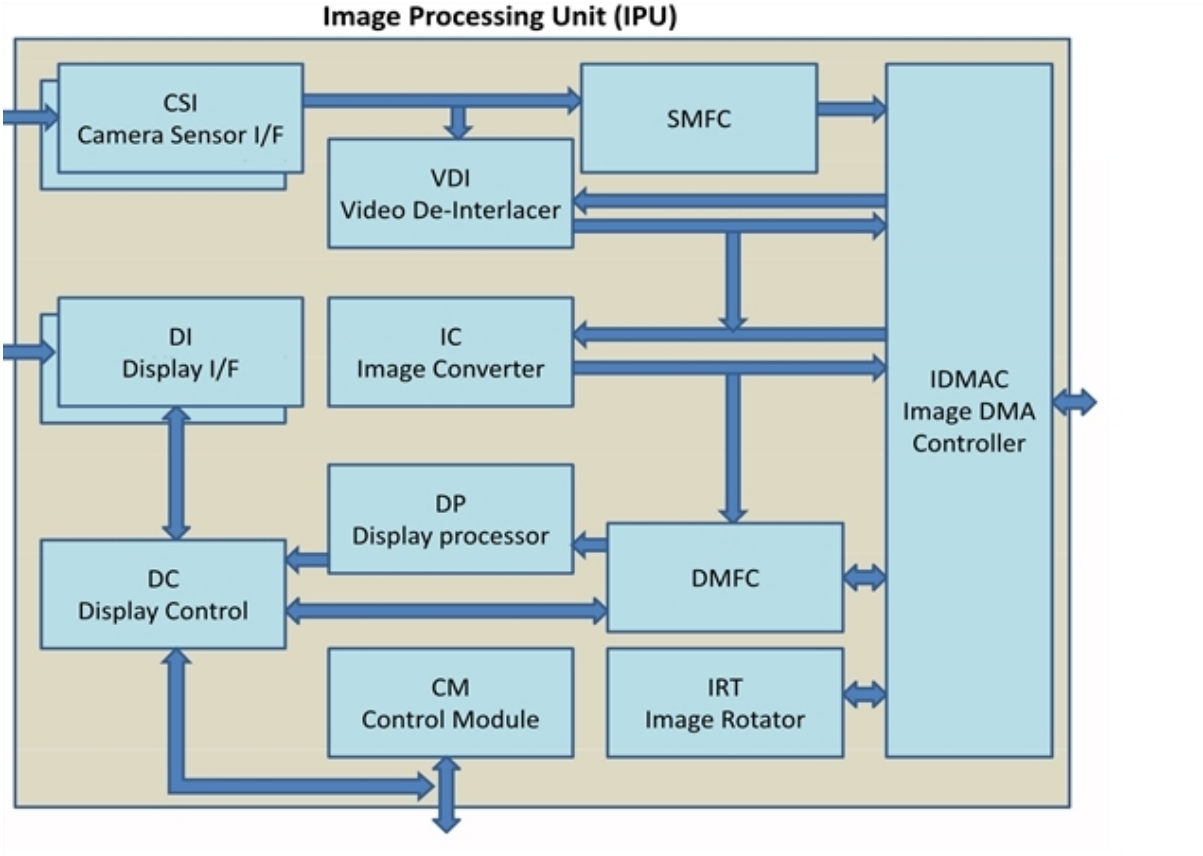
- Divx Home Theater decoder for profile (version 3.x, 4.x, 5.x, 6.x) and Xvid
- MPEG-2 decoder for main profile @ high level
- RV decoder for profile 8/9/10
- H.264/AVC encoder for baseline profile
- MPEG-4 encoder for simple profile
- H.263 encoder for baseline profile
- MJPEG encoder for baseline profile
- Multiple codec: supports up to 4 decoding/encoding processes simultaneously, each process can have a different format

- Other features
  - Supports rotating and mirroring simultaneously.
  - Built-in de-ringing filter
  - Built-in de-blocking filter for MPEG-2/MPEG-4/Divx
  - Simultaneous multi-stream and multi-standard processing capability
  - Robust error detection

Image Processing Unit (IPU)

- Connect relevant devices - cameras, displays, graphics accelerators, TV encoders and decoders
- Related image processing and manipulation: sensor image signal processing, display processing, image conversions, and so forth.
- Synchronization and control capabilities (for example, to avoid tearing artifacts)

The following figure shows the simplified block diagram of the IPU:



The image processing unit has the following blocks:

- Camera Sensor Interface - CSI
  - Controls a camera port; provides interface to an image sensor or a related device. The ConnectCore for i.MX51 has two camera blocks.
- Display Interface - DI
  - Provides interface to displays, display controllers and related devices. The ConnectCore for i.MX51 has two camera blocks.
- Display Controller - DC
  - Controls the display ports
- Display Processor - DP
  - Performs the processing required for data sent to display
- Image Converter - IC
  - Performs resizing, color conversion/correction, combining with graphics, and horizontal inversion
- Video De Interlacer - VDI
  - Performs video de interlacing (interlaced -> progressive)
- Image Rotator - IRT
  - Performs rotation (90 or 180 degrees) and inversion (vertical/horizontal)

- Image DMA Controller - IDMAC
  - Controls the memory port; transfers data to/from system memory
- Sensor Multi FIFO Controller - SMFC
  - Controls FIFOs for output from the CSIs to system memory
- Display Multi FIFO Controller - DMFC
  - Controls FIFOs for IDMAC channels related to the display system
- Control Module - CM
  - Provides control and synchronization

Keypad

The module provides a keypad port that can be used as a keypad matrix interface or as general purpose input/output.

The Keypad port is designed to interface with the keypad matrix with 2-point contact or 3-point contact keys. The Keypad port is designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the Keypad port is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously on the keypad.

- Supports up to an 6 × 4 external keypad matrix
- Port pins can be used as general purpose I/O
- Open drain design
- Glitch suppression circuit design
- Multiple-key detection
- Long key-press detection
- Standby key-press detection
- Synchronizer chain clear
- Supports a 2-point and 3-point contact key matrix

Memory cards

The ConnectCore for i.MX51 module provides up to four MMC/SD/SDIO interfaces.

- MultiMediaCard (MMC)

  This is a universal low-cost data storage and communication media that is designed to cover a wide area of applications including mobile video and gaming, WLAN or other wireless networks. Old MMC cards are based on 7-pin serial bus with a single data pin, while the newer high-speed MMC communication is based on an advanced 11-pin serial bus designed to operate at lower voltage.

- Secure Digital (SD) card

  This is an evolution of earlier MMC technology. It is specifically designed to meet the security, capacity, performance, and environment requirements inherent in newly emerging audio and video consumer electronic devices. The physical form factor, pin assignment and data transfer protocol are forward compatible with MMC, with some additions. Under the SD protocol, an SD card can be categorized as memory card, I/O card, or combo card (having both memory and I/O functions).

The main features of the Memory Card interfaces are the following:

- Designed to work with MMC, MMC plus, MMC RS, SD memory, miniSD memory, SDIO, and SD Combo. Compatible with the following specifications:
  - MMC System Specification Version 4.2
  - SD Host Controller Standard Specification Version 2.0
  - SD Memory Card Specification Version 2.0: supports High-Capacity SD Memory Cards
  - SDIO Card Specification Version 2.0
- Supports 1, 4, or 8 bit MMC modes and 1bit or 4 bit SD and SDIO modes
  - Card bus clock frequency up to 52 MHz
  - Up to 416 Mb/s of data transfer for MMC cards in 8-bit mode
  - Up to 200 Mb/s of data transfer for SD/SDIO cards in 4-bit mode
  - Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt period

The following table shows the memory card signals available on the module connectors:

Signal	Memory Card 1	Memory Card 2	Memory Card 3	Memory Card 4
Card Detect (CD #)	√			√
CLK	√	√	√	√
CMD	√	√	√	
LCTL				√
WP#	√			√
DATA3 - DATA0	√	√	√	√
DATA7 - DATA4	√		√	√

PWM

The ConnectCore for i.MX51 module provides two PWM interfaces. These PWM interfaces share the output pad in the i.MX51 CPU with the I^2C bus used on the module for the accelerometer. In order to use the PWM signals the I^2C bus must be disabled.

The main features of the PWM interface are the following:

- 16-bit up-counter with clock source selection
- 4 × 16 FIFO to minimize interrupt overhead

- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low power and debug modes
- Interrupts at compare and rollover

RTC

The ConnectCore for i.MX51 provides a Real Time Clock and a Secure Real Time clock.

The real time clock function is provided including time and day counters as well as an alarm function. The RTC utilizes the 32.768KHz crystal oscillator for the time base and is powered by the coin cell backup supply when main supply has dropped below operational range. In configurations where the SRTC is used, the RTC can be disabled to conserve current drain. The accuracy of the 32.768KHz crystal used for the Real-Time Clock is ±20ppm.

- RTC accuracy ±20ppm
- 17-bit time of day counter
- 15-bit day counter
- Time of day alarm
- Day alarm

The secure real time clock helps to comply with issues arising out of different applications requiring secure and certifiable time, for example Digital Rights Management (DRM) schemes.

The main features of the secure RTC interface are the following:

- Secure 47-bit time counter
- Non-secure 47-bit time counter
- Use-mode protection. The SRTC cannot be configured by non-secured SW.
- Re-programming protection. The SRTC cannot be altered or disabled after SRTC locked.
- Clock source protection
- Programmable secure and non-secure alarms with interrupt

SPDIF

The ConnectCore for i.MX51 has a Sony/Philips Digital Interface Transmitter (SPDIF Tx) audio module that allows the processor to transmit digital audio over it.

For the SPDIF transmitter, the processor provides the audio data. Zero is always inserted in the user data. The SPDIF transmitter generates a SPDIF output bitstream in the biphase mark format (IEC958), which consists of audio data, channel status, and user data. In the SPDIF transmitter, the IEC958 biphase bit stream is generated on both edges of the SPDIF transmit clock.

- IEC 60958 format SPIDF output
- 7 transmit clock source
- Consumer channel status support
- Support for interrupt and DMA

SPI

The module provides up to three SPI interfaces that can be configured in either master or slave mode. Two of the SPI interfaces contain one 64 x 32 receive buffer (RXFIFO) and one 64 x 32 transmit buffer (TXFIFO). The other SPI interface contains one 8 x 32 receive buffer and one 8 x 32 transmit buffer.

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Two SPI interfaces support SPI clocks up to 66MHz in both Master and Slave mode
- One SPI interface supports SPI clocks up to 16.5MHz in both Master and Slave mode
- Up to four chip selects (two chip select for SPI1) to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- Polarity and phase of the chip select (SS#) and SPI Clock (SCLK) are configurable
- Data ready output signal for fast data communication with fewer software interrupts
- DMA support

Watchdog timer

The watchdog timer module protects against system failures by providing a method of escaping from unexpected events or programming errors. Once the watchdog module is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the watchdog timer module asserts the internal system reset signal.

- A time-out counter with time-out periods from 0.5 to 128 seconds
- Time resolution of 0.5 seconds
- Configurable time-out counter that can be programmed to run or stop during low-power and debug modes
- Programmable interrupt generation prior to time-out
- Programmable time duration between interrupt and timeout events, from 0 to 128 seconds in steps of 0.5 seconds
- Power down counter enabled out of any reset by default

UART

The module provides up to three UART ports. The UART 1 is a full-modem UART port with all the handshake signals available. The UART 2 and UART 3 ports are 4-wire UART ports with data lines RXD/TXD and the handshake lines RTS#/CTS#.

The main features of these UART ports are the following:

- 7 or 8 data bits
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for RTS# and CTS# signals (signals direction according to DEC mode)
- Interrupt-based or DMA-based mode

- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbps)
- Auto baud rate detection (up to 115.2 Kbps)
- Programmable baud rate (up to 4Mb/s)
- Two independent 32-byte FIFOs for receive and transmit

USB Host and USB OTG

The ConnectCore for i.MX51 provides three USB Host interfaces and one USB On-The-Go (OTG) interface. These interfaces conform to the USB 2.0 specification, the OTG supplement, and the ULPI specification.

In addition to the normal USB functionality, the module also supports direct connections to on-board USB peripherals using serial or ULPI protocol. It also has serial/ULPI bypass mode connection and support for multiple interface types of ULPI and serial transceivers.

Main features of the USB Host interfaces:

- High-speed/full-speed/low-speed host
- HS/FS ULPI compliant interface
- Software configurable for full-speed/low-speed interface for serial transceivers
- Full-speed transceiverless link logic (FS-TLL) for on board connection to a FS/LS USB peripheral
- High-speed ULPI transceiverless link logic (HS-TLL) for onboard connection to a high- speed ULPI interface USB peripheral

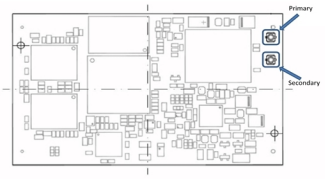
Main features of the USB OTG interface:

- High-speed OTG
- HS/FS ULPI compliant interface
- Software configurable for ULPI or serial transceiver interface
- High-speed (with ULPI transceiver), full-speed, and low-speed operation in host mode
- High-speed (with ULPI transceiver), and full-speed operation in peripheral mode
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional endpoints

WLAN

In addition to the on-module Ethernet interface, the ConnectCore for i.MX51 module can also provide an optional 802.11a/b/g/n WLAN interface with data rates up to 54 Mb/s on the a/b/g band and up to 65 Mb/s on the n band.

Two U.FL antenna connectors are provided on the module.



On the ConnectCore Wi-i.MX51 module variant, attach the antennas with the U.FL-RP-SMA female cable to the primary connector and secondary connector on the module.

Note When disconnecting U.FL connectors, we strongly recommend the use of a U.FL plug extraction tool (Hirose P/N U.FL-LP-N-2 or U.FL-LP(V)-N-2) to avoid damage to the U.FL connectors on the module.

To mate U.FL connectors, you must align the mating axes of both connectors. The “click” will confirm mated connection. Do not attempt insertion at an extreme angle.

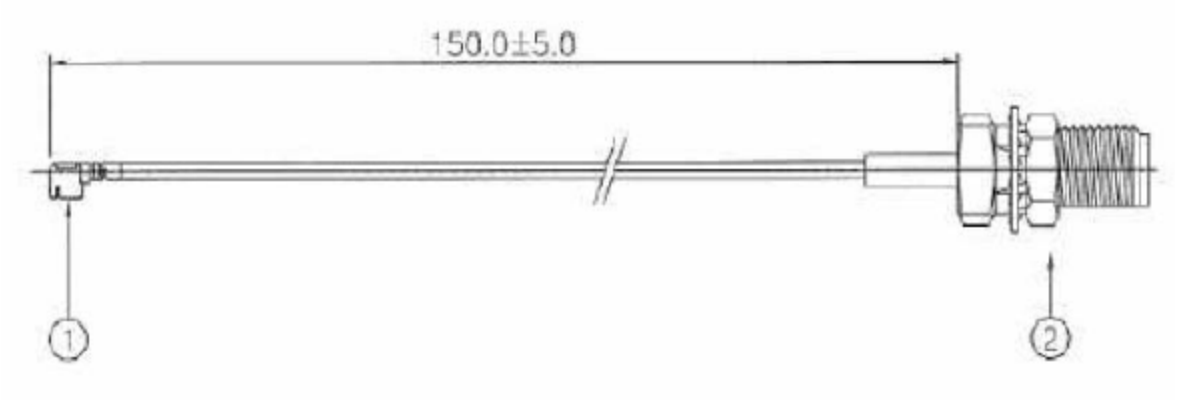
Cable specification: U.FL/W.FL to RP-SMA

Attributes

Attribute	Property
Impedance	50 Ohm
Frequency Range	0 to 6 GHz
Length	150 mm
Temperature Range	-40° to +90° C
Loss	3.8dB/m (3 GHz) 5.6dB/m (6 GHz)

Dimensions

Note Dimensions are provided for reference purposes only. The actual antenna might vary.



1 = U.FL

2 = RP-SMA

Note This module obtained its complete certification by using the cable described here. End users in North America should use a cable that matches these specifications to maintain the module’s certification.

About the development board

The development board supports the ConnectCore for i.MX51 module. This section describes the interfaces of the development board and explains how to configure the board for your requirements.

The development board has two 180-pin connectors that mate with the module connectors.

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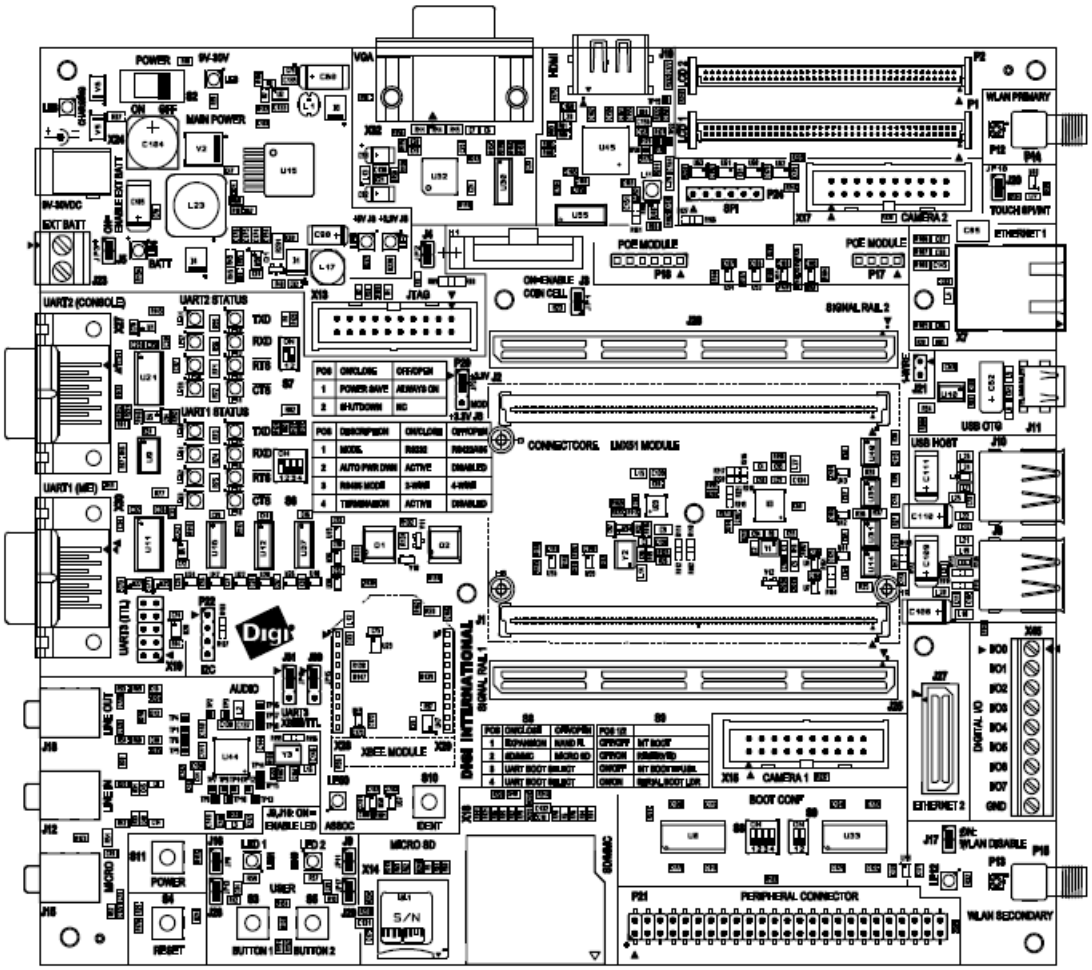
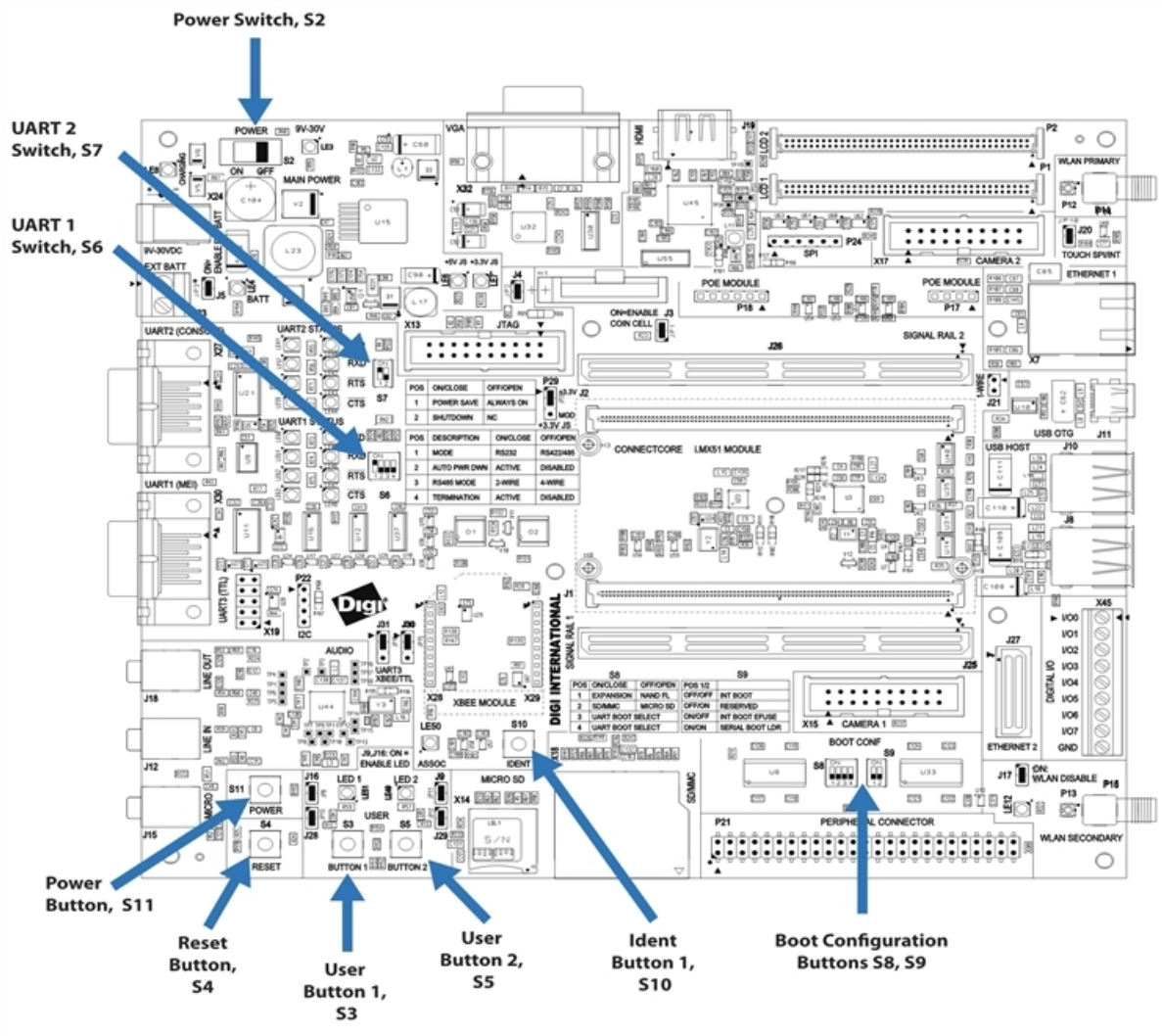


Switches and push-buttons



Power switch, S2

The development board has an ON/OFF switch, S2. The power switch S2 can switch both 9V-30VDC input power supply and 12VDC coming out of the optional PoE module. However, if a power plug is connected to the DC power jack, the PoE is disabled.

Reset button, S4

The reset push-button S4, resets the module and the peripherals on the development board. A push-button allows manual reset by connecting POR# or optionally RSTIN# to ground.

Power button, S11

The power button S11, generates a Turn On/Turn Off interrupt to the MC13892 power management device on the module.

The Turn Off event does not directly power off the module. The module is powered off by the processor's response to this interrupt. The software can configure a user initiated power down, or a transition to a low power off mode by pressing this power button.

When in Off mode or in low power mode, the module can be powered via the Turn On event generated by pressing the Power button.

User buttons, S3 and S5

Use the user push-buttons to interact with the applications running on the ConnectCore for i.MX51 module. Use these module signals to implement the push-buttons:

Signal name	Button	GPIO used
DISPB2_SER_DIO/GPIO3_6/USER_KEY1	S3	GPIO3_8
GPIO1_1/SD1_WP#/SPI_MISO/USER_KEY2	S5	GPIO1_1

GPIO3_6 is used in User Button S3 and also in the Digital I/O connector for Digital I/O7.

Ident button, S10

The Ident push-button S10 is associated to the commissioning input of the Digi XBee modules. This input provides a variety of simple functions to aid in deploying devices in a network. For a deeply description of this functionality please refer to the Digi XBee modules documentation.

Legend for multi-position switches

Switches S6, S7, S8 and S9 are multi-pin switches. In the description tables for these switches, the position is designated as *S[switch number].[pin number].* For example, position 1 on switch S6 is specified as S6.1.

UART 1 switch, S6

Use S6 to configure the line interface for serial port 1 MEI:

Switch Pin	Function	Comments
S6.1	On = RS232 transceiver enabled RS4xx transceiver disabled Off = RS232 transceiver disabled RS4xx transceiver enabled	

Switch Pin	Function	Comments
S6.2	On = Auto Power Down enabled Off = Auto Power Down disabled	Auto Power Down is not supported on this board. This signal is only accessible to permit the user to completely disable the MEI interface for using the signals for other purposes. To disable the MEI interface, go into RS232 mode (S6.1 = ON) and activate the Auto Power Down feature (S6.2 = ON) - be sure that no cable is connected to connector X30.
S6.3	On = 2-wire interface (RS4xx) Off = 4-wire interface (RS422)	
S6.4	On = Termination ON Off = No termination	

UART 2 switch, S7

Use S7 to configure the line interface for serial port 2 (console):

Switch Pin	Function	Comments
S7.1	On = Power save Off = Normal Operation	If there is a valid RS232 signal at receiver inputs the UART will be in normal operation mode. If there is not a valid RS232 signal at receiver inputs the UART will be in shutdown mode.
S7.2	On = Shutdown Off = Normal Operation	Shutdown is the highest priority functionality. If switch S7.2 = ON, the UART 2 will be in shutdown mode independently of the position of S7.1.

Boot configuration switches, S8 and S9

Use S8 to configure the source of the boot code when S9 is configures in internal boot, or to configure the source of the serial download when S9 is configured in serial downloader.

SwitchPin	Function	Comments
S8.1	On = Boot from expansion device Off = Boot from NAND Flash	Applies only if switch S9 is configured in internal boot mode

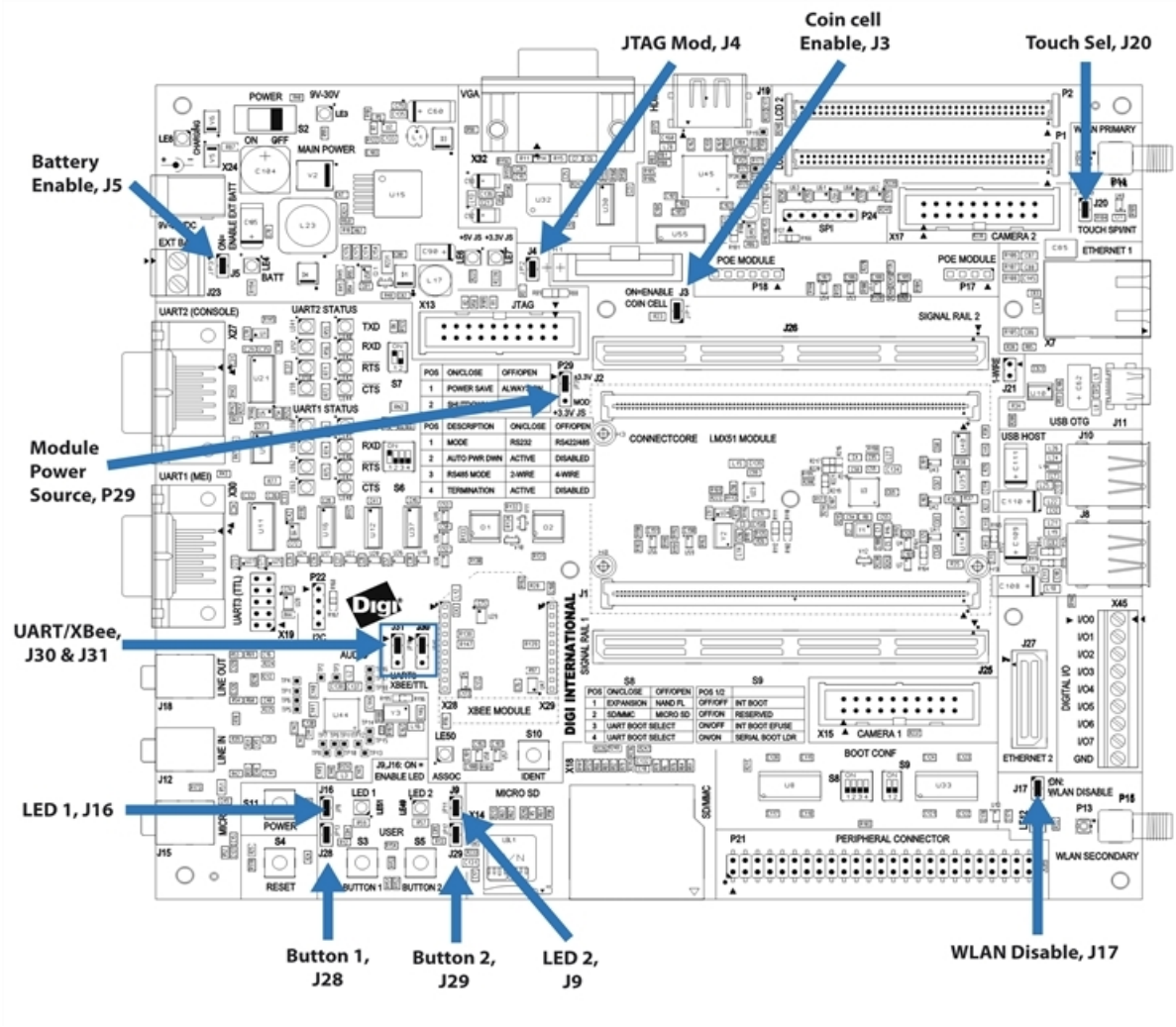
SwitchPin	Function	Comments
S8.2	On = Reserved Off = Boot from microSD™	Applies only if switch S9 is configured in internal boot mode and S8.1 is configured to boot from expansion device
S8.3 / S8.4	On / On = UART1 (MEI)	If S9 is configured in serial boot loader
S8.3 / S8.4	On / Off = UART2 (Console)	If S9 is configured in serial boot loader
S8.3 / S8.4	Off / On = UART3 (TTL)	If S9 is configured in serial boot loader
S8.3 / S8.4	Off / Off = Reserved	If S9 is configured in serial boot loader

Use S9 to configure the module boot mode:

Switch Pin	Function	Comments
S9.1 / S9.2	Off / Off	Internal Boot configured by switch S8
S9.1 / S9.2	Off / On	Reserved
S9.1 / S9.2	On / Off	Internal Boot configured by fuse block
S9.1 / S9.2	On / On	Serial downloader

For a detailed description of the ConnectCore for i.MX51 boot mode functionality, refer to the *Freescale i.MX51 Processor Hardware Reference Manual*.

Jumpers



Battery enable, J5

When J5 is set, the development board can be powered by an external battery connected to J23.

Module power source, P29

When set on positions 1-2, the 3.3V supply of the development board is generated on the +3.3V power regulator (U50).

When set on positions 2-3, the +3.3V supply of the development board is generated on the module.

LED 1, J16

When set, enables the User LED 1 (LE51) to show the status of this signal (on if low).

LED 2, J9

When set, enables the User LED 2 (LE49) to show the status of this signal (on if low).

Button 1, J28

When set, enables the User Button 1 (S3).

Button 2, J29

When set, enables the User Button 2 (S5).

UART3 / XBee selection, J30 and J31

The UART 3 port is shared on the development board between the XBee module socket and the UART 3 connector (X19).

When J30 and J31 are set to positions 1-2, the XBee module socket can be used.

When J30 and J31 are set to positions 2-3, the UART 3 on the connector (X19) can be used.

WLAN disable, J17

When set, this jumper disables the WLAN interface on the module.

Touch selection, J20

When set, an external SPI touch screen controller is configured for the LCD 1 interface and the internal analog touch screen controller (on module) is configured for the LCD 2 interface.

When removed, an internal touch screen controller is configured for the LCD 2 interface, and the internal analog touch screen controller (on module) is configured for the LCD 1 interface.

Coincell enable, J3

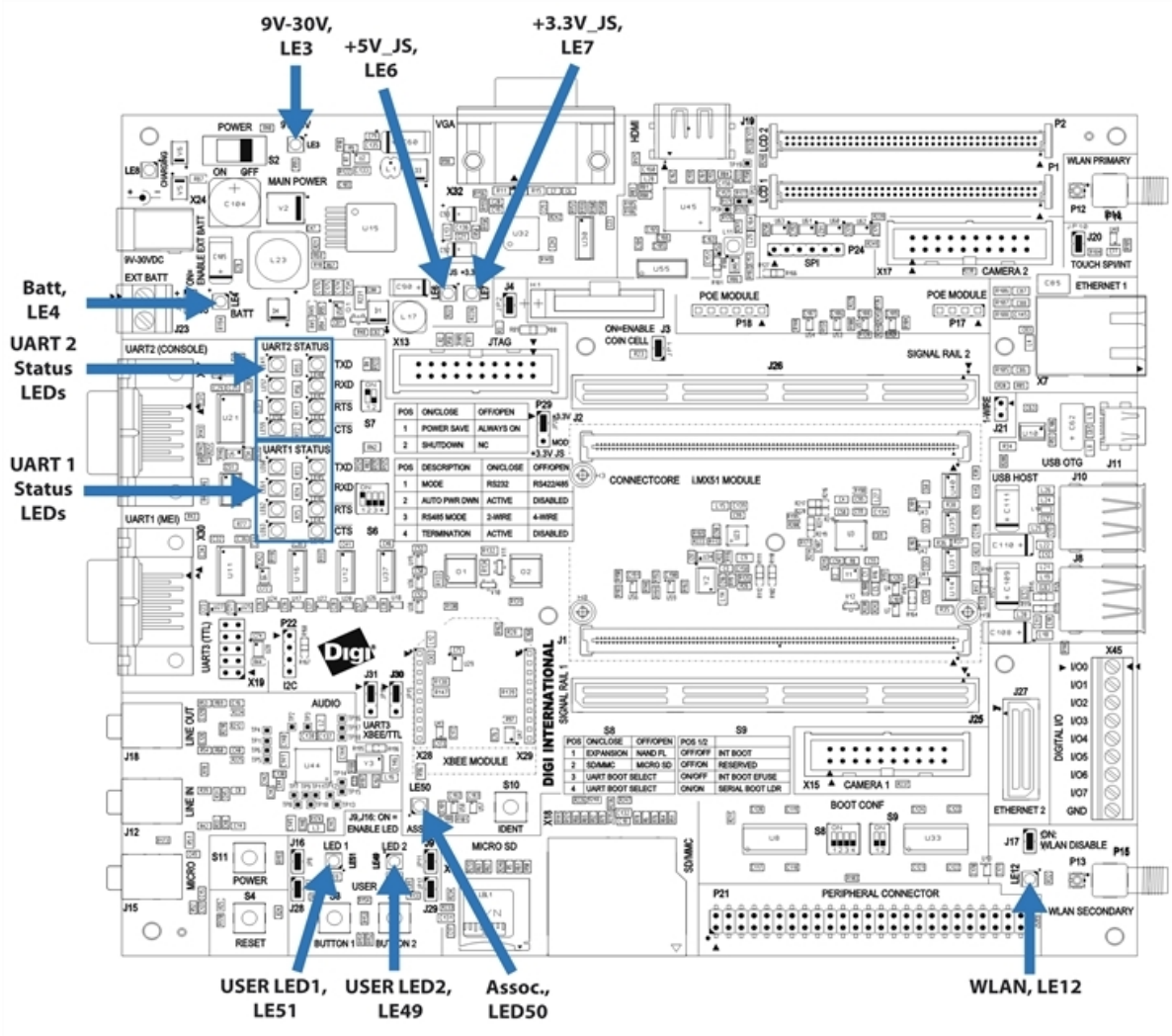
When set, this jumper supplies the real time clock with +3V from the lithium coin cell battery, even if the board is switched off.

JTAG mod., J4

When set, this jumper disables the JTAG interface for the ConnectCore for i.MX51.

When removed, the JTAG interface is enabled.

LEDs



WLAN, LE12

LED indicating WLAN operational status.

Power LEDs, LE3, LE4, LE6 and LE7

All power LEDs are red. The power supplies must be present:

- LE3 ON indicates that +9VDC / +30VDC power is present
- LE4 ON indicates that battery power is present
- LE6 ON indicates that +5VDC power for the development board is present
- LE7 ON indicates that +3.3VDC power for the development board is present

User LEDs, LE49 and LE51

The user LEDs are controlled through applications running on the ConnectCore for i.MX51 module. You may use these module signals to implement the LEDs:

Signal Name	LED	GPIO Used
NANDF_RB2/MII_COL/SP12_SCLK/GPIO3_10	LE51	GPIO3_10
NANDF_RB1/PATA_IORDY/SPI2_RDY/GPIO3_9	LE49	GPIO3_9

Serial status LEDs

The development board has two sets of serial port LEDs - four for serial port 1 and four for serial port 2. The LEDs are connected to the TTL side of the RS232 or RS4xx transceivers.

- Green means corresponding signal high
- Red means corresponding signal low
- The intensity and color of the LED will change when the voltage is switching

UART 1 status LEDs

LED Reference		Function
RED	GREEN	
LE60	LE45	TXD
LE61	LE46	RXD#
LE62	LE47	RTS#
LE63	LE48	CTS#

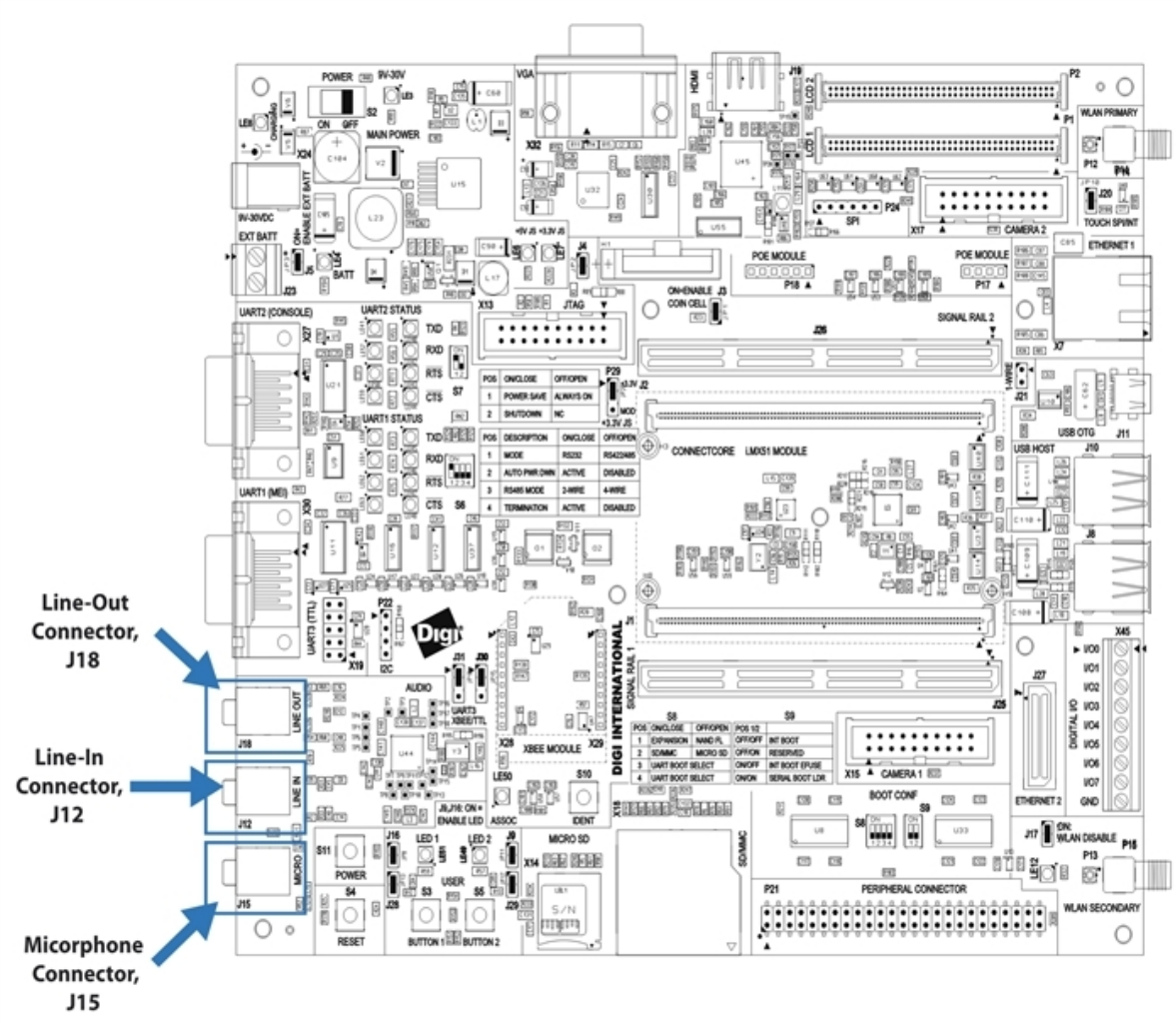
UART 2 status LEDs

LED Reference		Function
RED	GREEN	
LE41	LE40	TXD
LE57	LE42	RXD
LE58	LE43	RTS#
LE59	LE44	CTS#

XBee Associate, LE50

This LED is connected to the Associate output of the Digi XBee module. This LED provides information of the device's network status and diagnostics information. For a more in-depth description of this LED, refer to the Digi XBee modules documentation available at www.digi.com.

Audio interface



The development board provides an audio interface with a line input channel, a line-output channel and a microphone input. A Wolfson WM8753L audio CODEC is used in the development board. This audio CODEC is controlled through the I2C port 2 of the ConnectCore for i.MX51. Digital audio data is sent/received between the audio CODEC and the ConnectCore for i.MX51 through an I^2S interface (AUD3 channel of the i.MX51 AUDMUX).

The I2C device address of the audio CODEC is the following:

Interface	I^2C Address (7 bits)
Audio CODEC (WM8753L)	0 x 1A

Three stereo audio jacks are provided on the development board:

- J18 connector for LINE+OUT
- J12 connector for LINE+IN
- J15 connector for microphone

Line-out connector pinout, J18

Pin	Signal
1	GND
2	LINE-OUT-RIGHT
3	LINE-OUT-LEFT
4	HEADPHONE-DETECT
5	-

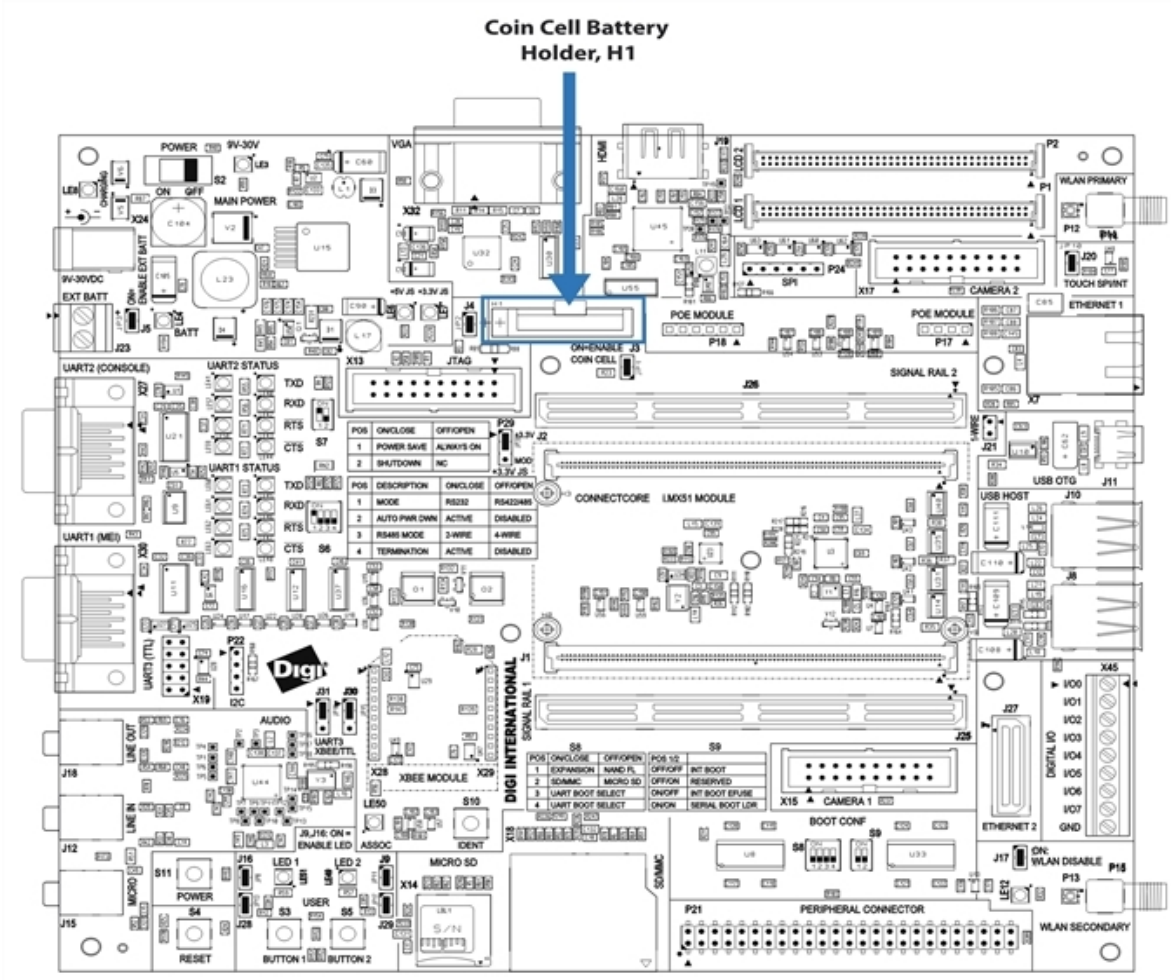
Line-in connector pinout, J12

Pin	Signal
1	GND
2	LINE-IN-RIGHT
3	LINE-IN-LEFT
4	GND
5	GND

Microphone connector pinout, J15

Pin	Signal
1	GND
2	MIC-IN
3	MICBIAS
4	GND
5	GND

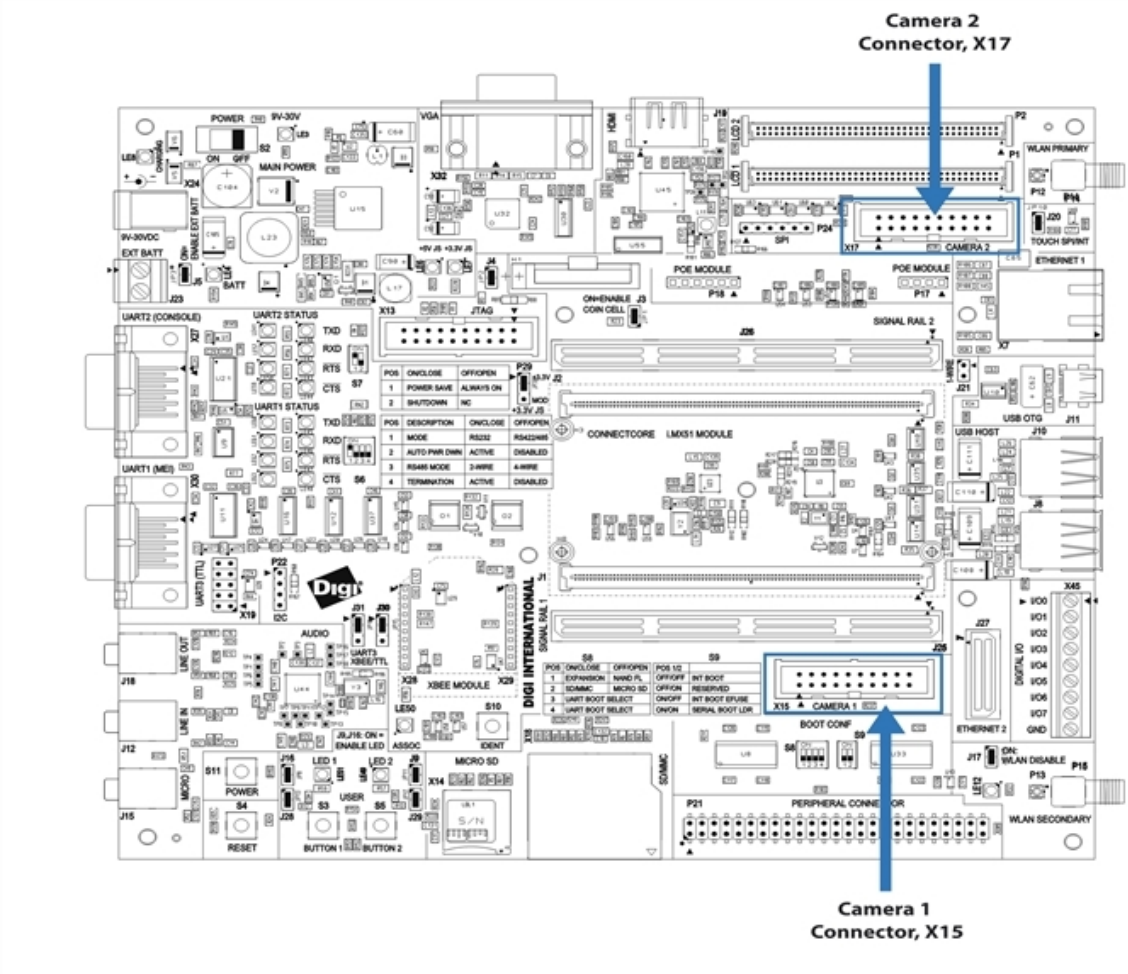
Coin cell battery



Battery Holder	Battery
Vertical Coin-Cell Holder for CR2032 Battery	Lithium coin cell, CR2032, 200mAh
Keystone 1065	Renata CR2032N
Ettinger 15.61.602	Panasonic CR2032N

The development board provides a coin cell battery to back up the module's integrated RTC while main power is disconnected. Jumper J3 controls if the coin cell battery power is available.

Camera interfaces



The development board provides two camera interfaces connected to the camera sensor interfaces of the ConnectCore for i.MX51 CPU. The I2C bus of the ConnectCore for i.MX51CPU is used to configure and control the two cameras.

The I2C device addresses of the Digi camera application kits (CC-ACC0MT9V111) are the following:

Interface	I²C Address (7 bits)
Camera 1	0 x 5C
Camera 2	0 x 48

Two 2 x 10 pin headers, X15 and X17, are provided on the development board for connecting two Digi camera application kits (optional) or customer specific hardware.

- X15 connector for camera 1
- X17 connector for camera 2

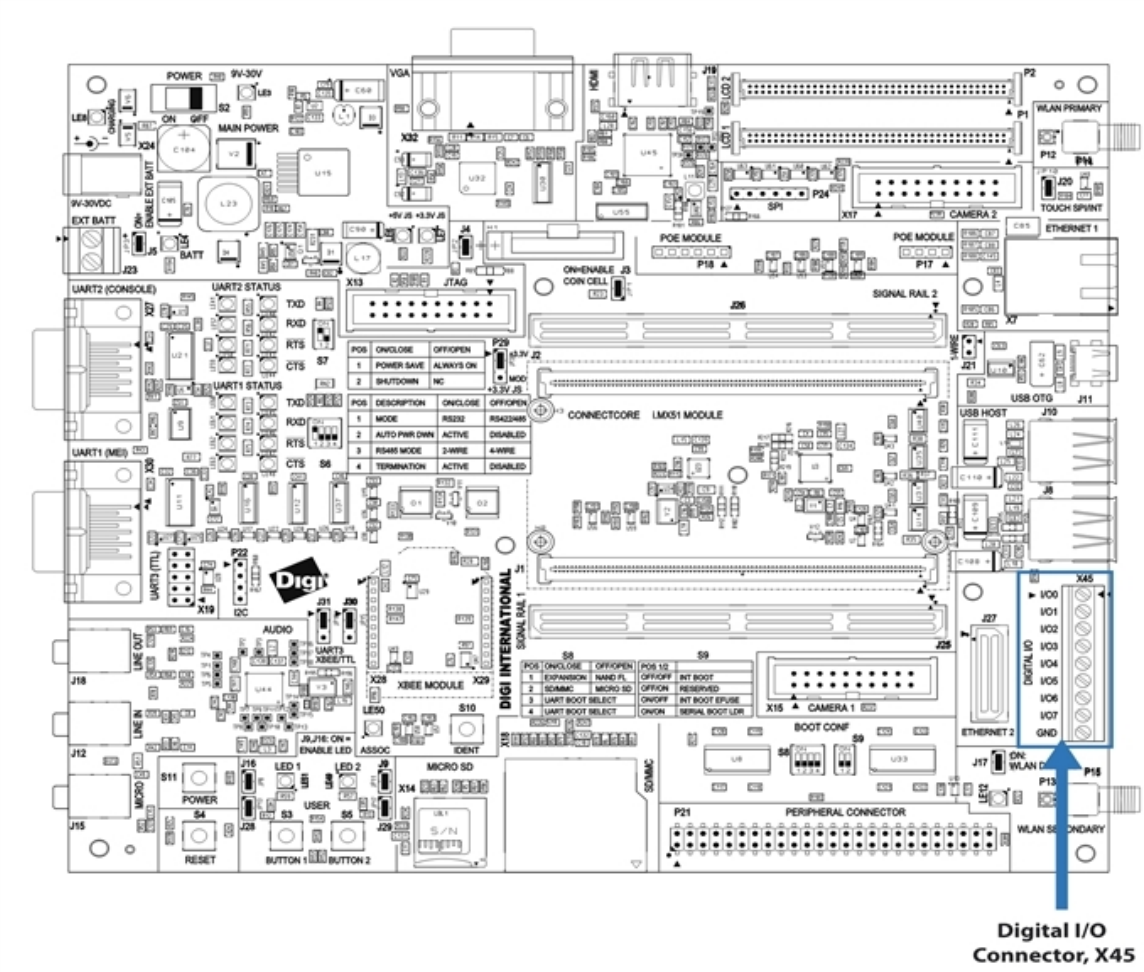
X15 pinout

Pin	Signal	Pin	Signal
1	+2.775V	2	GND
3	CSI1_D12	4	CSI1_D13
5	CSI1_D14	6	CSI1_D15
7	CSI1_D16	8	CSI1_D17
9	CSI1_D18	10	CSI1_D19
11	CSI1_MCLK	12	CSI1_PIXCLK
13	CSI1_HSYNC/GPIO3_15	14	CSI1_VSYNC/GPIO3_14
15	GPIO1_2/I2C2_SCL	16	GPIO1_3/I2C2_SDA
17	CSI1_D10	18	CAMRESET1#/GPIO3_13/CSI1_D19
19	GND	20	CSI1_D11

X17 pinout

Pin	Signal	Pin	Signal
1	+2.775V	2	GND
3	CSI2_D12/GPIO4_9	4	CSI2_D13/GPIO4_10
5	CSI2_D14	6	CSI2_D15
7	CSI2_D16	8	CSI2_D17
9	CSI2_D18/GPIO4_11	10	CSI2_D19/GPIO4_12
11	CSI1_MCLK	12	CSI2_PIXCLK/GPIO4_15
13	CSI2_HSYNC/GPIO4_14	14	CSI2_VSYNC/GPIO4_13
15	GPIO1_2/I2SC2_SCL	16	GPIO1_3/I2C2_SDA
17	-	18	CAMRESET2#/APIO3_7
19	GND	20	-

Digital IO interface



Digital I/O connector, X45

The development board provides a 3.81mm green terminal block, X45, for accessing eight on chip digital GPIOs of the i.MX51 CPU.

Pin	Signal	Voltage Level
1	GPIO3_11/SPI2_MISO/NANDF_RB3	+3.15V
2	GPIO3_18/NANDF_CS2#	+3.15V
3	GPIO3_9/SPI2_RDY/USER_LED2/NANDF_RB1	+3.15V
4	GPIO3_10/SPI2_SCLK/USER_LED1/NANDF_RB2	+3.15V
5	GPIO3_20/NANDF_CS4#	+3.15V

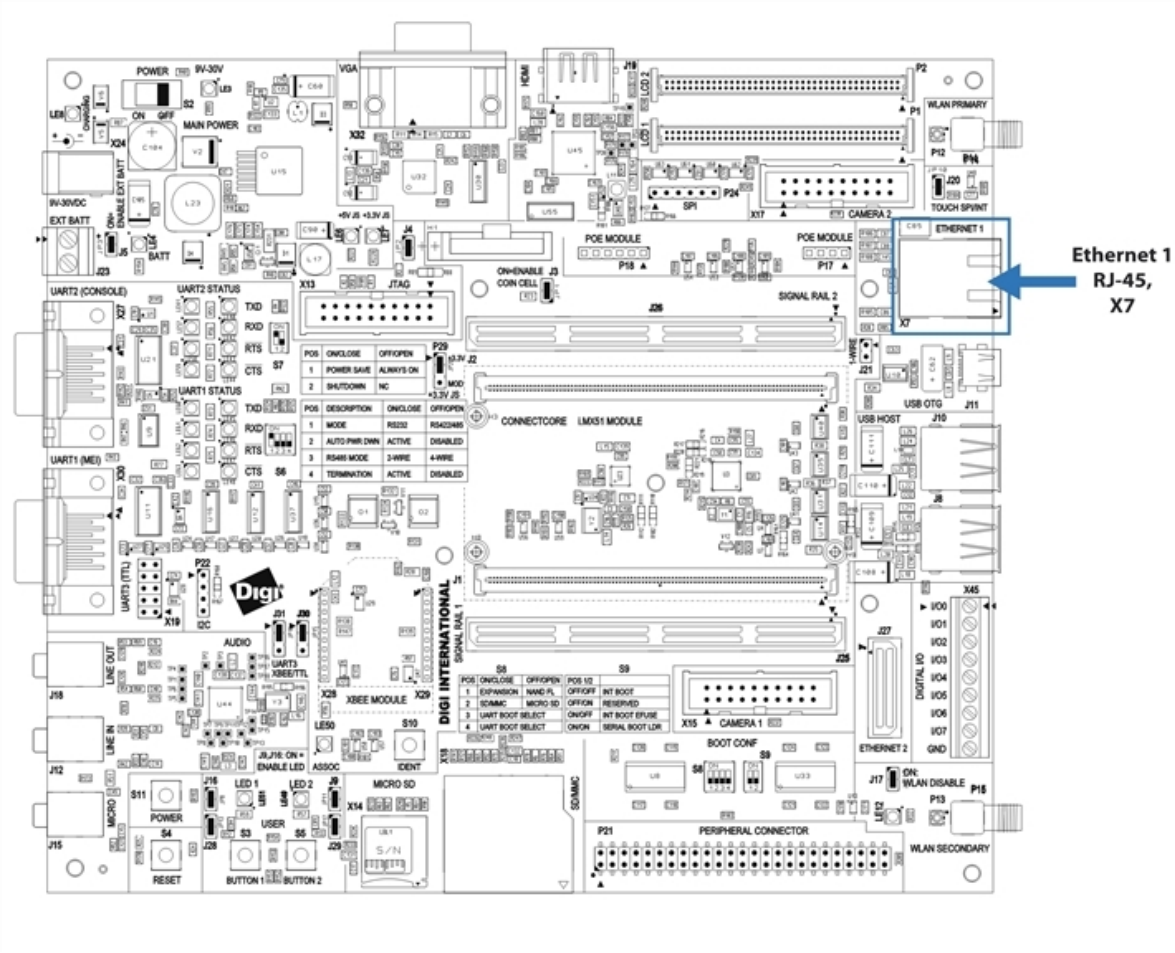
Pin	Signal	Voltage Level
6	GPIO3_21/NANDF_CS5#	+3.15V
7	GPIO3_22/NANDF_CS6#	+3.15V
8	GPIO3_6/DISPB2_SER_DIO/USER_KEY1	+2.775
9	GND	0V

On the development board, GPIO3_6 is connected to USER_KEY1. When using this signal as digital I/O, the USER_KEY1 should not be used.

Note The digital I/O interface is not protected against ESD, over voltage or inverse polarity. Care must be taken when using these signals.

WARNING! X45 pins 1, 3, and 4 should not be connected to GND during boot time if you intend to boot from NAND flash.

Ethernet 1 interface



The development board provides one 8-wire RJ-45 jack with integrated 1:1 transformers and link/activity LEDs for the Ethernet 1 interface. This interface is attached to the Fast Ethernet controller (FEC) of the i.MX51. The ConnectCore for i.MX51 module provides a 10/100 Ethernet PHY chip for this interface.

The Ethernet 1 RJ-45 connector also supports 802.3af (PoE).

Ethernet 1, RJ-45 connector X7

The table below shows the pinout of the Ethernet 1 RJ-45 connector.

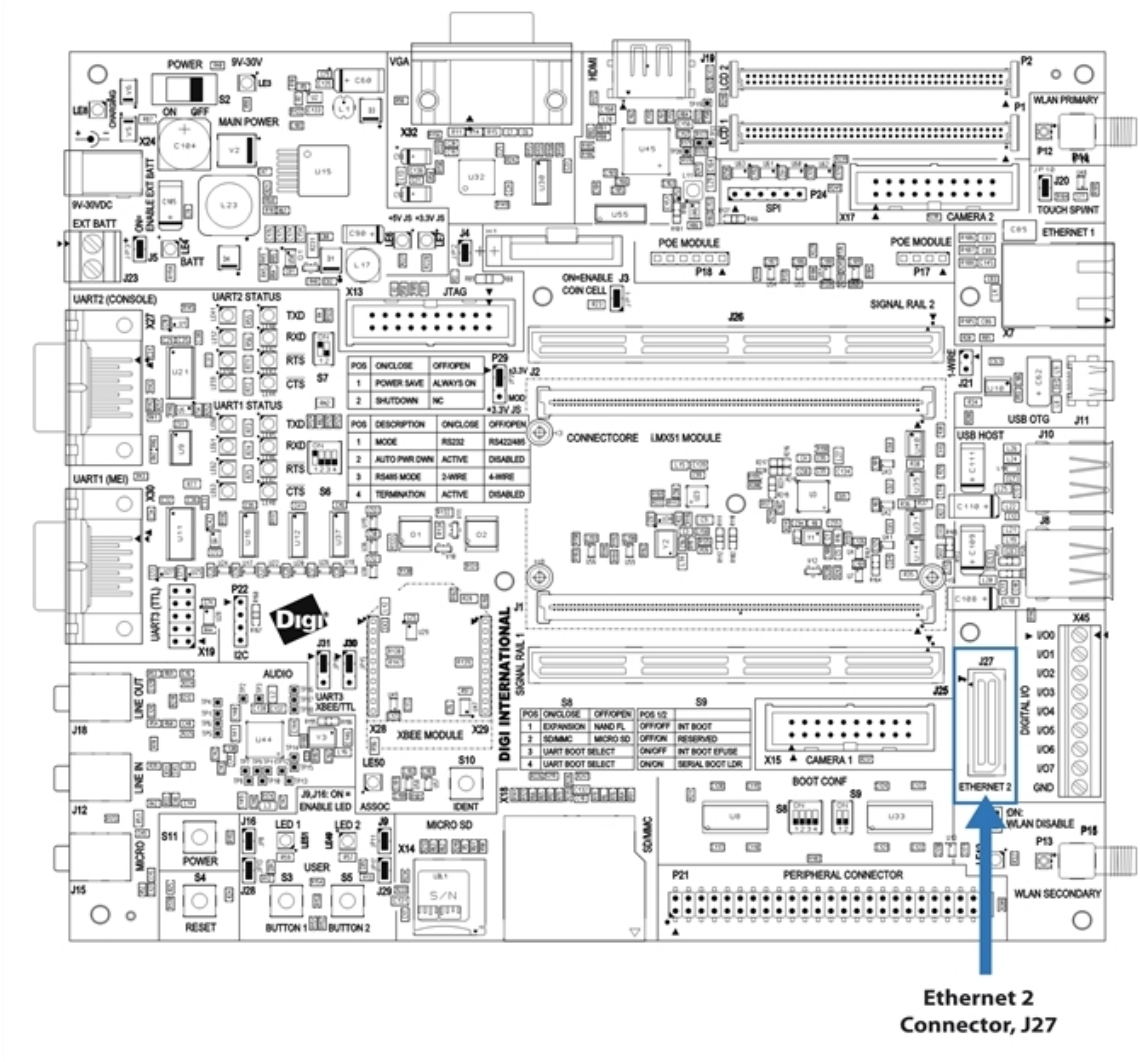
Pin	Signal	802.3af End-Span (mode A)	802.3ad Mid-Span (mode B)	Description
1	TXD+	Negative VPort		Transmit data+
2	TXD-	Negative V_{Port}		Trandmit data-
3	RXD+	Positive V_{Port}		Receive data+

Pin	Signal	802.3af End-Span (mode A)	802.3ad Mid-Span (mode B)	Description
4	EPWR+		Positive V_{Port}	Power from switch+
5	EPWR+		Positive V_{Port}	Power from switch+
6	RXD-	Positive V_{Port}		Receive data-
7	EPWR-		Negative V_{Port}	Power from switch-
8	EPWR-		Negative V_{portP}	Power from switch-

The table below shows the description of the Ethernet 1 LEDs.

LED	Description
Yellow	Network activity (speed): ■ Flashing - indicates network traffic ■ Off - no network traffic
Green	Network link: ■ On - indicates an active network link ■ Off - no network link present

Ethernet 2 interface



The development board provides a 2x20 expansion connector for connecting an optional Digi Ethernet adapter board (100M_ETHADPT) or customer specific setup. The Ethernet 2 interface is provided by an optional on-module Ethernet MAC/PHY.

Note The ConnectCore for i.MX51 modules included in the development kits are supporting the Ethernet 2 interface.

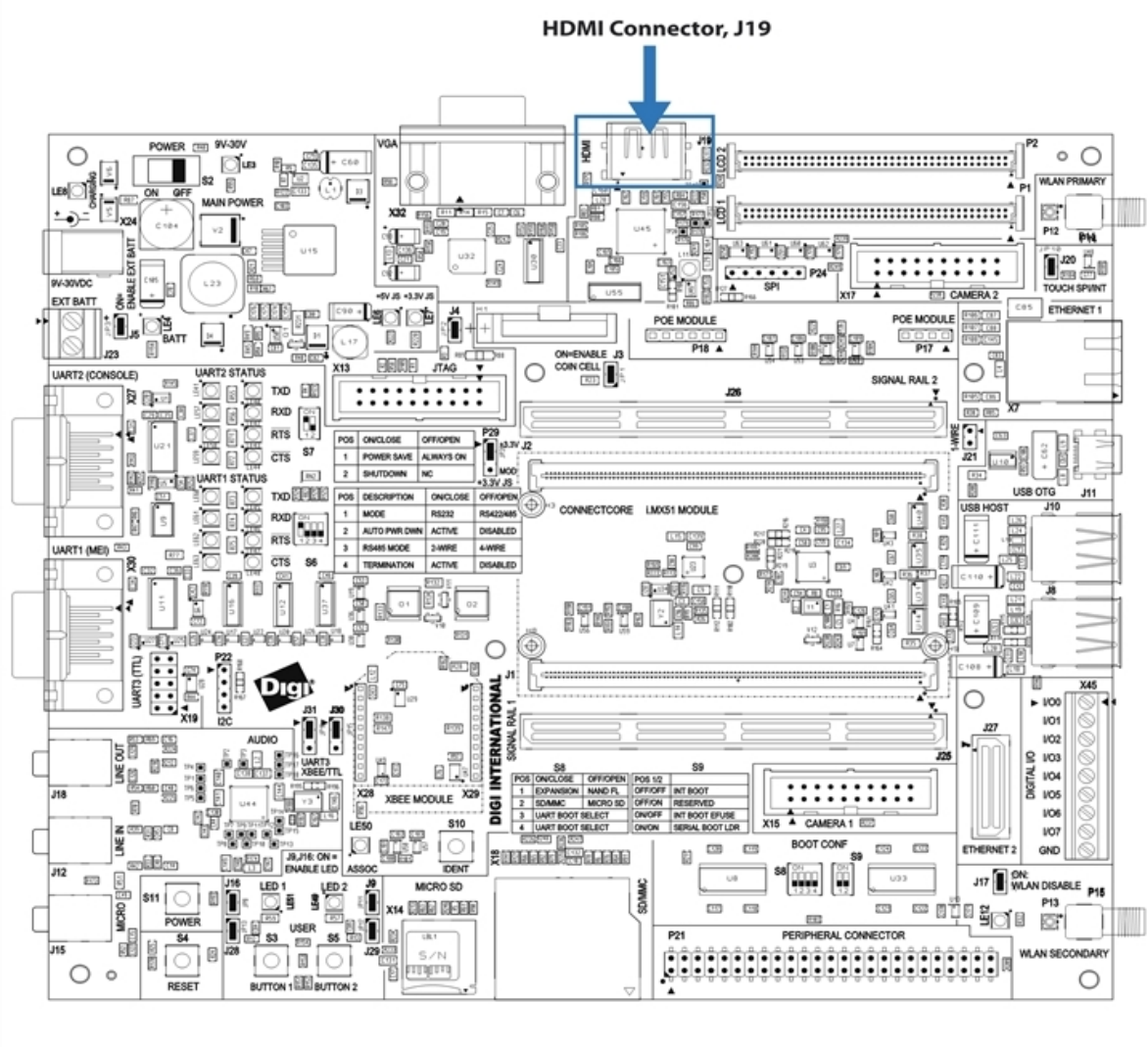
Ethernet 2, connector J17

The table below shows the pinout of the Ethernet 2 expansion connector.

Pin	Signal	Pin	Signal
1	GND	2	GND

Pin	Signal	Pin	Signal
3	ETH2_TX+	4	ETH2_RX+
5	ETH2_TX-	6	ETH2_RX-
7	GND	8	GND
9	Reserved (ETH2_DC+)	10	Reserved (ETH2_DD+)
11	Reserved (ETH2_DC-)	12	Reserved (ETH2_DD-)
13	GND	14	GND
15	ETH2_ACTIVITY#	16	ETH2_LINK#
17	-	18	-
19	-	20	-
21	-	22	-
23	-	24	-
25	-	26	-
27	-	28	-
29	-	30	-
31	-	32	-
33	-	34	-
35	-	36	-
37	-	38	-
39	-	40	-

HDMI interface



The development board provides an HDMI interface connected to the display interface 1 of the ConnectCore for i.MX51 CPU. An Analog Devices AD9389 HDMI transmitter is used in the development board. This HDMI transmitter is controlled through the I²C port 2 of the ConnectCore for i.MX51.

The I²C device address of the HDMI transmitter is the following:

Interface	I²C Address (7 bits)
HDMI transmitter (AD9389)2	0 x 39

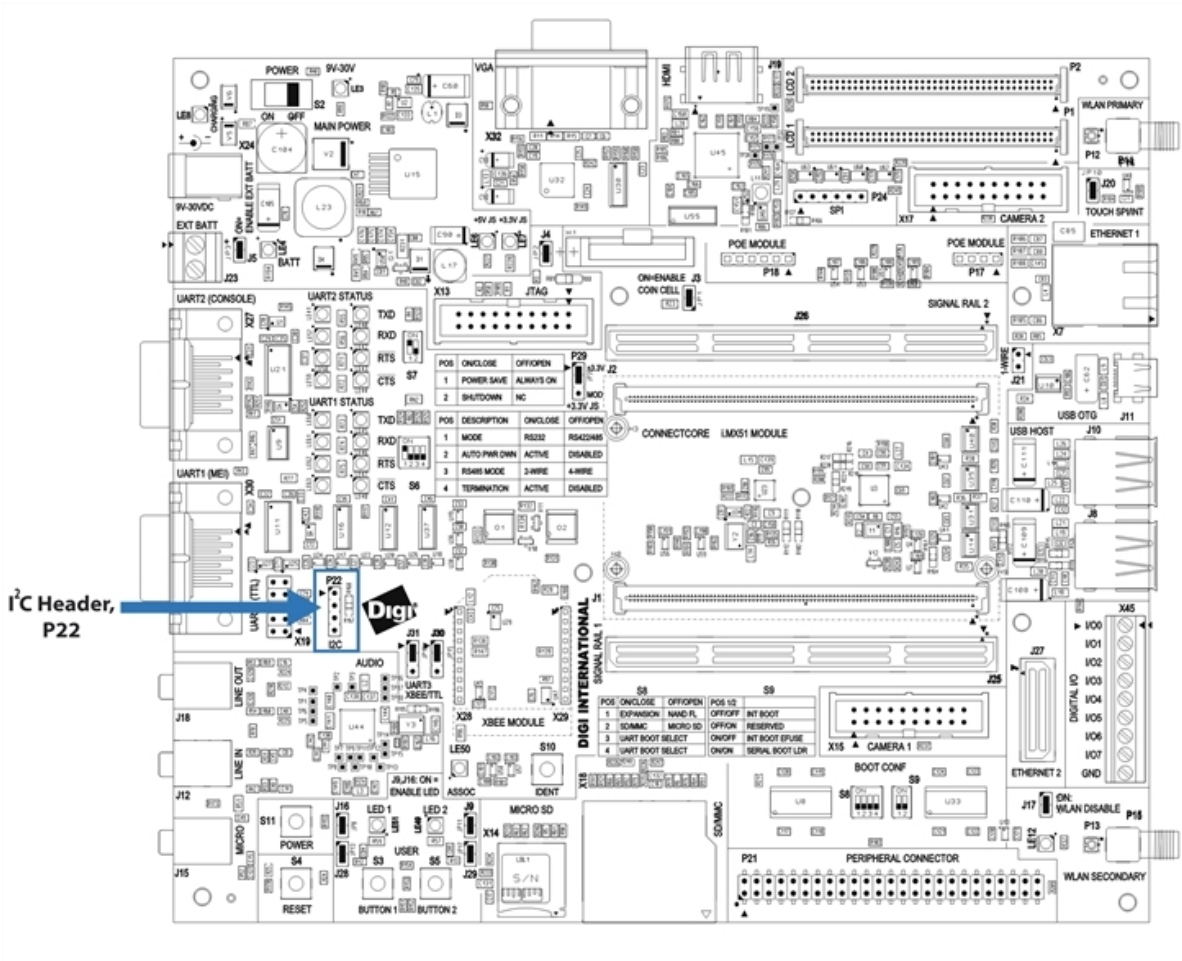
HDMI connector, J19

The development board provides an HDMI connector, J19. The HDMI interface is connected to the Display 1 interface of the ConnectCore for i.MX51 CPU.

The table below shows the pinout of the HDMI connector:

Pin	Signal
1	HDMI_TX2+
2	GND
3	HDMI_TX2-
4	HDMI_TX1+
5	GND
6	HDMI_TX1-
7	HDMI_TX0+
8	GND
9	HDMI_TX0-
10	HDMI_TXC+
11	GND
12	HDMI_TXC-
13	NC
14	NC
15	HDMI_SCL
16	HDMI_SDA
17	GND
18	+5V
19	HOTPLUG_DET

I²C interface



I²C header, P22

Pin header P22 provides access to the i.MX51 I²C port 2 interface.

The I2C port 2 is connected to the following headers/interfaces on the development board.

Interface	I2C Address (7 bits)
I2C Header	-
Camera 1	0 x 5 C (Digi CC-ACC-MT9V111)
Camera 2	0 x 4 8 (Digi CC-ACC-MT9V111)
HDMI Transmitter	0 x 39
LCD 1	-
LCD 2	-

Interface	I2C Address (7 bits)
Audio CODEC	0 x 1A
Peripheral connector	-

I²C port 2 is connected to the following interfaces of the ConnectCore for i.MX51 module:

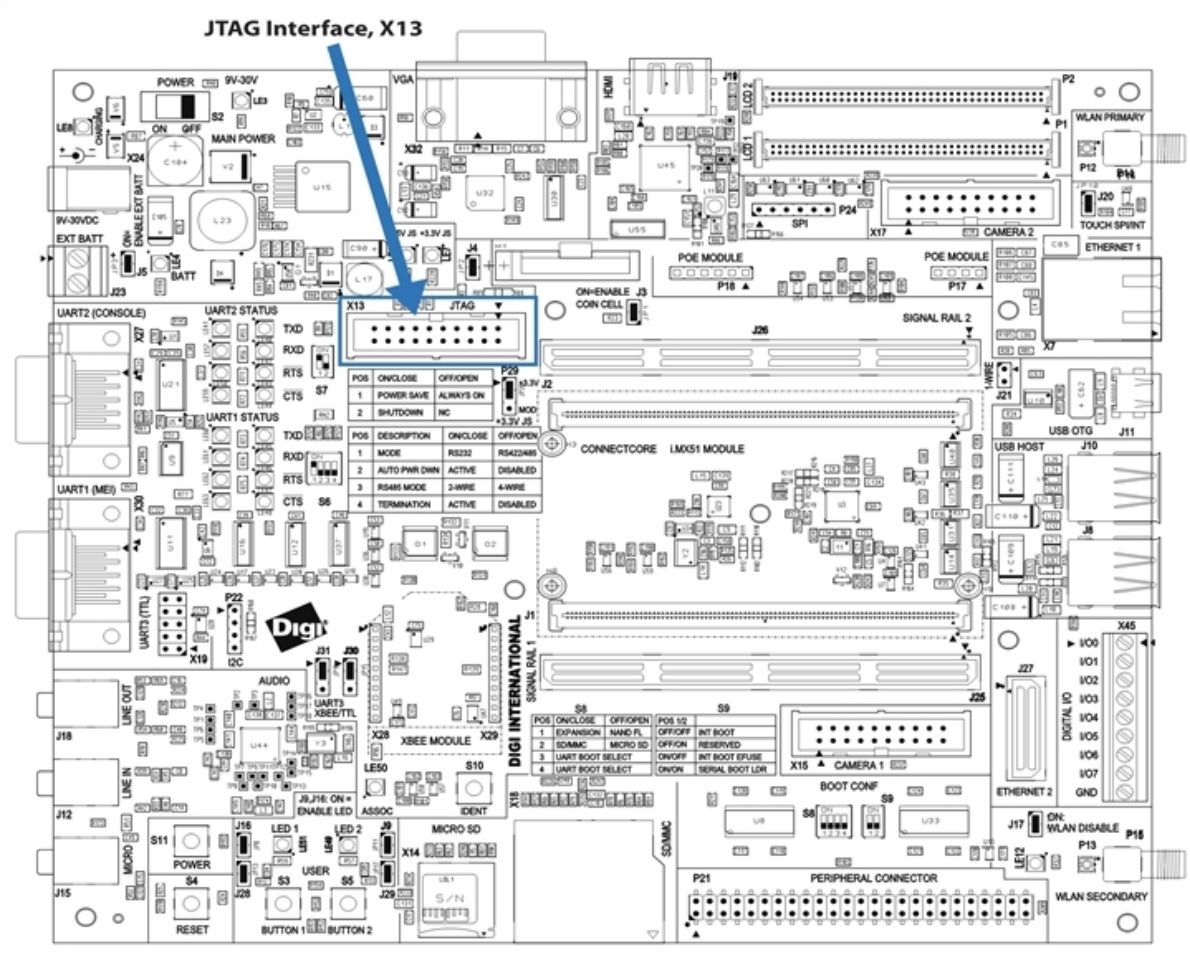
Interface	I²C Address (7 bits)
Accelerometer (MMA7455L)	0 x 1D

The table below provides the pinout of connector P22:

Pin	Function	Defaults to
1	I2C_SDA	GPIO1_3
2	+2.775V	
3	I2_SCL	GPIO1_2
4	GND	

By default, this interface is configured to operate in GPIO mode.

JTAG interface



Standard JTAG ARM connector, X13

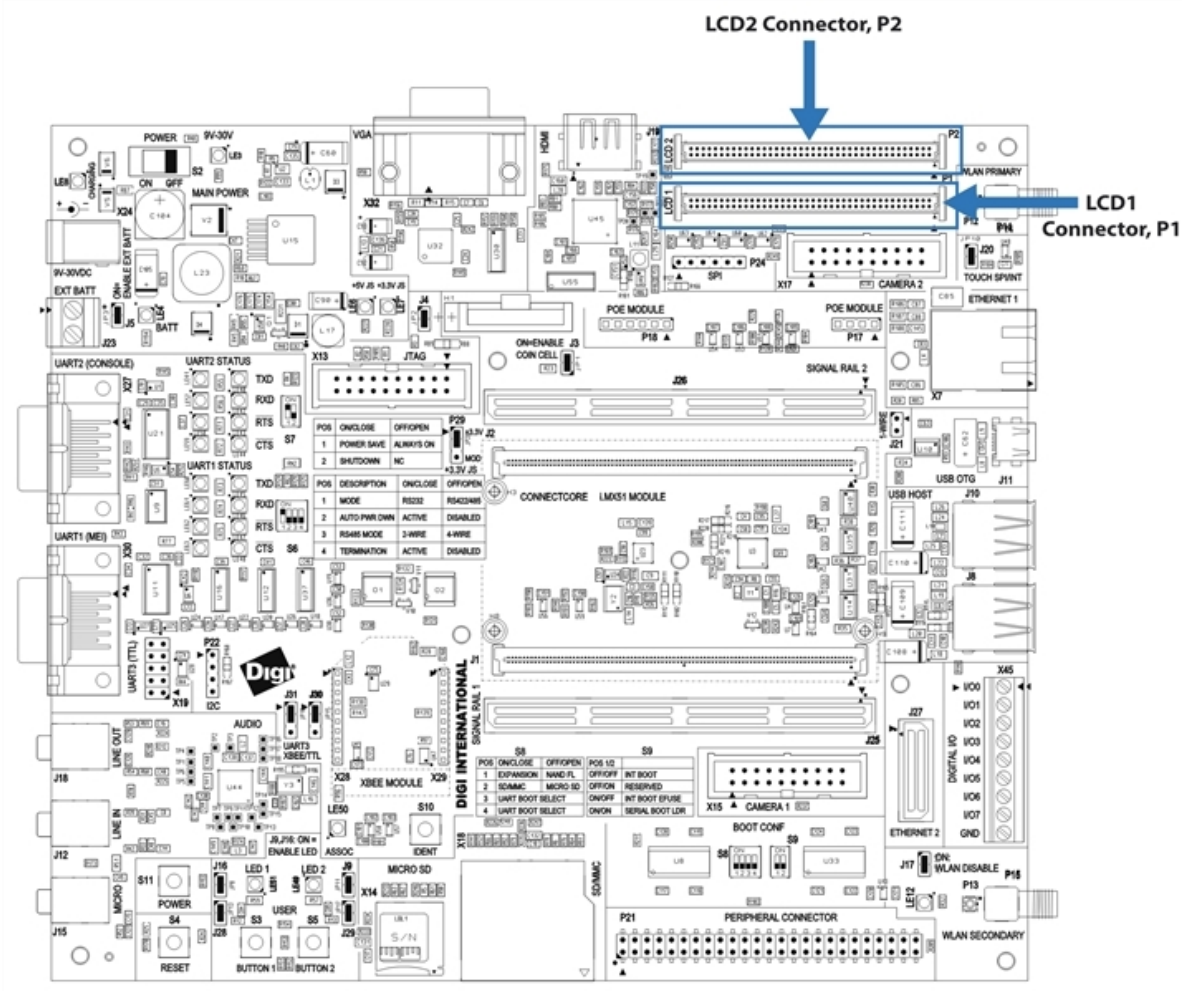
The standard JTAG ARM connector is a 20-pin header and can be used to connect development tools (ICS) such as Ronetix PEEDI or other.

Pin	Function	Pin	Function
1	+1.8V	2	+3.3V
3	JTAG_TRST#	4	GND
5	JTAG_TDI	6	GND
7	JTAG_TMS	8	GND
9	JTAG_TCK	10	GND
11	Reserved (RTCK)	12	GND

Pin	Function	Pin	Function
13	JTAG_TDO	14	GND
15	JTAG_RESET#	16	GND
17	JTAG_DE#	18	GND
19	GND	20	GND

Note In order to enable ETM functionality, Digi offers an optional ETM adapter board (sold separately, Digi P/N CC-ACC-MX51-ETM). Please contact us.

LCD interfaces



The development board provides two 2x40 pin, 1.27mm connectors for accessing a Digi-provided LCD application boards (CC-ACC0LCDW-70) or a user defined LCD application board.

- P1: corresponds to i.MX51 display interface 1
- P2: corresponds to i.MX51 display interface 2

LCD 1 connector, P1

This connector provides access to the following capabilities:

- 18-bit (RGB x 8bit) LCD
- SPI bus for a touch screen controller
- Touch screen (on-module, shared with LCD2)
- Interrupt input for touch screen
- I^2C bus
- 2 x GPIO
- +3.3VDC supply and a 9-30VDC supply

P1 pinout

The table below shows the pinout of the LCD1 connector, P1:

Pin	Function	Pin	Function
1	LCD1_DATA16 (R0)	2	LCD1_DATA17 (R1)
3	LCD1_DATA12 (R2)	4	LCD1_DATA13 (R3)
5	LCD1_DATA14 (R4)	6	LCD1_DATA15 (R5)
7	LCD1_DATA16 (R6)	8	LCD1_DATA17 (R7)
9	-	10	-
11	-	12	-
13	GND	14	GND
15	LCD1_DATA10 (G0)	16	LCD1_DATA11 (G1)
17	LCD1_DATA6 (G2)	18	LCD1_DATA7 (G3)
19	LCD1_DATA8 (G4)	20	LCD1_DATA9 (G5)
21	LCD1_DATA10 (G6)	22	LCD1_DATA11 (G7)
23	-	24	-
25	-	26	-
27	GND	28	GND
29	LCD1_DATA4 (B0)	30	LCD1_DATA5 (B1)
31	LCD1_DATA0 (B2)	32	LCD1_DATA1 (B3)
33	LCD1_DATA2 (B4)	34	LCD1_DATA3 (B5)
35	LCD1_DATA4 (B6)	36	LCD1_DATA5 (B7)
37	-	38	-

Pin	Function	Pin	Function
39	-	40	-
41	GND	42	GND
43	LCD1_BIAS	44	LCD1_PCLK
45	LCD1_PWREN#	46	GND
47	LCD1_VSYNC	48	LCD1_HSYNC
49	-	50	-
51	-	52	-
53	-	54	-
55	GND	56	GND
57	TOUCH_X1	58	TOUCH_Y1
59	TOUCH_X2	60	TOUCH_Y2
61	I2C^2_SDA	62	I2C^2_SCL
63	LCD_SPI_SS#	64	SPI1_CLK
65	SPI1_MOSI	66	SPI1_MISO
67	RESET#	68	LCD1_TOUCH_INT/EXT#
69	LCD1_GPIO1	70	LCD1_GPIO2
71	LCD_PENIRQ	72	GND
73	+3.3V	74	+3.3V
75	+9-30V	76	+9-30V
77	+9-30V	78	+9-30V
79	-	80	-

LCD 2 connector, P2

This connector provides access to the following capabilities:

- 18-bit (RGB x 8bit) LCD
- SPI bus for a touch screen controller
- Touch screen (on-module, shared with LCD1)
- Interrupt input for touch screen
- I^{2}C bus
- 2 x GPIO
- +3.3VDC supply and a 9-30VDC supply

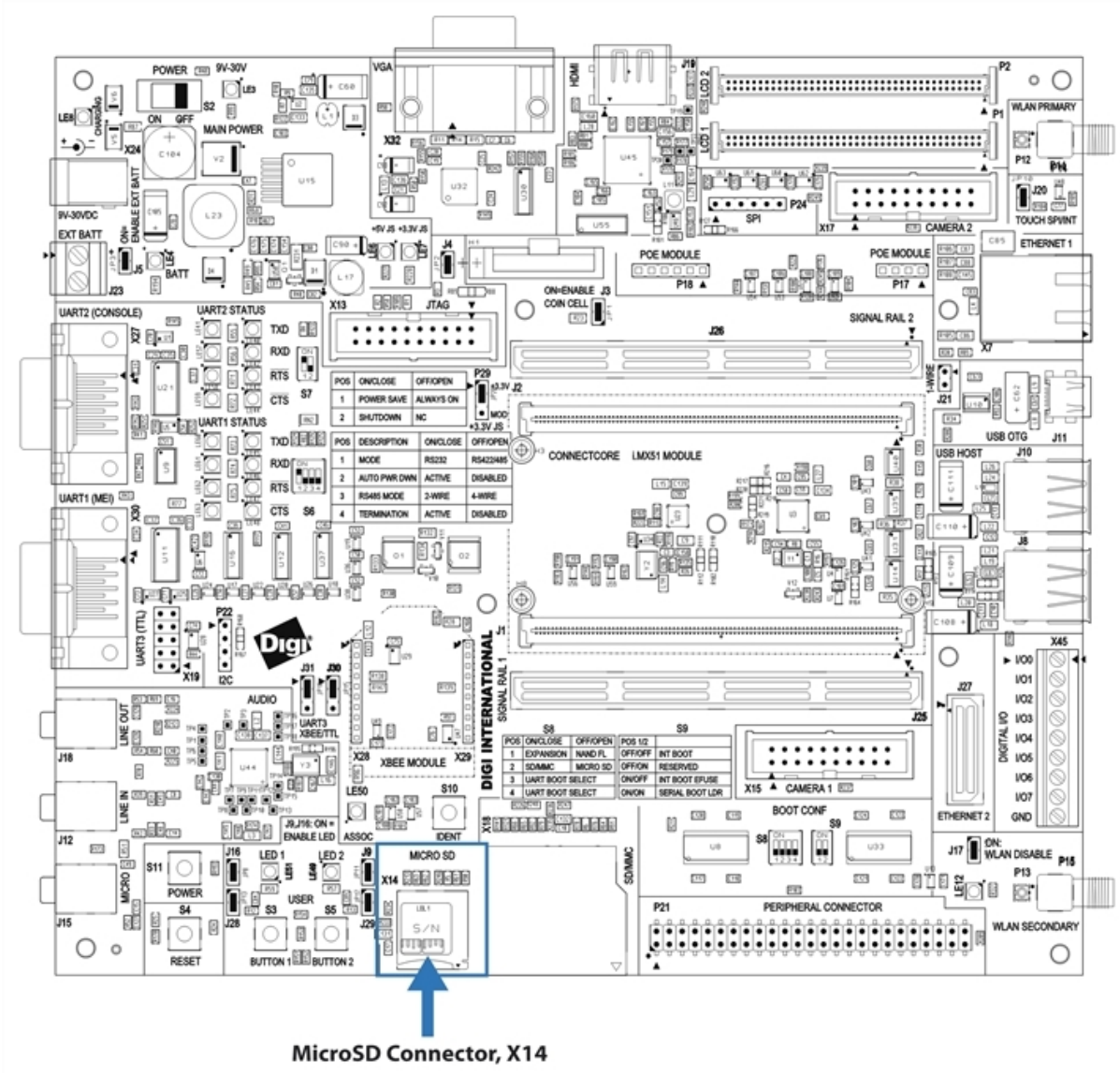
P2 pinout

The table below shows the pinout of the LCD2 connector, P2:

Pin	Function	Pin	Function
1	LCD2_DATA16 (R0)	2	LCD2_DATA17 (R1)
3	LCD2_DATA12 (R2)	4	LCD2_DATA13 (R3)
5	LCD2_DATA14 (R4)	6	LCD2_DATA15 (R5)
7	LCD2_DATA16 (R6)	8	LCD2_DATA17 (R7)
9	-	10	-
11	-	12	-
13	GND	14	GND
15	LCD2_DATA10 (G0)	16	LCD2_DATA11 (G1)
17	LCD2_DATA6 (G2)	18	LCD2_DATA7 (G3)
19	LCD2_DATA8 (G4)	20	LCD2_DATA9 (G5)
21	LCD2_DATA10 (G6)	22	LCD2_DATA11 (G7)
23	-	24	-
25	-	26	-
27	GND	28	GND
29	LCD2_DATA4 (B0)	30	LCD2_DATA5 (B1)
31	LCD2_DATA0 (B2)	32	LCD2_DATA1 (B3)
33	LCD2_DATA2 (B4)	34	LCD2_DATA3 (B5)
35	LCD2_DATA4 (B6)	36	LCD2_DATA5 (B7)
37	-	38	-
39	-	40	-
41	GND	42	GND
43	LCD2_BIAS	44	LCD2_PCLK
45	LCD2_PWREN#	46	GND
47	LCD2_VSYNC	48	LCD2_HSYNC
49	-	50	-
51	-	52	-
53	-	54	-
55	GND	56	GND

Pin	Function	Pin	Function
57	TOUCH_X1	58	TOUCH_Y1
59	TOUCH_X2	60	TOUCH_Y2
61	$I2C^2$_SDA	62	$I2C^2$_SCL
63	LCD_SPI_SS#	64	SPI1_CLK
65	SPI1_MOSI	66	SPI1_MISO
67	RESET#	68	LCD2_TOUCH_INT/EXT#
69	LCD2_GPIO1	70	LCD2_GPIO2
71	LCD_PENIRQ	72	GND
73	+3.3V	74	+3.3V
75	+9-30V	76	+9-30V
77	+9-30V	78	+9-30V
79	LED_BCK+	80	LED_BCK-

MicroSD™ card interface



MicroSD connector, X14

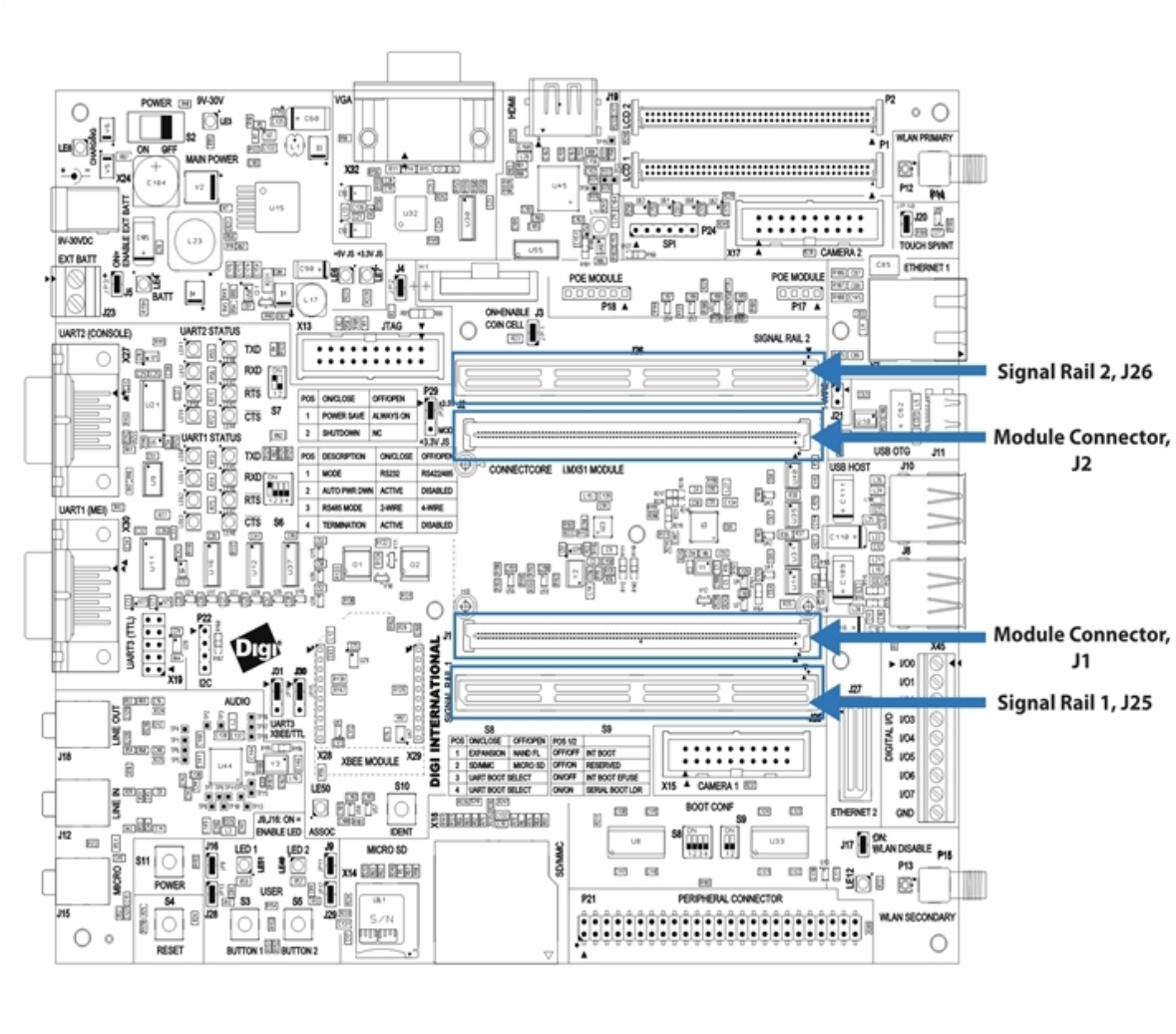
The development board provides one MicroSD card connector, X14. This interface is connected to the enhanced Secured Digital Host controller 1 (eSDHC1) of the i.MX51 CPU.

The MicroSD connector used on the development board does not provide a card detect pin (pin-9 and pin-10 are connected to chassis). A hot-plug insertion or removal is not possible with this connector.

The following table shows the pinout of the MicroSD connector:

Pin	Signal
1	SD_DATA2
2	SD_DATA3
3	SD_CMD
4	+3.3V
5	SD_CLK
6	GND
7	SD_DATA0
8	SD_DATA1
9	SD_CD (Connected to chassis)
10	SD_CD (Connected to chassis)

Module connectors and signal rails



Module connectors

See the Module pinout for related information.

Signal rails, J25 and J26

The development board provides two 2x80 pin signal rails, J25 and J26. These connectors provide most of the signals available on the module connectors and can be used for measurement or development purposes.

- J25 corresponds to module connector J1
- J26 corresponds to module connector J2

J25 pinout

Pin	Signal	Pin	Signal
1	CSI1_D8	2	CSI1_D9
3	CSI1_D10	4	CSI1_D11
5	CSI1_D12	6	CSI1_D13
7	CSI1_D14	8	CSI1_D15
9	CSI1_D16	10	CSI1_D17
11	CSI1_D18	12	CSI1_D19
13	CSI1_VSYNC/GPIO3_14	14	CSI1_HSYNC/GPIO3_15
15	CSI1_PIXCLK	16	CSI1_MCLK
17	WLAN_TDO	18	WLAN_TCK
19	WLAN_TDI	20	WLAN_TMS
21	WLAN_LED	22	RS_BT_PRIORITY
23	RS_WLAN_ACTIVE	24	RS_BT_ACTIVE
25	+2.775V	26	WLAN_DISABLE#
27	+2.775V	28	+2.775V
29	MC13892_GPO1	30	+2.775V
31	PMIC_PWRON1	32	PMIC_STDBY_REQ
33	PMIC_INT_REQ	34	PWRGTDRV1
35	CHRGLED	36	PWRGTDRV2
37	CHRGSE1#	38	VCC_COINCELL
39	VLIO	40	+5V_IN
41	VLIO	42	+5V_IN
43	VLIO	44	+5V_IN
45	DISP2_SER_DIN/GPIO3_5	46	DISPB2_SER_DIO/GPIO3_6
47	DISPB2_SER_RS/GPIO3_8	48	DISPB2_SER_CLK/GPIO3_7
49	DISP2_DATA0/MII_RXD3/USBH3_CLK	50	DISP2_DATA1/MII_RX_ER/USBH3_DIR
51	DISP2_DATA2	52	DISP2_DATA3
53	DISP2_DATA4	54	DISP2_DATA5
55	DISP2_DATA6/MII_TXD1/USBH3_STP	56	DISP2_DATA7/MII_TXD2/USBH3_NXT

Pin	Signal	Pin	Signal
57	DISP2_DATA8/MII_TXD3/USBH3_DATA0	58	DISP2_DATA9/MII_TXEN/USBH3_DATA1
59	DISP2_DATA10/MII_COL/USBH3_DATA2	60	DISP2_DATA11/MII_RX_CLK/USBH3_DATA3
61	DISP2_DATA12/MII_RX_DV/USBH3_DATA4	62	DISP2_DATA13/MII_TX_CLK/USBH3_DATA5
63	DISP2_DATA14/MII_RXD0/USBH3_DATA6	64	DISP2_DATA15/MII_TXD0/USBH3_DATA7
65	D12_PIN2/MII_MDC	66	D12_DISP_CLK/MII_RXD1
67	D12_PIN4/MII_CRS	68	D12_PIN3/MII_MDIO
69	IOR	70	IOG
71	IOR_BACK	72	IOG_BACK
73	IOB	74	JTAG_TRST#
75	IOB_BACK	76	JTAG_MOD#
77	JTAG_TCK	78	JTAG_DE#
79	JTAG_TMS	80	RESET_IN#
81	JTAG_TDI	82	+1.8V
83	JTAG_TDO	84	EIM_CS1/GPIO2_26
85	POR#	86	EIM_CS3/GPIO2_28
87	EIM_CS0/GPIO2_25	88	EIM_CS5_LAN9221_CS#/GPIO2_30
89	EIM_CS2/GPIO2_27	90	EIM_LBA/GPIO3_1
91	EIM_CS4/GPIO2_29	92	EIM_DA1/TRACE17
93	EIM_DTACK/GPIO2_31	94	EIM_DA3/TRACE19
95	EIM_DA0/TRACE16	96	EIM_DA5/TRACE21
97	EIM_DA2/TRACE18	98	EIM_DA7/TRACE23
99	EIM_DA4/TRACE20	100	EIM_DA9/TRACE25
101	EIM_DA6/TRACE22	102	EIM_DA11/TRACE27
103	EIM_DA8/TRACE 24	104	EIM_DA13/TRACE29
105	EIM_DA10/TRACE26	106	EIM_DA15/TRACE31
107	EIM_DA12/TRACE28	108	EIM_DA17/TRACE1
109	EIM_DA14/TRACE30	110	EIM_DA19/TRACE3

Pin	Signal	Pin	Signal
111	EIM_DA16/TRACE0	112	EIM_DA21/TRACE5
113	EIM_DA18/TRACE2	114	EIM_DA23/TRACE7
115	+3.15V	116	EIM_DA25/TRACE9
117	EIM_DA20/TRACE4	118	EIM_DA27/TRACE11
119	EIM_DA22/TRACE6	120	EIM_DA29/TRACE13
121	EIM_DA24/TRACE8	122	EIM_DA31/TRACE15
123	EIM_DA26/TRACE10	124	EIM_A17/GPIO2_11
125	EIM_DA28/TRACE12	126	EIM_A19/GPIO2_13
127	EIM_DA30/TRACE14	128	EIM_A21/GPIO2_15
129	EIM_A16/GPIO2_10	130	EIM_A23/GPIO2_17
131	EIM_A18/GPIO2_12	132	EIM_A25/GPIO2_19
133	EIM_A20/GPIO2_14	134	EIM_A27/GPIO2_21
135	EIM_A22/GPIO2_16	136	EIM_OE#/GPIO2_24
137	EIM_A24/GPIO2_18	138	EIM_RW#
139	EIM_A26.GPIO2_20	140	EIM_CRE/GPIO3_2
141	EIM_EB0	142	EIM_WAIT
143	EIM_EB1	144	GND
145	EIM_EB2/GPIO2_22/TRCTL	146	EIM_BCLK
147	EIM_EB3/GPIO2_23/TRCLK	148	GND
149	NANDF_ALE/GPIO3_5	150	NAND_RE#/SD3_DATA1/GPIO3_4
151	NANDF_WP#/SD3_DATA2/GPIO3_7	152	NANDF_CLE/GPIO3_6
153	NANDF_RB1_SP12_RDY/GPIO3_9	154	NANDF_RB0/SD3_DATA3/GPIO3_8
155	NANDF_RB3/SP12_MISO/GPIO3_11	156	NANDF_R2/SP12_SCLK/GPIO3_10
157	-	158	-
159	-	160	-

J26 pinout

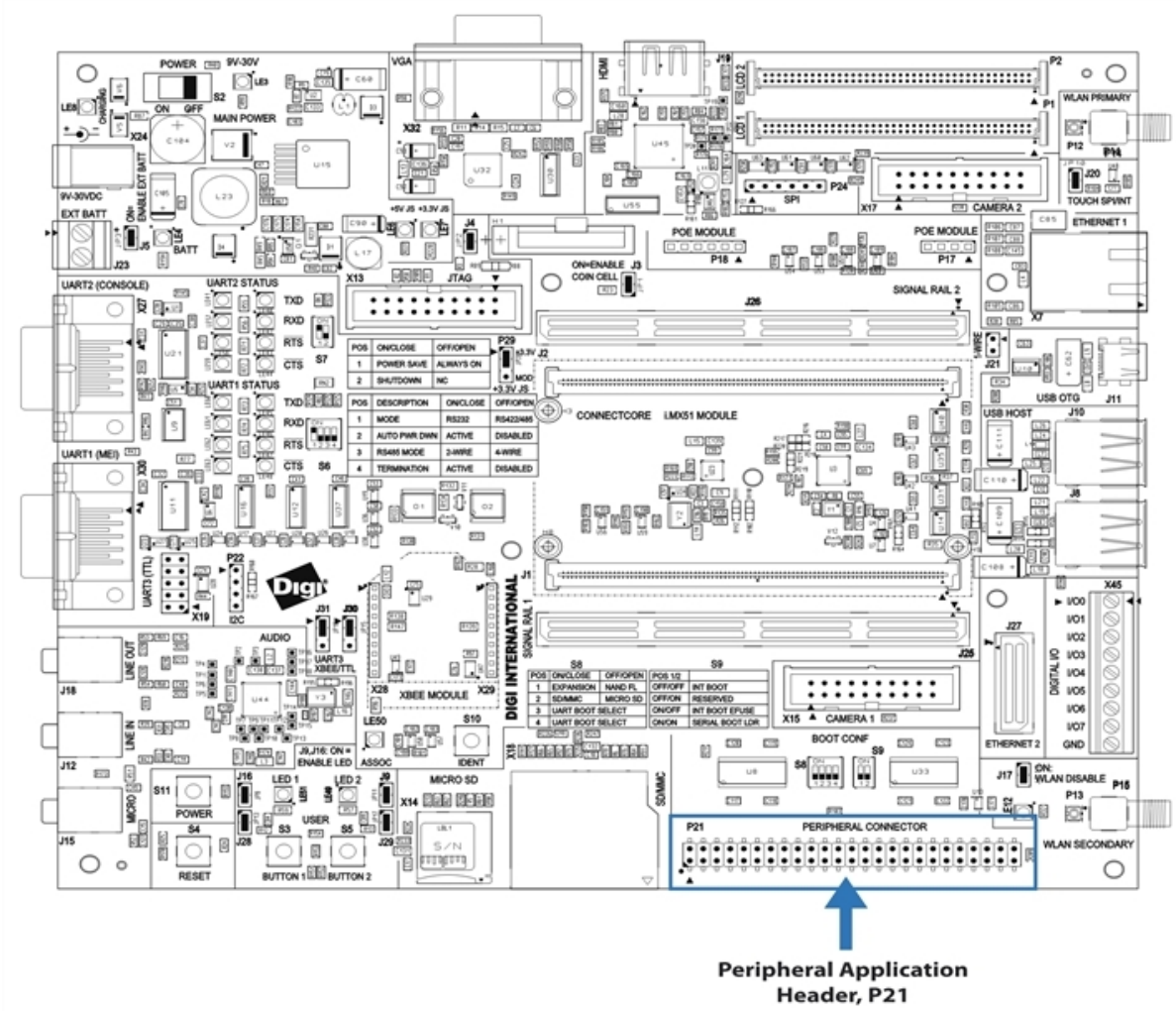
Pin	Signal	Pin	Signal
1	DISP1_DAT0	2	DISP1_DAT1
3	DISP1_DAT2	4	DISP1_DAT3

Pin	Signal	Pin	Signal
5	DISP1_DAT4	6	DISP1_DAT5
7	DISP1_DAT6	8	DISP1_DAT7
9	DISP1_DAT8	10	DISP1_DAT9
11	DISP1_DAT10	12	DISP1_DAT11
13	DISP1_DAT12	14	DISP1_DAT13
15	DISP1_DAT14	16	DISP1_DAT15
17	DISP1_DAT16	18	DISP1_DAT17
19	DISP1_DAT18	20	DISP1_DAT19
21	DISP1_DAT20	22	DISP1_DAT21
23	DISP1_DAT22	24	DISP1_DAT23
25	DI1_PIN2	26	DI1_DISP_CLK
27	DI1_PIN11/GPIO3_0	28	DI1_PIN3
29	DI1_PIN13/GPIO3_2	30	DI1_PIN12/GPIO3_1
31	DI1_PIN15	32	DI_GP1
33	DI_GP2	34	DI_GP3/MII_TX_ER
35	DI_GP4/MII_RXD2	36	DI1_D0_CS/GPIO3_3
37	DI1_D1_CS/GPIO3_4	38	ADIN5
39	TOUCH_X1	40	ADIN6
41	TOUCH_X2	42	ADIN7
43	TOUCH_Y1	44	ADC_GND
45	TOUCH_Y2	46	ADTRIG
47	SWBST	48	-
49	LEDR	50	-
51	LEDG	52	-
53	LEDB	54	-
55	CSI2_D12/GPIO4_9	56	CSI2_D13/GPIO4_10
57	CSI2_D14	58	CSI2_D15
59	CSI2_D16	60	CSI2_D17
61	CSI2_D18/GPIO4_11	62	CSI2_D19/GPIO4_12

Pin	Signal	Pin	Signal
63	CSI2_VSYNC/GPIO4_13	64	CSI2_HSYNC/GPIO4_14
65	CSI2_PIXCLK/GPIO4_15	66	GPIO1_8/USB_PWR
67	GPIO1_7/MMA7455LR_INT1	68	GPIO1_2/PWM1/I2C2_SCL
69	GPIO1_6/MMA7455LR_INT2	70	GPIO1_3/PWM2/I2C2_SDA
71	CKIH1	72	CLK32K_PER
73	SD2_DATA0/SD1_DATA4/SPI_MOSI	74	CKIH2
75	SD2_DATA1/SD1_DATA5	76	SD2_CLK/I2C1_SDA/SPI_SCLK
77	SD2_DATA2/SD1/DATA6	78	SD2_CMD/I2C1_SCL/SPI_MOSI
79	SD2_DATA3/SD1_DATA7/SPI_SS2	80	KEY_COL0
81	ROW0	82	KEY_COL1
83	ROW1	84	KEY_COL2
85	ROW2	86	KEY_COL3
87	ROW3	88	KEY_COL5/UART3_CTS#/I2C2_SDA
89	KEY_COL4/UART3_RTS#/I2C2_SCL	90	GPIO1_0/SD1_CD#/SPI_SS2
91	OWIRE_LINE/GPIO1_24	92	GPIO1_1/SD1_WP#/SPI_MISO
93	SC1_CMD/AUD5_RXFS/SPI_MOSI	94	SD1_DAT0/AUD5_TXD/SPI_MOSI
95	SD1_CLK/AUD5_RXC/SPI_SCLK	96	SD1_DATA1/AUD5_RXD
97	WDOG1#/GPIO1_4	98	SD1_DATA2/AUD5_TXC
99	CSPI1_MOSI/I2C1_SDA/GPIO4_22	100	SD1_DATA3/AUD5_TXFS/SPI_SS1
101	CSPI1_MISO/AUD4_RXD/GPIO4_23	102	CSPI1_SS0_PMIC/AUD4_TXC/GPIO4_24
103	CSPI1_SCLK/I2C1_SDA/GPIO4_27	104	CSPI1_SS1/AUD4_TXD/GPIO4_25
105	UART1_RXD/GPIO4_28	106	CSPI1_RDY/AUD4_TXFS/GPIO4_26
107	UART1_TXD/PWM2/GPIO4_29	108	UART1_RTS#/GPIO4_30
109	UART2_RXD/GPIO1_20	110	UART1_CTS#/GPIO4_31
111	UART2_TXD/GPIO1_21	112	UART3_RXD/UART1_DTR#/GPIO1_22
113	USBH1_DATA2/UART2_TXD/GPIO1_13	114	UART3_TXD/UART1_DSR#/GPIO_23
115	USBH1_DATA4/SPI_SS0/GPIO1_15	116	USBH1_DATA0/UART2_CTS#/GPIO1_11
117	USBH1_DATA6/SPI_SS2/GPIO1_17	118	USBH1_DATA1/UART2_RXD/GPIO1_12
119	USBH1_DIR/SPI_MOSI/GPIO1_26/I2C2_SDA	120	USBH1_DATA3/UART2_RTS#/GPIO1_14

Pin	Signal	Pin	Signal
121	USBH1_STP/SPI_RDY/GPIO1_27	122	USBH1_DATA5/SPI_SS1/GPIO1_16
123	USBH1_NXT/SPI_MISO/GPIO1_28	124	USBH1_DATA7/SPI_SS3/SPI2_SS3/GPIO1_18
125	AUD3_BB_TXD/GPIO4_18	126	USBH1_CLK/SPI_SCLK/GPIO1_25/I2C2_SCL
127	AUD3_BB_RXD/UART3_RXD/GPIO4_19	128	HS_I2C_SCL/GPIO4_16
129	AUD3_BB_CK/GPIO4_20	130	HS_I2C_SDA/GPIO4_17
131	+3.3V MOD	132	AUD3_BB_FS/UART3_TXD/GPIO4_21
133	NANDF_D0/PATA_D0/SD4_DATA7/GPIO4_8	134	+3.3V
135	NANDF_D2/PATA_D2/SD4_DATA5/GPIO4_6	136	NANDF_D1/PATA_D1/SD4_DATA6/GPIO4_7
137	NANDF_D4/PATA_D4/SD4_CD/GPIO4_4	138	NANDF_D3/PATA_D3/SD4_DATA4/GPIO4_5
139	NANDF_D6/PATA_D6/SD4_LCTL/GPIO4_2	140	NANDF_D5/PATA_D5/SD4_WP#/GPIO4_3
141	NANDF_D8/PATA_D8/GPIO4_0/SD3_DATA0	142	NANDF_D7/PATA_D7/GPIO4_1
143	NANDF_D10/PATA_D10/GPIO3_30/SD3_D2	144	NANDF_D9/PATA_D9/GPIO3_31/SD3_D1
145	NANDF_D12/PATA_D12/GPIO3_28/SD3_D4	146	NANDF_D11/PATA_D11/GPIO3_29/SD3_D3
147	NANDF_D14/PATA_D14/GPIO3_26/SD3_D6	148	NANDF_D13/PATA_D13/GPIO3_27/SD3_D5
149	NANDF_CS0#/GPIO3_16	150	NANDF_D15/PATA_D15/GPIO3_25/SD3_D7
151	NANDF_CS2#/PATA_CS0#/GPIO3_18	152	NANDF_CS1#/GPIO3_17
153	NANDF_CS4#/PATA_DA0/GPIO3_20	154	NANDF_CS3#/PATA_CS1#/GPIO3_19
155	NANDF_CS6#/PATA_DA2/GPIO3_22	156	NANDF_CS5#/PATA_DA1/GPIO3_21
157	NANDF_RDY_INT/GPIO3_24	158	NANDF_CS7#/GPIO3_23
159	NANDF_WE#/PATA_DIOW/GPIO3_3	160	GPIO_NAND/PATA_INTRQ/GPIO3_12

Peripheral application header



The development board provides one, 2x25-pin, 2.54mm pitch header for applications-specific daughter cards/expansion boards:

- P21, Peripheral application header. Provides access to a 16-bit data bus, 10-bit address bus and control signals (such as CS#, OE#, WE#), as well as I2C and power (+3.3V). Using these signals you can connect Digi-specific extension modules or your own custom daughter card to the module's address/data bus and other interfaces.

Peripheral application header, P21

Pin	Signal	Pin	Signal
1	GND	2	D0
3	D1	4	D2

Pin	Signal	Pin	Signal
5	D3	6	GND
7	D4	8	D5
9	D6	10	D7
11	GND	12	D8
13	D9	14	D10
15	D11	16	GND
17	D12	18	D13
19	D14	20	D15
21	GND	22	8-bit / 16-bit (default)
23	GND	24	+3.3V
25	+3.3V	26	A0
27	A1	28	A2
29	A3	30	GND
31	A4	32	A5
33	A6	34	A7
35	GND	36	A8
37	A9	38	GND
39	CS0#	40	$I2C^2$_SDA/GPIO1_3
41	WE#	42	OE#
43	$I2C^2$_SCL/GPIO1_2	44	GPIO3_2
45	+3.3V	46	+3.3V
47	BE2#	48	BE3#
49	BCLK	50	GND

The voltage level of the data, address and control signals provided by the module is +1.8V. A level shifter is provided on the development board to buffer and change the voltage level of most peripheral application signals on this header to +3.3V.

The Data bus signals D0 - D15 are connected to the i.MX51 data bus signals D16 - D31.

The Address bus signals A0 - A9 are connected to the i.MX51 data/address bus signals DA0 - DA9.

The BE2# signal is connected to the i.MX51 byte enable 2 (D16 - D23).

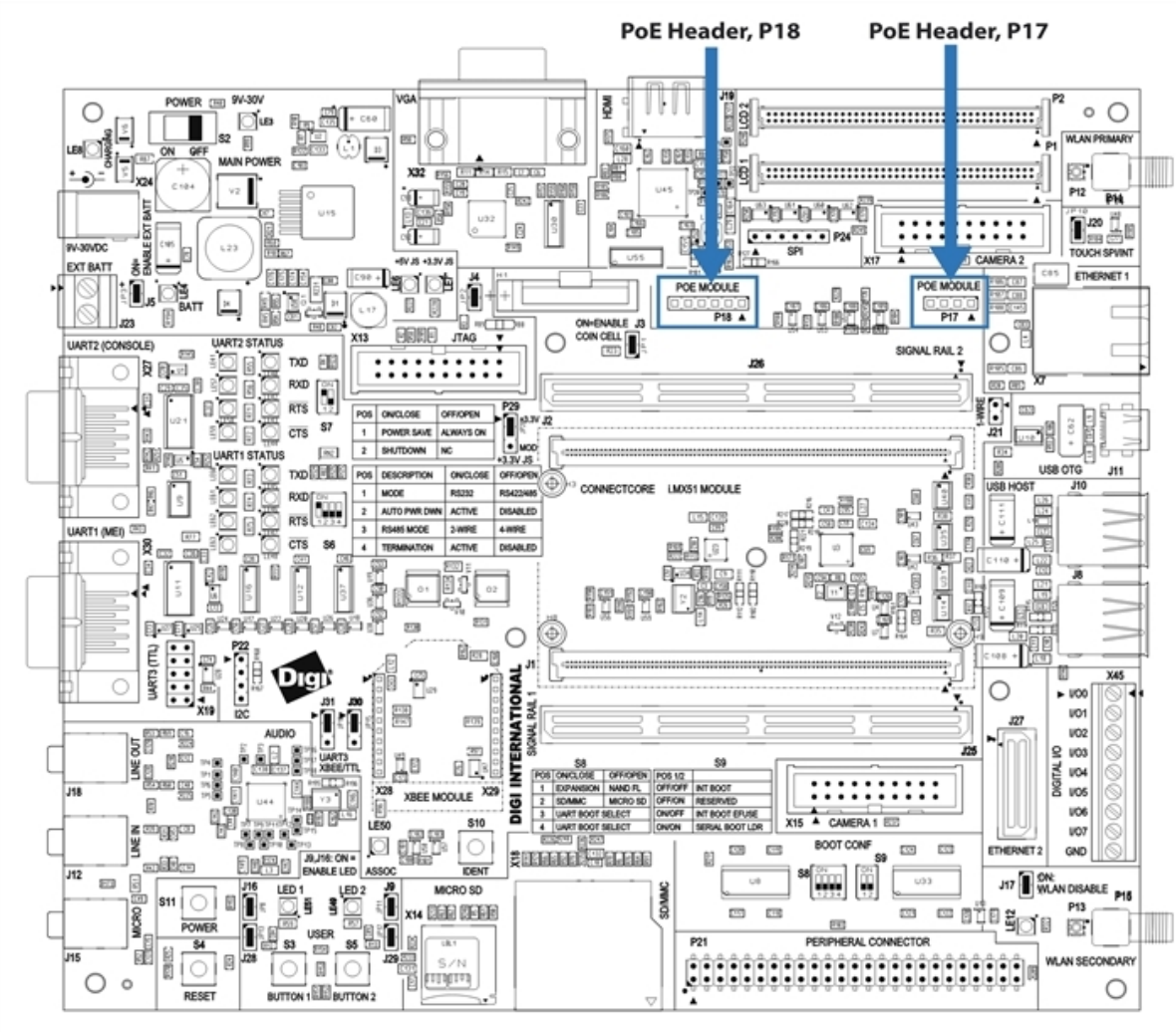
The BE3# signal is connected to the i.MX51 byte enable 3 (D24 - D31).

The BCLK signal corresponds to the i.MX51 burst clock signal. This clock signal is not buffered, and its voltage level is +1.8V. This signal is connected to the peripheral connector through a 0R resister. By default, this resistor is not populated.

The I2C interface corresponds to i.MX51 I2C port 2. For more information, refer to About the module.

The signal GPIO3_2 can only be used as an input signal to the i.MX51. This signal is intended to be used as interrupt line in the peripheral boards.

Power-Over-Ethernet (PoE) - IEEE802.3af



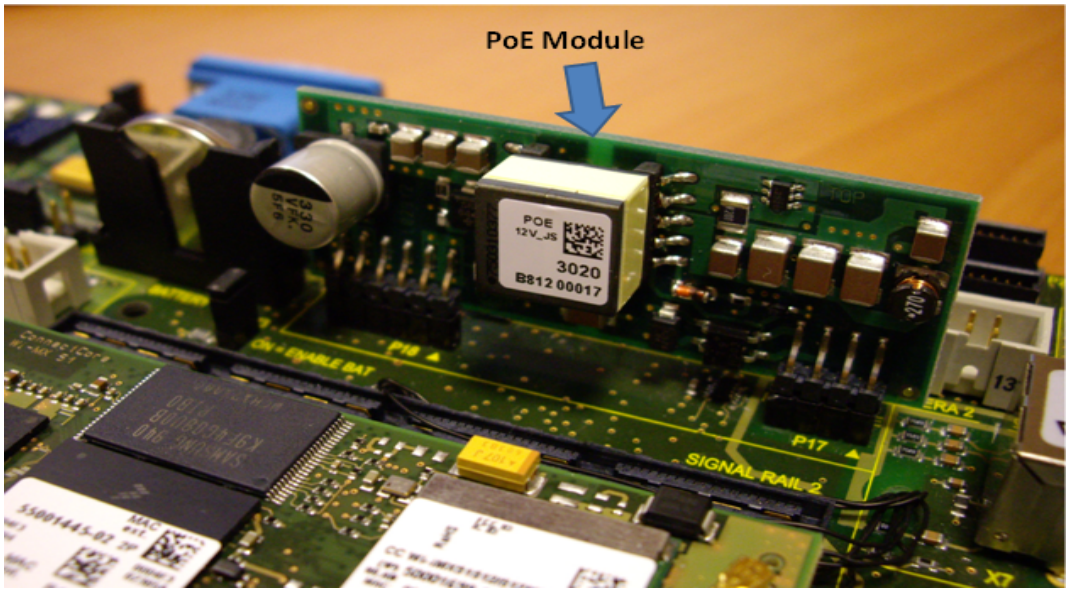
The development board provides two PoE module connectors, P17 and P18, to plug a Digi PoE module (DG-ACC-POE). The PoE module is an optional accessory item that can be plugged on the development board through the two connectors.

- P17, input connector: provides access to the PoE signals from the Ethernet connector
- P18, output connector: provides the output power supply from the PoE module

The PoE module

Plug in the PoE module at a right angle to the development board, as shown in the picture below.

Note the PoE module is part of the optional Digi 802.3af application kit (sold separately, Digi P/N DG-ACC-POE).



PoE connector (power in), P17

The table below provides the pinout of the PoE input connector:

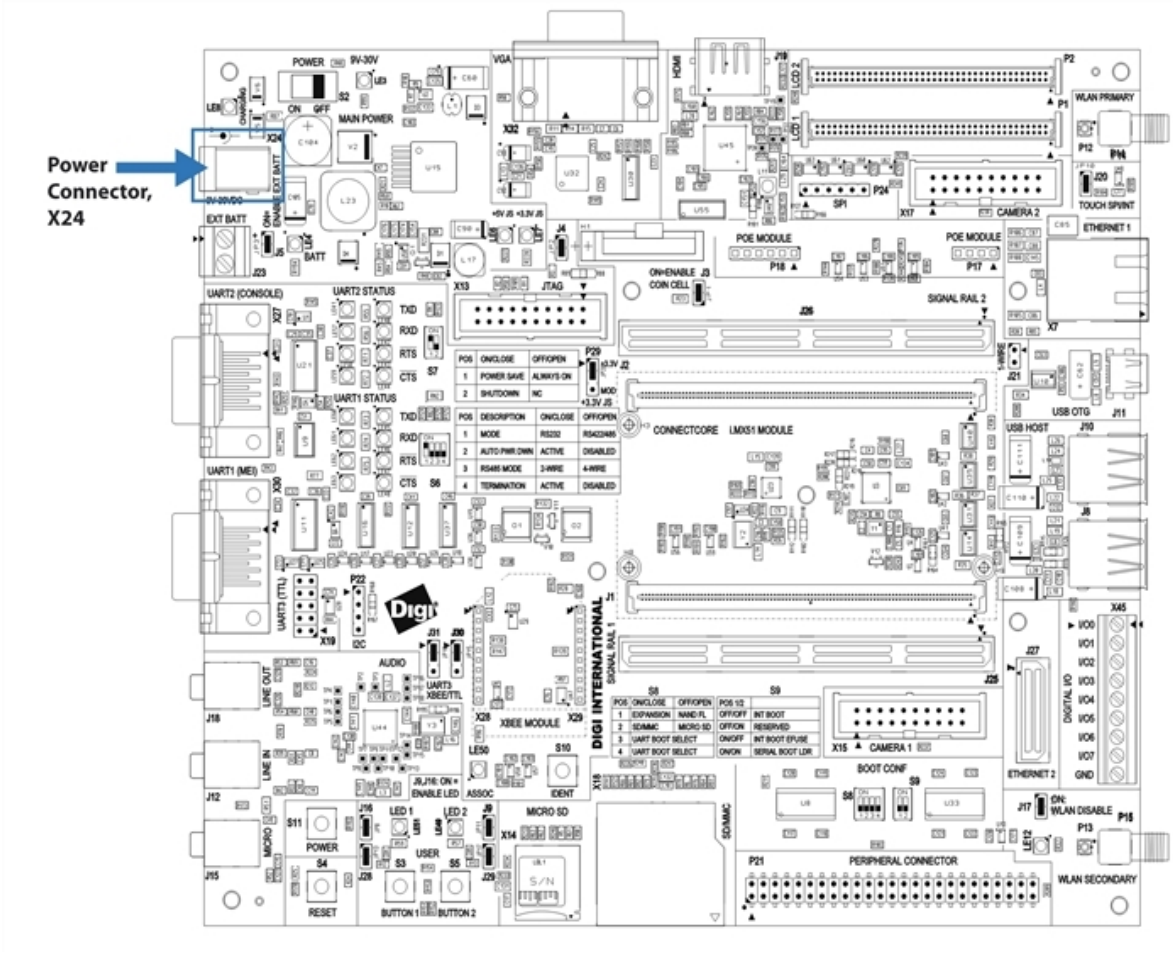
Pin	Signal
1	POE_TX_CT
2	POE_RX_CT
3	POE_RJ45_4/5
4	POE_RJ45_7/8

PoE connector (power out), P18

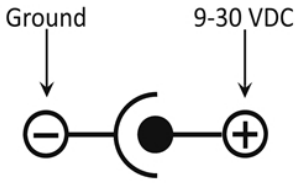
The table below provides the pinout of the PoE output connector:

Pin	Signal
1	+12V_PoE
2	+12V_PoE
3	GND
4	GND
5	PoE_GND
6	PoE_GND

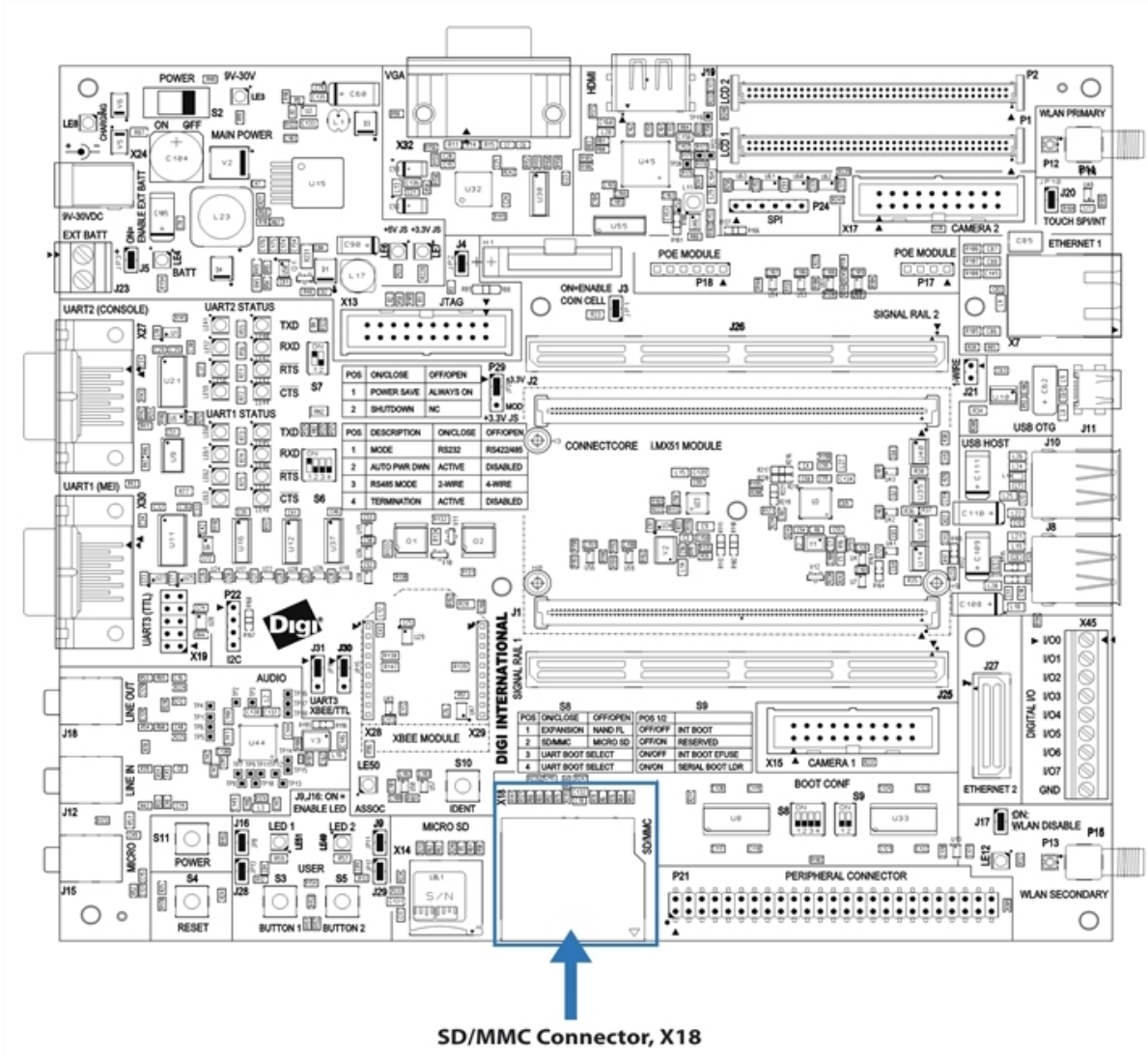
Main power connector



The main power connector (X24) is a barrel connector for the development board's 9-30VDC power supply. The figure below shows the polarity.



SD-card interface



SD/MMC connector, X18

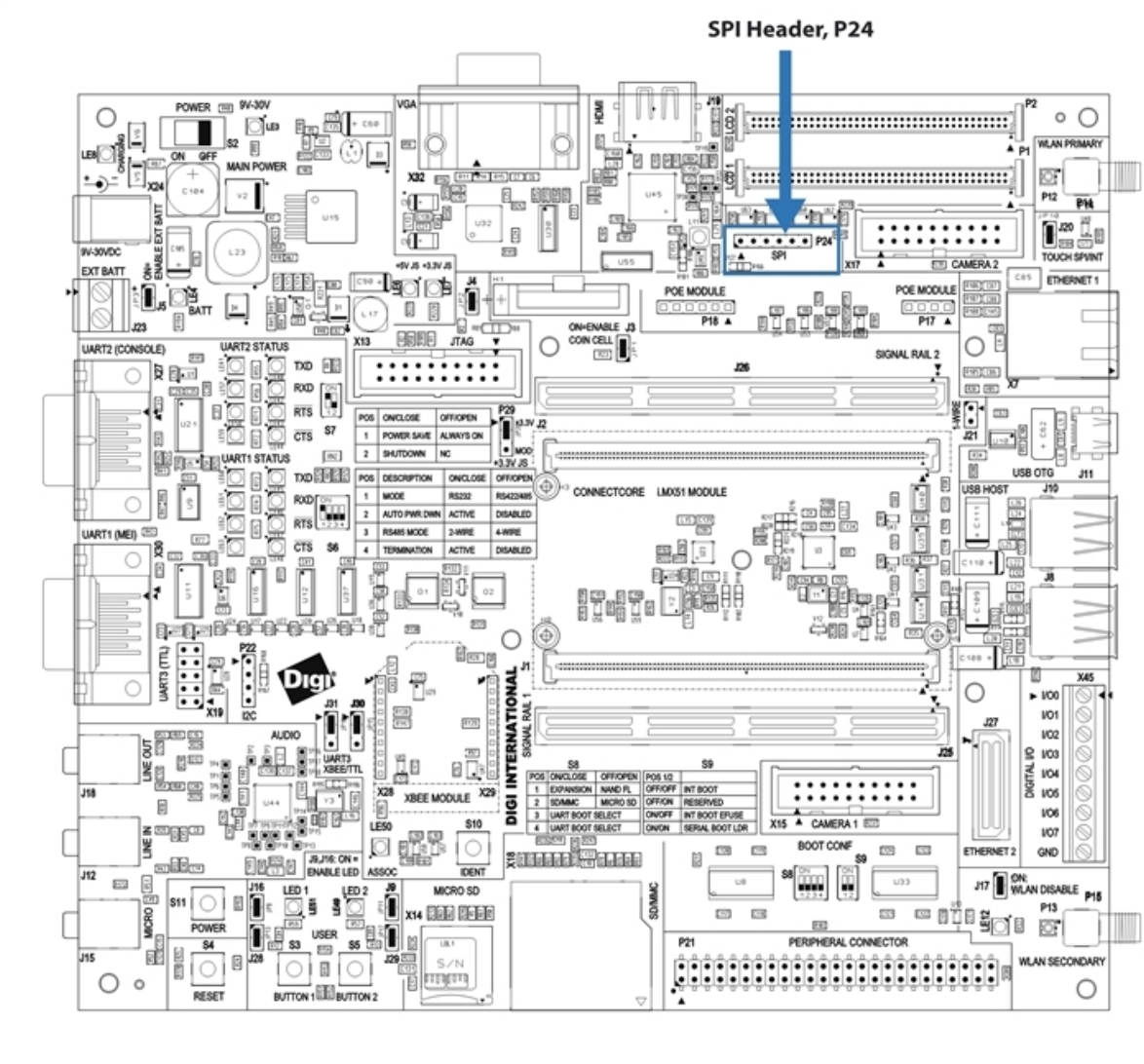
The development board provides one SD/MMC card connector, X18. This interface is connected to the enhanced Secured Digital Host controller 3 (eSDHC3) of the i.MX51 CPU.

The following table provides the pinout of the SD/MMC connector:

Pin	Function
1	SD_DATA3
2	SD_CMD#
3	GND

Pin	Function
4	+3.3V
5	SD_CLK
6	GND
7	SD_DATA0
8	SD_DATA1
9	SD_DATA2
10	-
11	-
12	-
13	-
14	SD_CD#
15	SD_WP#

SPI interface



SPI header, P24

The development board provides access to the SPI interface on the module using the SPI header, P24. This interface is connected to i.MX51 ECSPI1 port.

The SPI bus is connected to the following interfaces on the development board:

Interface	Chip Select
SPI Header	CSPI1_SS1/GPIO4_25
LCD1	GPIO4_26 (*)
LCD2	GPIO4_26 (*)

Interface	Chip Select
(*) the SPI chip select signal for the two LCD interfaces is generated with a logic combination of GPIO4_26 and the touch selection jumper (J20).	

The SPI bus is connected to the following interfaces of the ConnectCore for i.MX51 module.

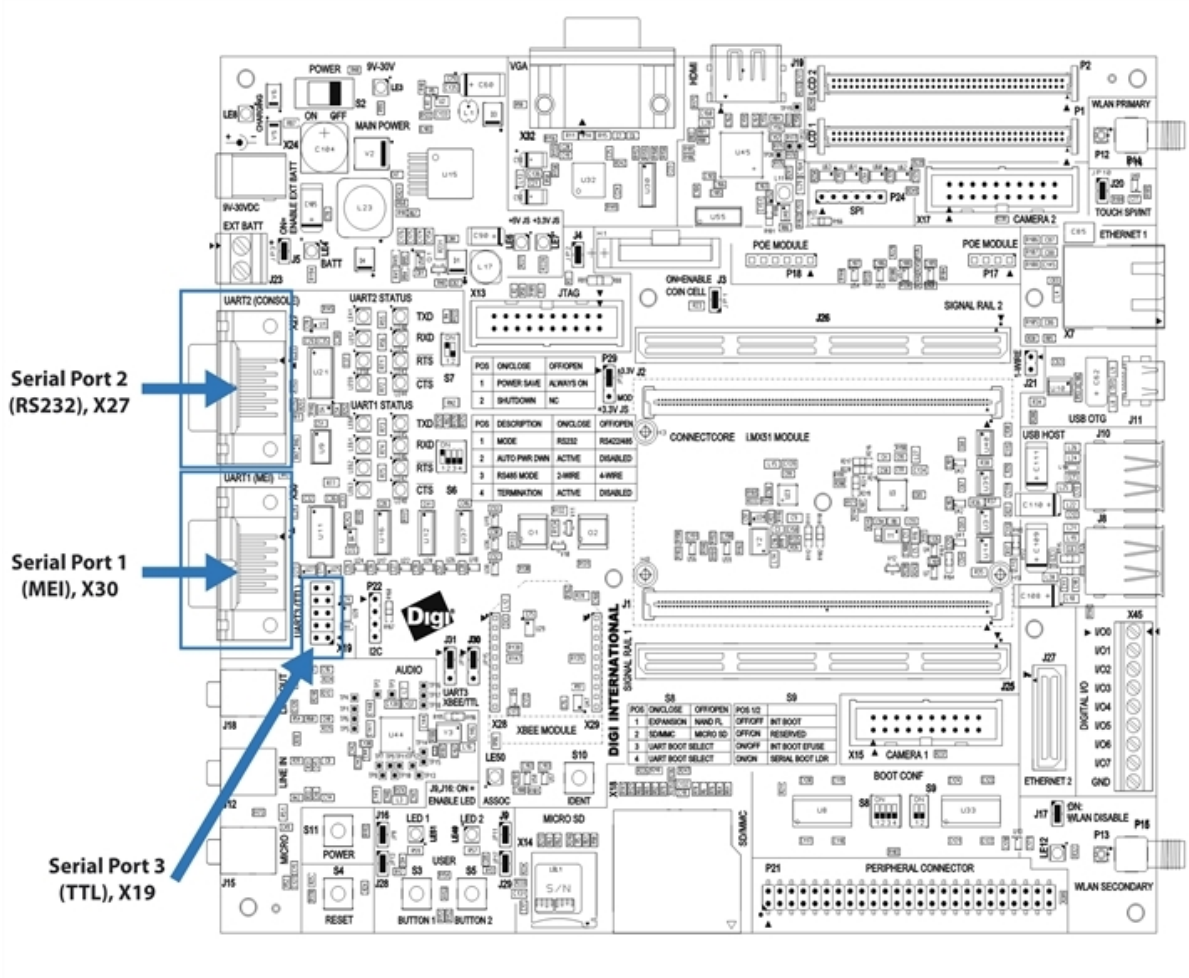
Interface	Chip Select
MC13892 Power Management	CSPI1_SS0/GPIO4_24

The table below provides the pinout of the SPI header:

Pin	Function	Defaults to
1	+2.775V	
2	SPI_MOSI/GPIO4_22	GPIO4_22
3	SPI_MISO/GPIO4_23	GPIO4_23
4	SPI_SCLK/GPIO4_27	GPIO4_27
5	SPI_SS1/GPIO4_25	GPIO4_25
6	GND	

By default, SPI pins are configured as GPIO signals.

UART interface



Serial port 2, RS232, X27

The serial (UART) port 2 connector, X27, is a DB-9 male connector, which is also used as the standard console port. This asynchronous serial port is operating in DTE mode and requires a null-modem cable to connect to a computer serial port.

The serial port 2 interface is connected to i.MX51 UART port 2. The corresponding line driver on the development board can be enabled or disabled using switch S7. Refer to Switches and push-buttons for more information.

Serial port 2 pins are allocated as shown:

Pin	Function	Defaults to
1	NC	-
2	RXD	GPIO1_20

Pin	Function	Defaults to
3	TXD	GPIO1_21
4	NC	-
5	GND	-
6	NC	-
7	RTS#	GPIO1_14
8	CTS#	GPIO1_11
9	NC	-

By default, serial port 2 signals are configured as GPIO signals.

Serial port 1, MEI interface, X30

The serial (UART) port 1 connector, X30, is a DB-9 male connector. This asynchronous serial port is operating in DTE mode and requires a null-modem cable to connect to a computer serial port.

The serial port 1 MEI (multiple electrical interface) interface corresponds to i.MX51 UART port 1. The line drivers are configured using the switch S6. Refer to Switches and push-buttons for more information.

Serial port 1 pins are allocated as shown:

Pin	RS232 Function	RS232 Default	RS485 Function	RS485Default
1	-	-	CTS-	-
2	RXD	GPIO4_28	RX+	GPIO4_28
3	TXD	GPIO4_29	TX+	GPIO4_29
4	-	-	RTS-	-
5	GND	-	GND	-
6	-	-	RX-	-
7	RTS#	GPIO4_30	RTS+	GPIO4_30
8	CTS#	GPIO4_31	CTS+	GPIO4_31
9	-	-	TX-	-

By default, serial port 1 signals are configured as GPIO signals.

Serial port 3, TTL interface, X19

The serial (UART) port 3 interface is a TTL interface connected to a 2x5 pin, 2.54mm connector, X19. The connector supports only TTL level signals.

The serial port 3 interface is connected to i.MX51 UART port 3.

Serial port 3 pins are allocated as shown:

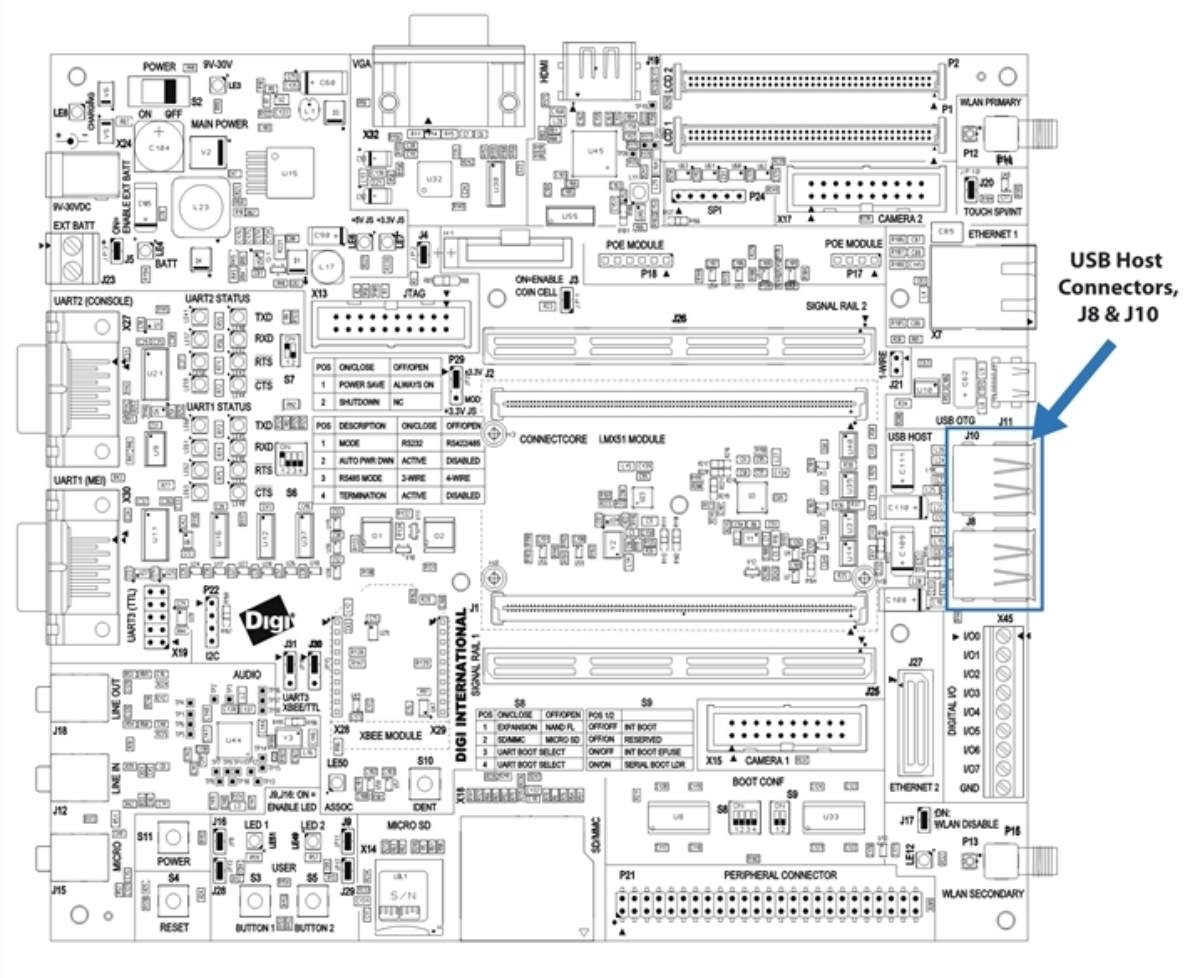
Pin	Function	Defaults to
1	NC	-
2	NC	-
3	RXD	GPIO1_22
4	RTS#	KEY_COL4
5	TXD	GPIO1_23
6	CTS#	KEY_COL5
7	NC	-
8	NC	-
9	GND	-
10	+3.3V	-

By default, serial port 3 signals are configured to their respective GPIO or KEY_COL signals.

Serial port 3 is connected to the X19 connector and to the XBee module socket. Two jumpers (J30 and J31) are used in the development board to select the connector where serial port 3 will be available. Refer to Jumpers for more information.

By default serial port 3 CTS# signal is not connected to X19. A 0Ω resistor, R44, must be manually populated to connect this signal to the X19 connector.

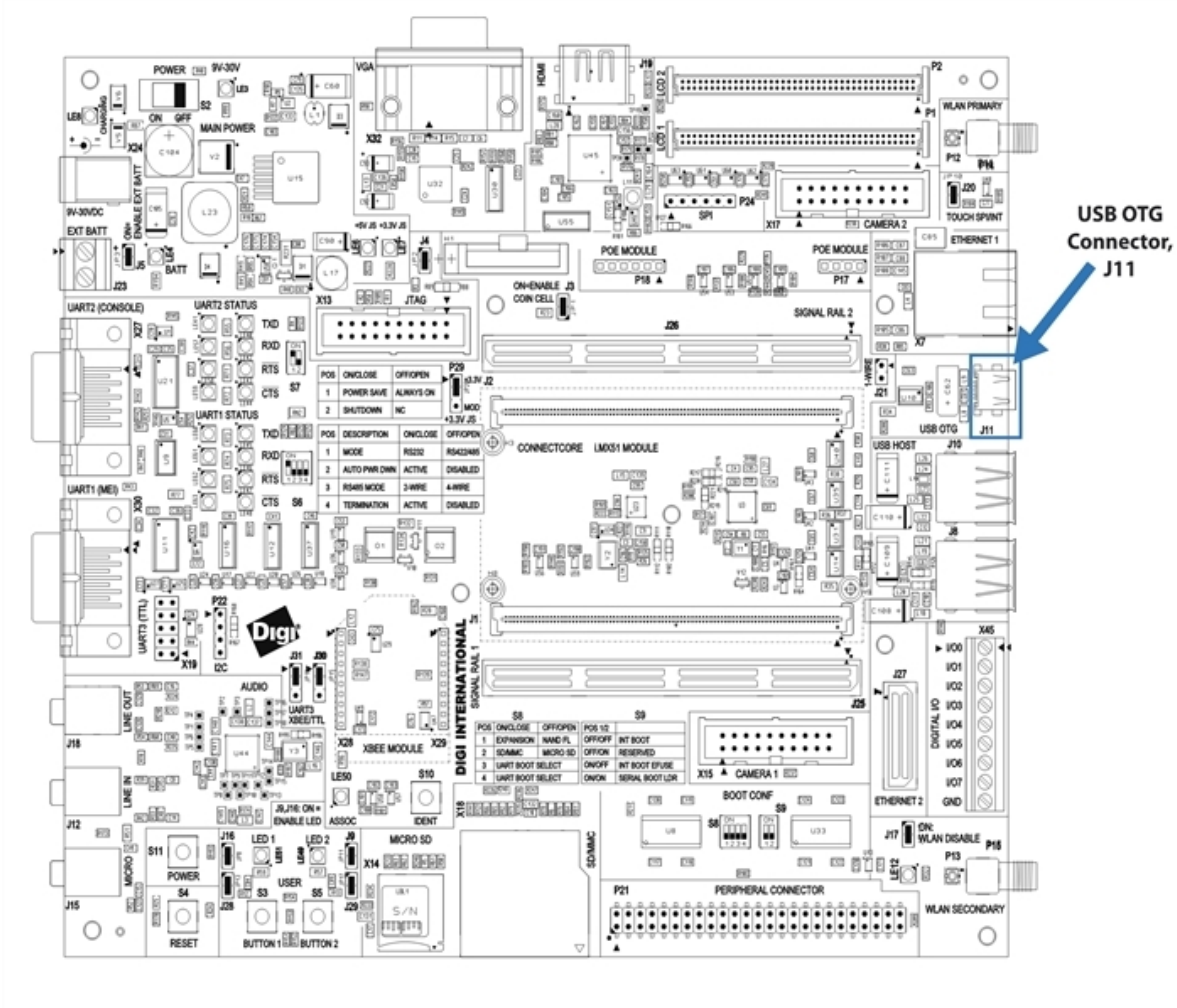
USB host interface



USB host connectors, J8 and J10

The development board provides four standard type A receptacles for a USB host connection. A 4-Port USB hub is used in the development board to convert the USB host port 1 of the module into four USB host ports. The module supports low, full and high speed USB 2.0 connectivity.

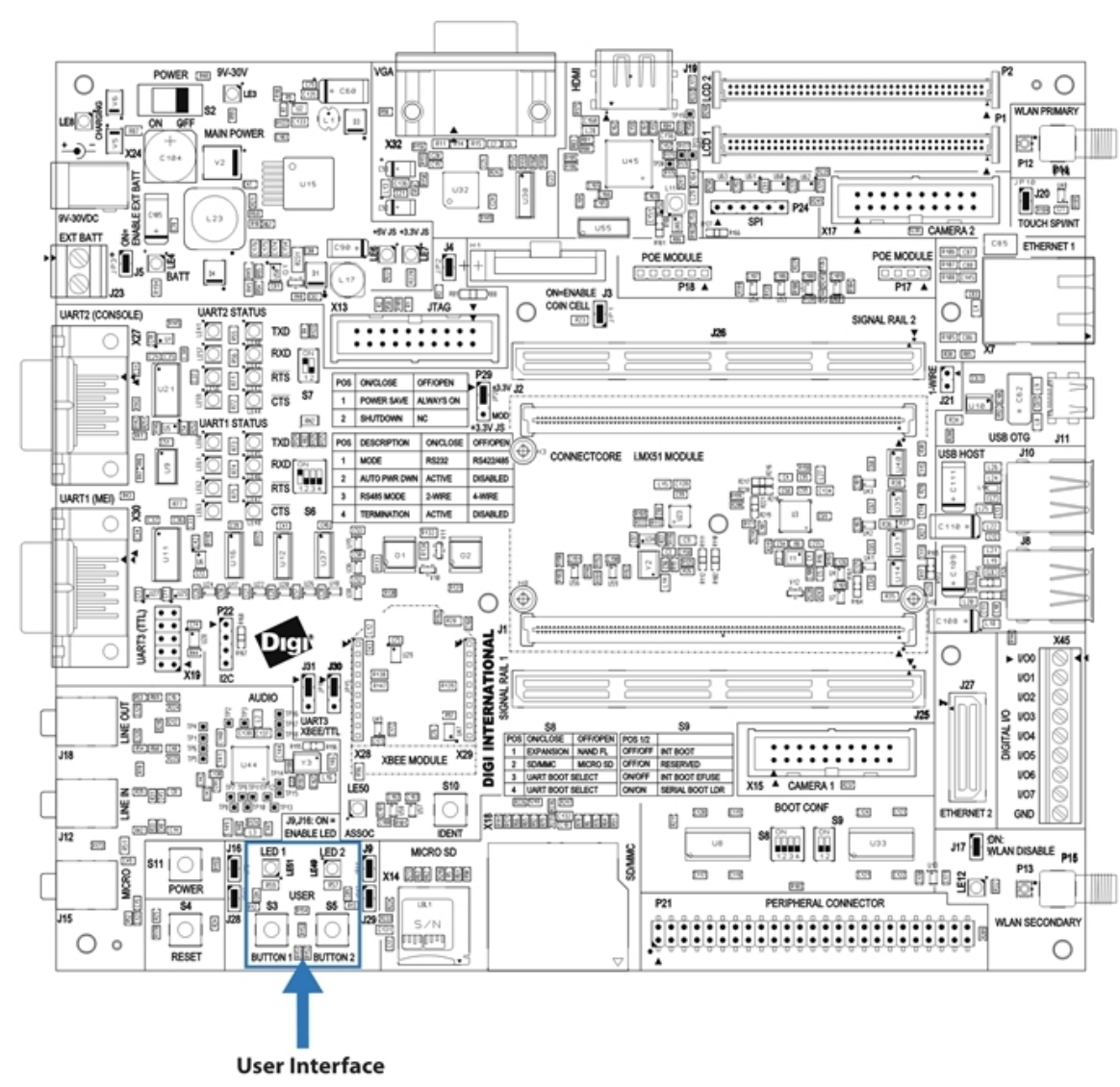
USB OTG interface



USB OTG connector, J11

The development board provides a standard mini-AB type receptacle for a USB OTG connection. The module supports full and high speed USB2.0 connectivity.

User interface



The development board provides two user buttons and two user LEDs connected to GPIO signals of the i.MX51.

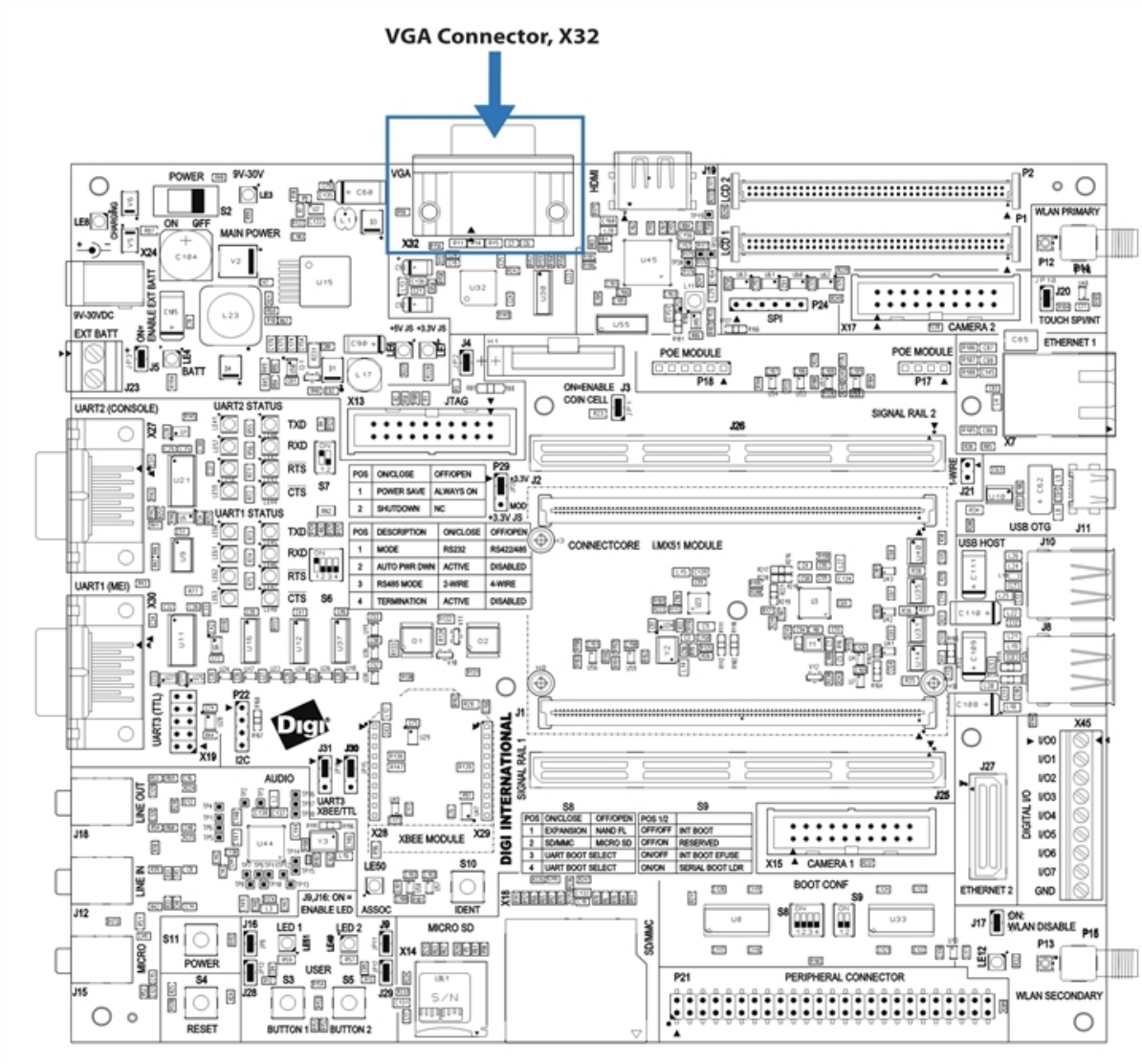
The user buttons and the user LEDs can be enabled or disabled by correctly setting the corresponding jumpers.

The table below shows the GPIO signal assigned to the user interface, and the jumpers used to enable/disable the buttons and LEDs:

Signal	GPIO	Jumper	Comment
USER_BUTTON1	GPIO3_6	J28	10K pull-up to +2.775V on the development board
USER_LED1#	GPIO3_10	J16	

Signal	GPIO	Jumper	Comment
USER_BUTTON2	GPIO1_1	J29	10K pull-up to +2.775V on the development board
USER_LED2#	GPIO3_9	J9	

Analog video interface



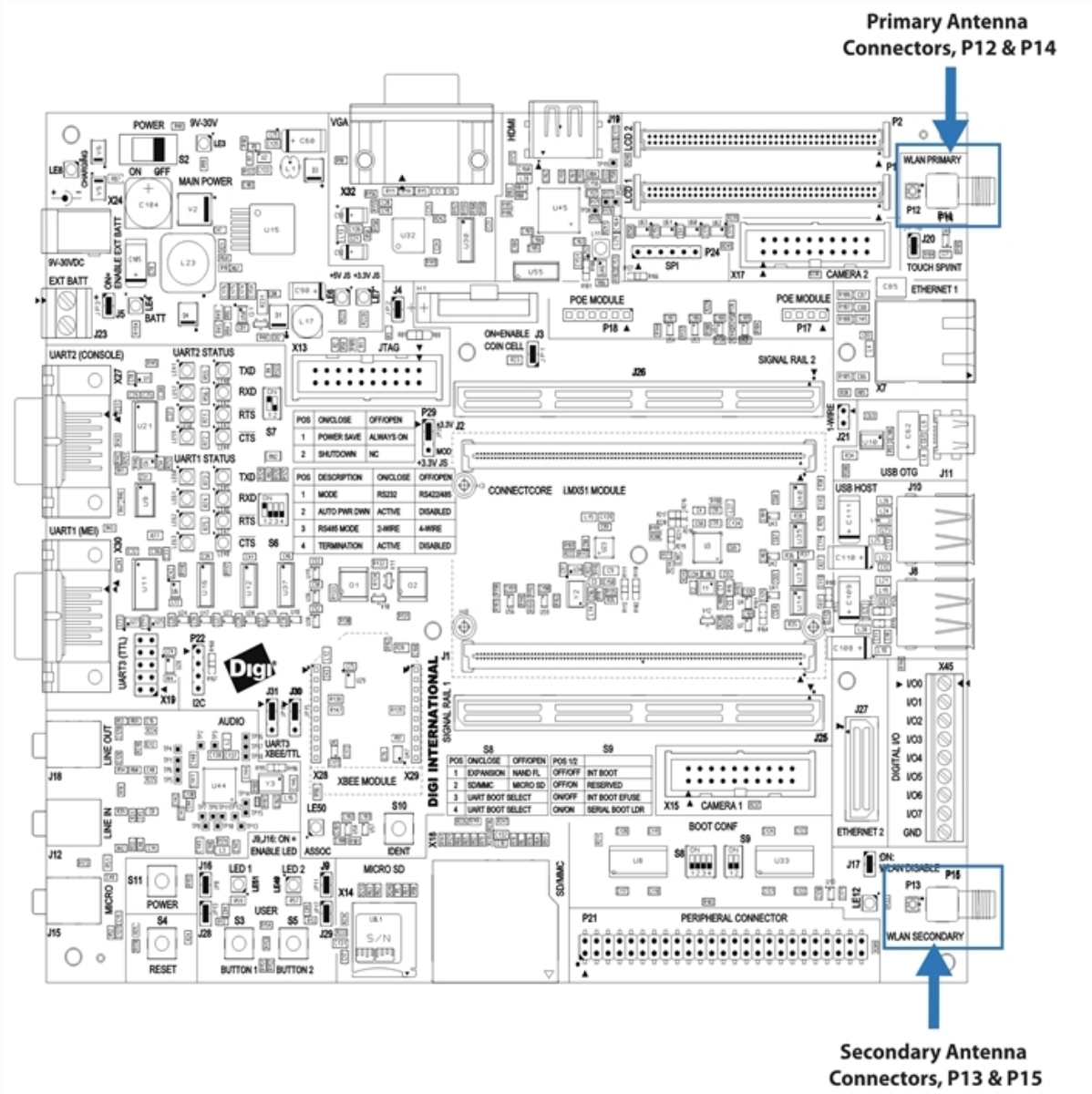
Analog video connector, X32

The development board provides an Analog Video connector. This connector is a 15-pin female connector, labeled X32. The Analog Video interface is connected to the Display 1 interface of the i.MX51 CPU.

The table below shows the pinout of the Analog Video connector.

Pin	Signal
1	VGA_RED
2	VGA_GREEN
3	VGA_BLUE
4	NC
5	GND
6	RED_RETURN
7	GREEN_RETURN
8	BLUE_RETURN
9	NC
10	GND
11	NC
12	NC
13	HSYNC#
14	VSYNC#
15	NC

WLAN interface

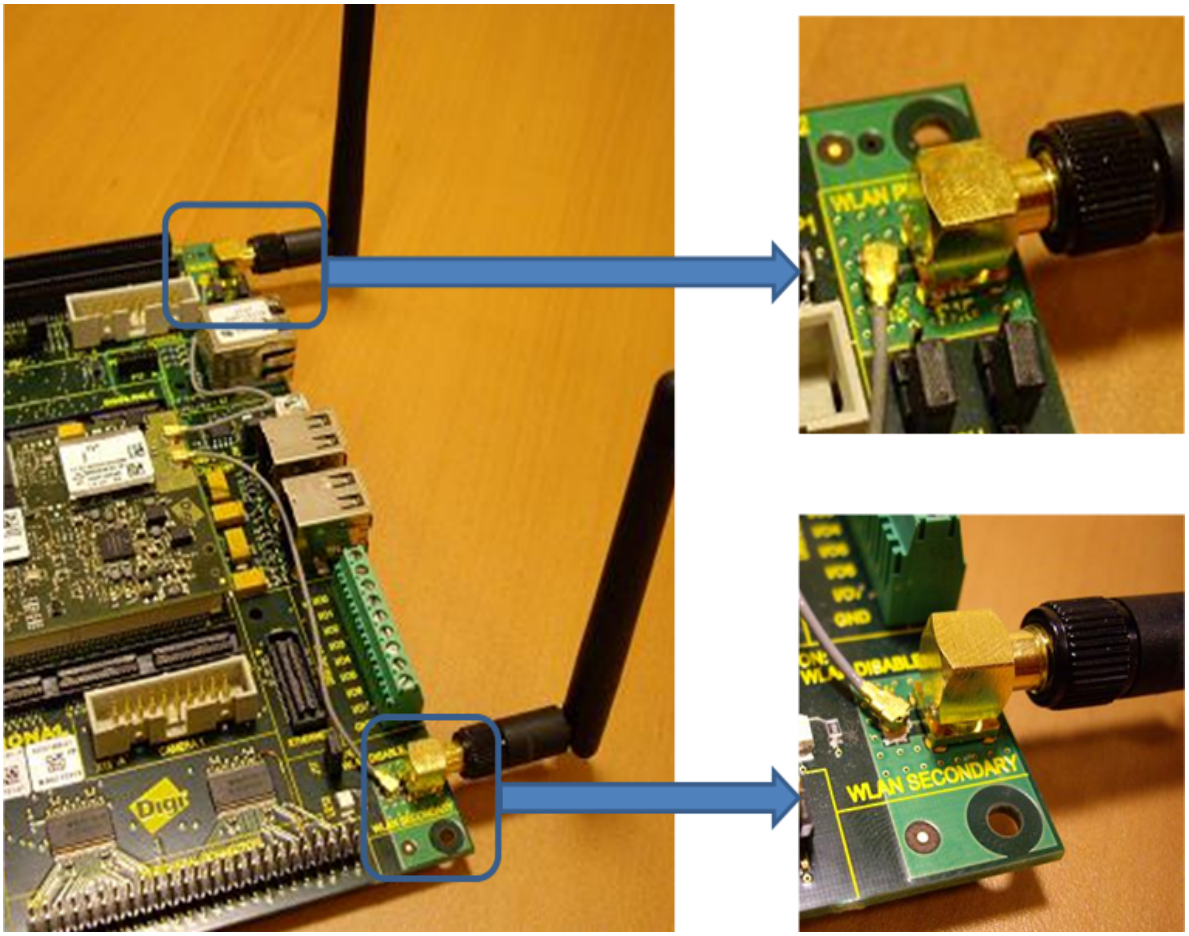


Antenna connectors (WLAN)

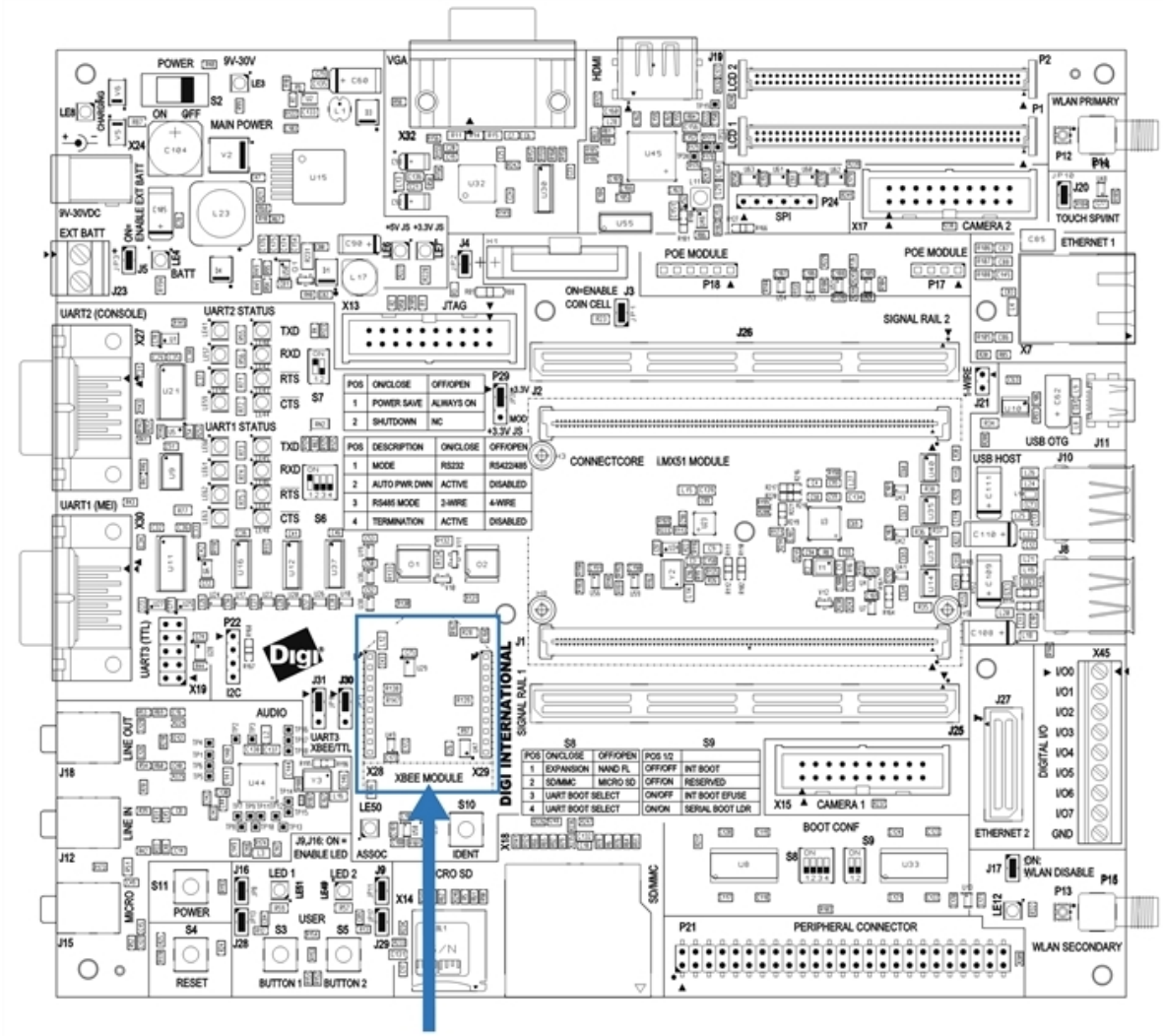
The development board provides the following connectors for the WLAN interface:

- P12 and P13: these two UFL connectors are used to connect the WLAN interface of the ConnectCore for i.MX51 to the development board. Two coaxial cables are used for this connection.
- P14 and P15: these two RP-SMA connectors are used to connect two (primary and secondary) WLAN antennas

The following picture shows the WLAN antenna connections.


WLAN SECONDARY

Digi XBee interface



Digi XBee
Connectors, X28 & X29

Digi XBee module connectors, X28 and X29

The development board provides two 10-pin, 2.0mm connectors, X28 and X29, supporting a Digi XBee module.

The XBee serial port is shared with UART port 3 on the development board. Two jumpers (J30 and J31) are used in the development board to select the connector where serial port 3 will be available. Refer to Jumpers for more information.

The table below shows the pinout of the XBee module connectors.

Pin	Signal	Pin	Signal
X28-1	+3.3V	X29-1	IDENT
X28-2	XBEE_DOUT	X29-2	
X28-3	XBEE_DIN	X29-3	
X28-4	NC	X29-4	
X28-5	XBEE_RESET#	X29-5	XBEE_RTS#
X28-6	-	X29-6	ASSOC
X28-7	-	X29-7	
X28-8	-	X29-8	ON/SLEEP#
X28-9	XBEE_SLEEP_RQ	X29-9	XBEE_CTS#
X28-10	GND	X29-10	

Module specifications

This section provides ConnectCore for i.MX51 module specifications.

Mechanical specifications

Length	82 mm (3.228 inches)
Width:	50 mm (1.968 inches)
Height :	
PCB:	1.40 mm (0.055 inches)
Top side part:	3.60 mm (0.142 inches)
Bottom side part:	2.20 mm (0.087 inches)

Fasteners and appropriate torque

We recommend using a M2x8mm PCB standoff with a slotted cheese head screw, DIN 84, M2x04, 6MM (Digi P/N MA00898) in combination with a flat washer, DIN 125, M2, Nylon 6 (Digi P/N MA01617). Additionally, we recommend the use of a torque key with 10 cNm.

Do not use a standard metal M2 washer.

Environmental specifications

Operating temperature:	600MHz variant: -40° C to +85° C (-40° F to +185° F) 800MHz variant: -20° C to +70° C (-4° F to +158° F)
Storage temperature:	-40° C to +125° C (-40° F to +257° sF)

Network interface

Antenna specifications: 802.11 a/b/g antenna

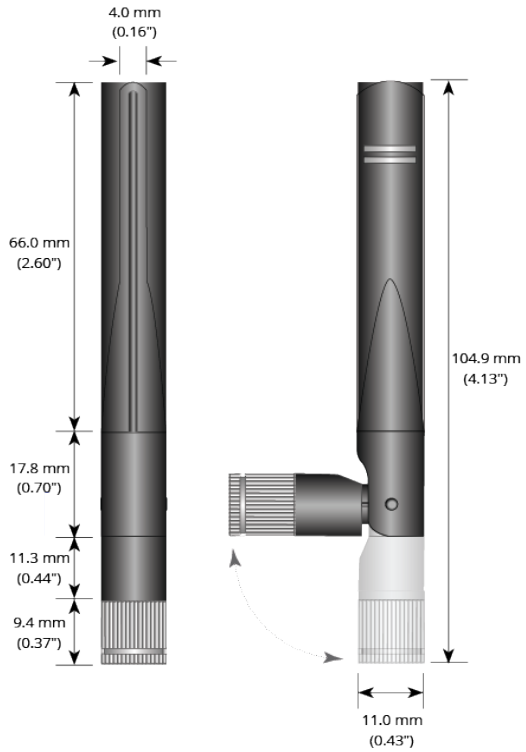
Attributes

Attribute	Band 1	Band 2
Frequency	2.4 ~ 2.4835 GHz	5.15 ~ 6 GHz
Bandwidth	120MHz	875MHz
Wavelength	1/4 Wave	1/4 Wave
Impedance	50 Ohm	50 Ohm
VSWR	< 19 typ. Center	< 19 typ. Center
Connector	RP-SMA	RP-SMA

Attribute	Band 1	Band 2
Gain	2.3dBi	3.6dBi
Dimension	See the measurements in the drawing after this table	
Part Number	ANT-DB1-RAF-RPS	

Dimensions

Note Dimensions are provided for reference purposes only. The actual antenna might vary.



Antenna specification: 802.11b/g antenna

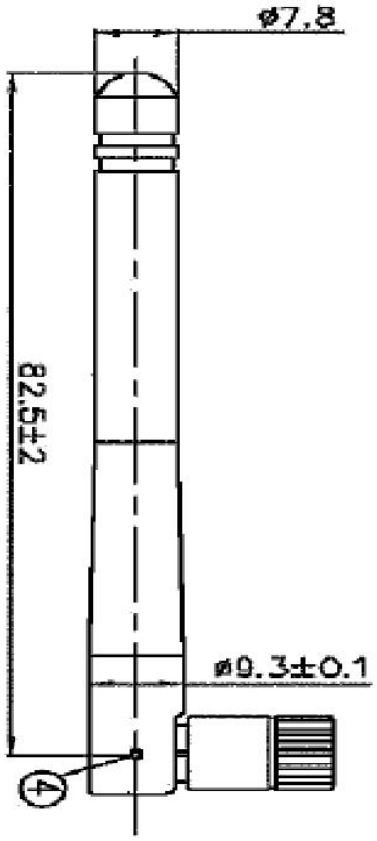
Attributes

Attribute	Property
Frequency	2.4 ~ 2.5GHz
Power Output	2W
DB Gain	2dBi
VSWR	< or = 2.0

Attribute	Property
Dimension	108.5 mm% 10.0mm
Weight	10.5g
Temperature Rating	-40 °to +80° C
Part Number	DG-ANT-20DP-BG

Dimensions

Note Dimensions are provided for reference purposes only. The actual antenna might vary.



Ethernet 1

Standard:	IEEE 802.3/802.3u
Physical layer:	10/100Base
Data rate:	10/100 Mb/s
Mode:	Full or half duplex

Ethernet 2

Standard:	IEEE 802.3/802.3u
Physical layer:	10/100Base
Data rate:	10/100 Mb/s
Mode:	Full or half duplex

WLAN

Standard

- IEEE 802.11a/b/g/e/i/h/j standards
- Single-stream IEEE 802.11n

Frequency band

- 2.400 - 2.500 GHz (Low Band)
- 4.900 - 5.850 GHz (High Band)

Data rates

- 802.11n :6.5, 13, 19.5, 26, 39,52, 58.5, 65 Mb/s
- 802.11a/g :6, 9, 12, 18, 24, 36, 48, 54 Mb/s
- 802.11b :1, 2, 5.5, 11 Mb/s

Media access control

- Dynamic selection of fragment threshold, data rate and antenna depending on the channel statistics
- WPA, WPA2 and WMM support

Wireless medium

- 802.11b/g: Direct Sequence-Spread Spectrum (DSSS) and Orthogonal Frequency Divisional Multiplexing (OFDM)
- 802.11a/n: OFDM

DFS client

- This module supports the DFS Client only between 5.25 - 5.35 GHz and 5.50 - 5.70 GHz bands. It does not support being DFS Master, or can it be connected to an Ad hoc network in these bands.

- This device cannot act as an access point on the non-DFS legacy frequency in the 5.15 and 5.25 GHz bands.

Modulation DSSS

- Differential Binary Shift Keying (DBPSK) @ 1 Mb/s
- Differential Quadrature Phase Shift Keying (DQPSK) @ 2 Mb/s
- Complementary Code Keying (CCK) @ 5.5 Mb/s and 11 Mb/s
- BPSK @ 6 and 9 Mb/s
- QPSK @ 12 and 18 Mb/s
- 16-Quadrature Amplitude Modulation (QAM) @24 and 36 Mb/s
- 64-QAM @ 48 and 54 Mb/s

Frequency bands

- 2.412 to 2.472 GHz (ETSI)
- 2.412 to 2.462 GHz (FCC)
- 5.150 to 5.250 GHz (ETSI) ISM Band 1
- 5.250 to 5.350 GHz (ETSI) ISM Band 2 excluding TPC and DFS Client
- 5.470 to 5.725 GHz (ETSI) ISM Band 3 excluding TPC and DFS Client
- 5.150 to 5.250 GHz (U-NII-1)
- 5.250 to 5.350 GHz (U-NII-2) excluding TPC and DFS Client
- 5.470 to 5.725 GHz (U-NII Worldwide) excluding TPC and DFS Client
- 5.725 to 5.825 GHz (U-NII-3)

Available transmit power settings (typical +- (2 dBm)@25°C)

(Maximum power settings will vary according to individual country regulations.)

- IEEE 802.11b (~16 mW ETSI) (~37 mW FCC 15.247) @ 1, 2, 5.5 and 11 Mb/s
- IEEE 802.11g (~ 10 mW ETSI) (~72 mW FCC 15.247) @ 6, 12, 18, 24, 36 and 54 Mb/s
- IEEE 802.11n 2.4 GHz Band (~12.5 mW ETSI) (~83 mW FCC 15.247)

- IEEE 802.11a & IEEE 802.11n

  (~15mW ETSI)

  (5.150 to 5.250 GHz ~17 mW FCC 15.407)

  (5.250 to 5.350 GHz ~17 mW FCC 15.407)

  (5.470 to 5.725 GHz ~22 mW FCC 15.407)

  (5.725 to 5.850 GHz ~28 mW FCC 15.247)

  @ 6, 12, 18, 24, 36 and 54 Mb/s and

  @ 6.5, 13, 19.5, 26, 39,52, 58.5, 65 Mb/s

Receive sensitivity

Data Rate (bg Mode)	Typical Sensitivity (+ / - 1.5 dBm)
1 Mb/s	-94.0 dBm (< 8% PER)
2 Mb/s	-89.0 dBm (< 8% PER)
11 Mb/s	-86.0 dBm (< 8% PER)
6 Mb/s	-89.0 dBm (< 10% PER)
54 Mb/s	-74.0 dBm (< 10% PER)
645Mb/s	-71.0 dBm (< 10% PER)
Data Rate (a Mode)	Typical Sensitivity (+ / - 1.5 dBm)
6 Mb/s	-88.0 dBm (< 10% PER)
54 Mb/s	-72.0 dBm (< 10% PER)

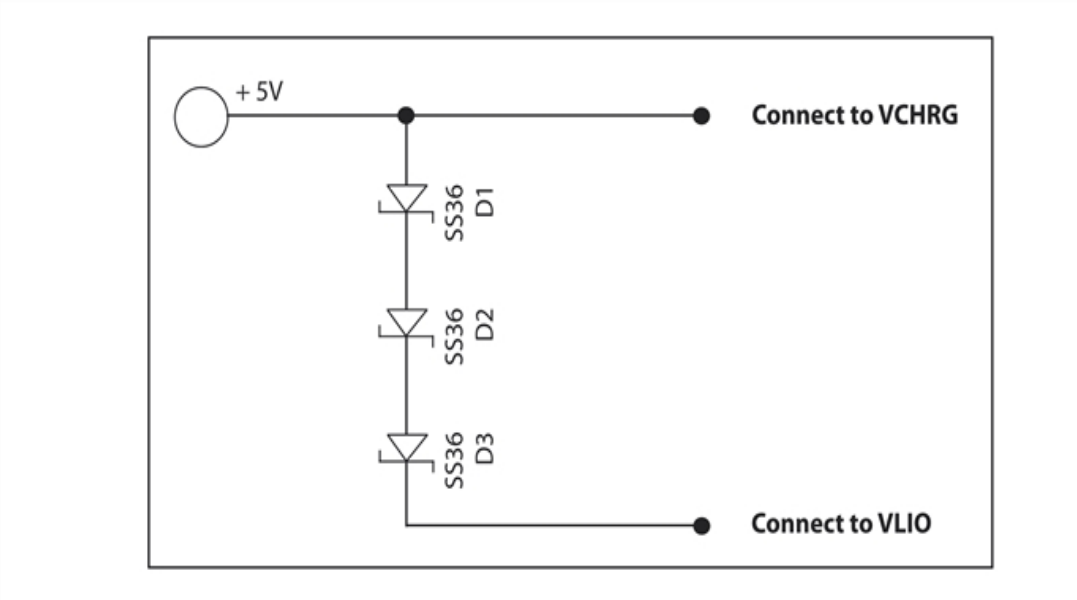
Data Rate (bg Mode)	Typical Sensitivity (+ / - 1.5 dBm)
65 Mb/s	-69.0 dBm (< 10% PER)

Electrical characteristics

Charger vs. battery

The ConnectCore for i.MX51 can be supplied solely either through the battery input or also through the charger input, although the VLIO input is the preferred method. When using solely the charger input, and when no battery is connected to VLIO, the ConnectCore for i.MX51 will not be functional across the entire rated temperature of the product. As an example, when using the product at -20C, the ConnectCore for the i.MX51 will not be functional due to the internals state machine of the module PMIC.

To override this limitation for all instances, you must generate a battery voltage on the carrier board. Different options are available for simulating a battery voltage - below is one example, based on three Schottky diodes in series.



Note When using the charger as unique power source for the ConnectCore for i.MX51 module, the CHRGSE1# (J1.45) pin must be forced low as a charger attach indicator.

Supply voltages

Parameter	Symbol	Min	Typ	Max	Unit
Battery Input	VLIO	3.4	3.7	4.8	V
Charger Input	VCHRG	3.4	5	5.6	V
Coin cell Input for RTC	VCC_COINCELL	2.5	3	3.6	V

Supply current

The following table provides current draw guidance utilizing the power management capabilities of the module. The module variant used for the measurements works at 800MHz, with 512 MB NAND Flash, 512 MB DDR2, dual Ethernet, WLAN, and accelerometer. A Windows Embedded CE kernel with power management capabilities has been used to make the current consumption measurements. A different kernel (Linux or Windows CE) with a different driver configuration will show different current consumption values.

The ConnectCore for i.MX51 module can be powered from an external battery (VLIO) or from a battery charger (VCHRG). Current drawn by the modules is different depending on the supply voltage used. The following tables show the current drawn by the module from the two power supplies.

The current drawn by the module is highly dependent on the number and type of interfaces used. To make some current measurements three different interface configurations have been defined:

Interface Configuration	Interfaces Used
Minimum	Console, Ethernet. +3.3V of development board drawn from external power supply.
Typical	VGA, USB Host (two devices connected), Audio, Ethernet, Console. +3.3V of development board drawn from module.
Maximum	Display1, Display2, Camera1, Camera2, USB OTG, USB Host (four devices connected), Audio, Ethernet, Console, WLAN, SD Card, microSD™ Card. +3.3V of development board drawn from module.

The ConnectCore for i.MX51 supports several power modes. The current drawn by the module is highly dependent on the power modes. To make some current measurements, five different power modes have been defined:

Interface Configuration	Interfaces Used
Full Load	System running at 100% CPU load.
Normal	Normal operating state. User interacting with the device.
User Idle	After a long period of user inactivity some devices are turned off.
System Idle	In this state the user is not using the system, even passively, and devices that are not actively doing work are turned off.
Suspend	This is the sleep state, no threads are running, the CPU is idle, the peripherals are turned off, and the system can wake up only by means of hardware wake-source interrupt.

The tables below show the current drawn by the module for the different power modes and the different interface configurations.

On-module power supplies

The following table provides the on-module power supplies available through the module connectors, which can be used to supply the components integrated on a customer baseboard.

Supply	Source	Output Voltage	Load Capacity	Off-module Available Current	Comments
+2.775V	PMIC VIOHI LDO	+2.775V	100mA max	50mA max	Used on module to power IPU, Peripheral interfaces, Accelerometer, I^2C, Ethernet PHY, and bootstraps
+1.8V	PMIC VGEN3 LDO	+1.8V	250mA max	250mA max	

Supply	Source	Output Voltage	Load Capacity	Off-module Available Current	Comments
+3.3V	DC/DC Converter	+3.3V	1.2A max	400mA max (*)	Used on module to power WLAN, Ethernet Controller and Ethernet PHY
+3.15V	PMIC VGEN2 LDO	+3.15V	350mA max	300mA max	Used on module to power NAND Flash SD1 and fuse interface
SWBST	PMIC +5V Boost Switcher	+5V	300mA max	300mA max	
(*)The off-module available current for the wired variant modules is 800mA.					

I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O and High-Speed General Purpose I/O (GPIOxx/HSGPIOxx)
- Low Voltage I/O (LVIO)
- Ultra High Voltage I/O (UHVIOxx)
- WLAN
- PMIC_GPO, PMIC_PWRON, PMIC_STDBY, PMIC_INT, PMIC_PWDRV, PMIC_SE, PMIC_CHRGLED, and PMIC_LED
- Ethernet (ETH)
- Analog RGB
- ADC subsystem (ADIN)
- Digital and analog USB (DIG_USB, AN)USB)

The I/O type associated to each I/O signal of the module is shown in Module pinout.

The following table shows the General Purpose I/O and High-Speed General Purpose I/O (GPIOxx/HSGPIOxx) DC parameters. The “xx” reference signifies the supply voltage level.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD xx = 18 xx = 27 xx = 33	 1.65 2.5 3.0	 1.8 2.775 3.3	 1.95 3.1 3.6	V
High-level output voltage	Voh (Vol USB)	VDD-0.15 VDD-0.43	- -	VDD+0.3 VDD+0.3	V
Low-level output voltage	Vol (Vol USB)	- -	 --	0.15 0.43	V

Parameter	Symbol	Min	Typ	Max	Unit
High-level output current	Ioh - Low drive - Medium drive - High drive - Max drive	 -1.9 -3.7 -5.2 -5.6	-	-	mA
Low-level output current	Iol - Low drive - Medium drive - High drive - Max drive	 1.9 3.7 5.2 5.6	-	-	mA
High-level input voltage	VIH	0.7 x VDD	-	VDD	V
Low-level input voltage	VIL	0	-	0.3 x VDD	V
Input Current (no/pull)	Iin	-	-	2	µA
Input Current (22kΩ/pull-up)	Iin	-	-	161	µA
Input Current (47kΩ/pull-up)	Iin	-	-	76	µA
Input Current (100kΩ/pull-up)	Iin	-	-	36	µA
Input Current (100kΩ/pull-down)	Iin	-	-	36	µA
Keeper circuit resistance	-	-	17	-	kΩ
Output driver impedance	Rout - Low drive - Medium drive - High drive - Max drive	 80 40 27 20	 104 52 35 26	 250 125 83 62	Ω

The following table shows the LVIO DC parameters.

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	1.65	1.8	1.95	V
High-level output voltage	Voh	VDD-0.15	-	-	V
Low-level output voltage	Vol	-	-	0.15	V
High-level output current	Ioh - Low drive - Medium drive - High drive - Max drive	 -2.1 -4.2 -6.3 -8.4	-	-	mA
Low-level output current	Iol - Low drive - Medium drive - High drive - Max drive	 2.1 4.2 6.3 8.4	-	-	mA

Parameter	Symbol	Min	Typ	Max	Unit
High-level input voltage	VIH	0.7 x VDD	-	VDD	V
Low-level input voltage	VIL	0	-	0.3 x VDD	V
Input Current (no/pull)	Iin	-	-	1	µA
Input Current (22kΩ/pull-up)	Iin	-	-	161	µA
Input Current (47kΩ/pull-up)	Iin	-	-	76	µA
Input Current (100kΩ/pull-up)	Iin	-	-	36	µA
Input Current (100kΩ/pull-down)	Iin	-	-	36	µA
Keeper circuit resistance	-	-	17	-	kΩ
Output driver impedance	Rout - Low drive - Medium drive - High drive - Max drive	 80 40 27 20	 150 75 51 38	 250 125 83 62	Ω

The following table shows the Ultra-High Voltage I/O (UHVIOxx) DC parameters. The “xx” reference signifies the supply voltage level.

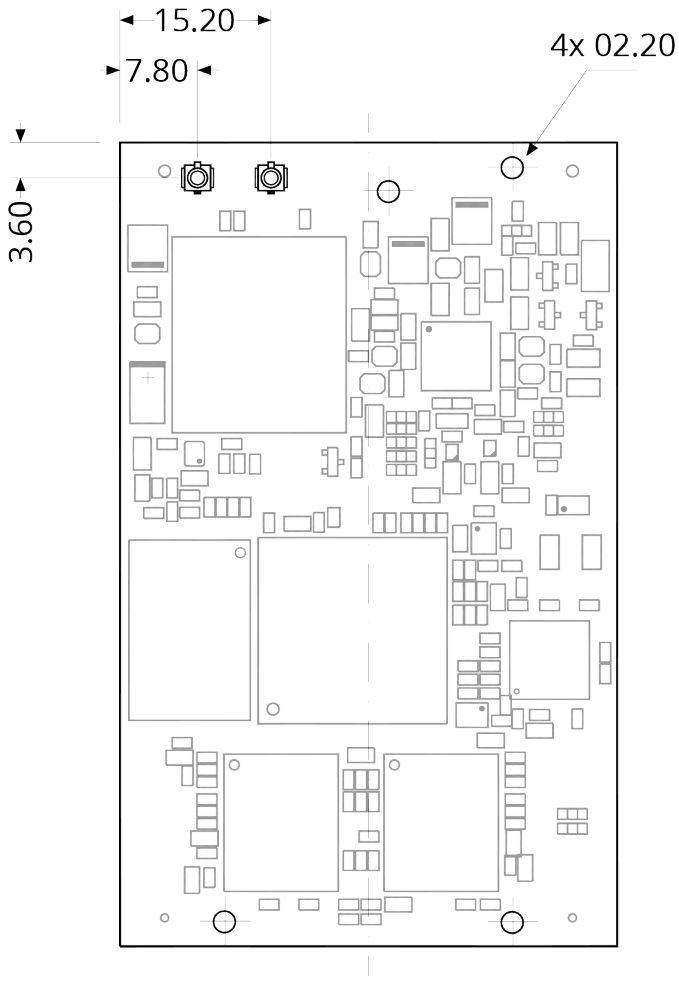
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD xx = 31 xx = 33	 3.0 3.0	 3.15 3.3	 3.6 3.6	V
High-level output voltage	Voh (USB, WLAN)	VDD-0.15 VDD-0.43	- -	VDD-0.15 VDD-0.43	V
Low-level output voltage	Vol (USB, WLAN)	- -	 --	0.15 0.43	V
High-level output current	Ioh - Low drive - Medium drive - High drive	 -5.1 -10.2 -15.3	-	-	mA
Low-level output current	Iol - Low drive - Medium drive - High drive	 5.1 10.2 15.3	-	-	mA
High-level input voltage	VIH	0.7 x VDD	-	VDD	V
Low-level input voltage	VIL	0	-	0.3 x VDD	V
Input Current (no/pull)	Iin	-	-	10	µA
Input Current (22kΩ/pull-up)	Iin	-	-	202	µA

Parameter	Symbol	Min	Typ	Max	Unit
Input Current (75kΩ/pull-up)	Iin	-	-	61	µA
Input Current (100kΩ/pull-up)	Iin	-	-	47	µA
Input Current (360kΩ/pull-down)	Iin	-	-	5.7	µA
Keeper circuit resistance	-	-	17	-	kΩ
Output driver impedance	Rout - Low drive - Medium drive - High drive	 114 57 38	 135 67 45	 206 103 69	Ω

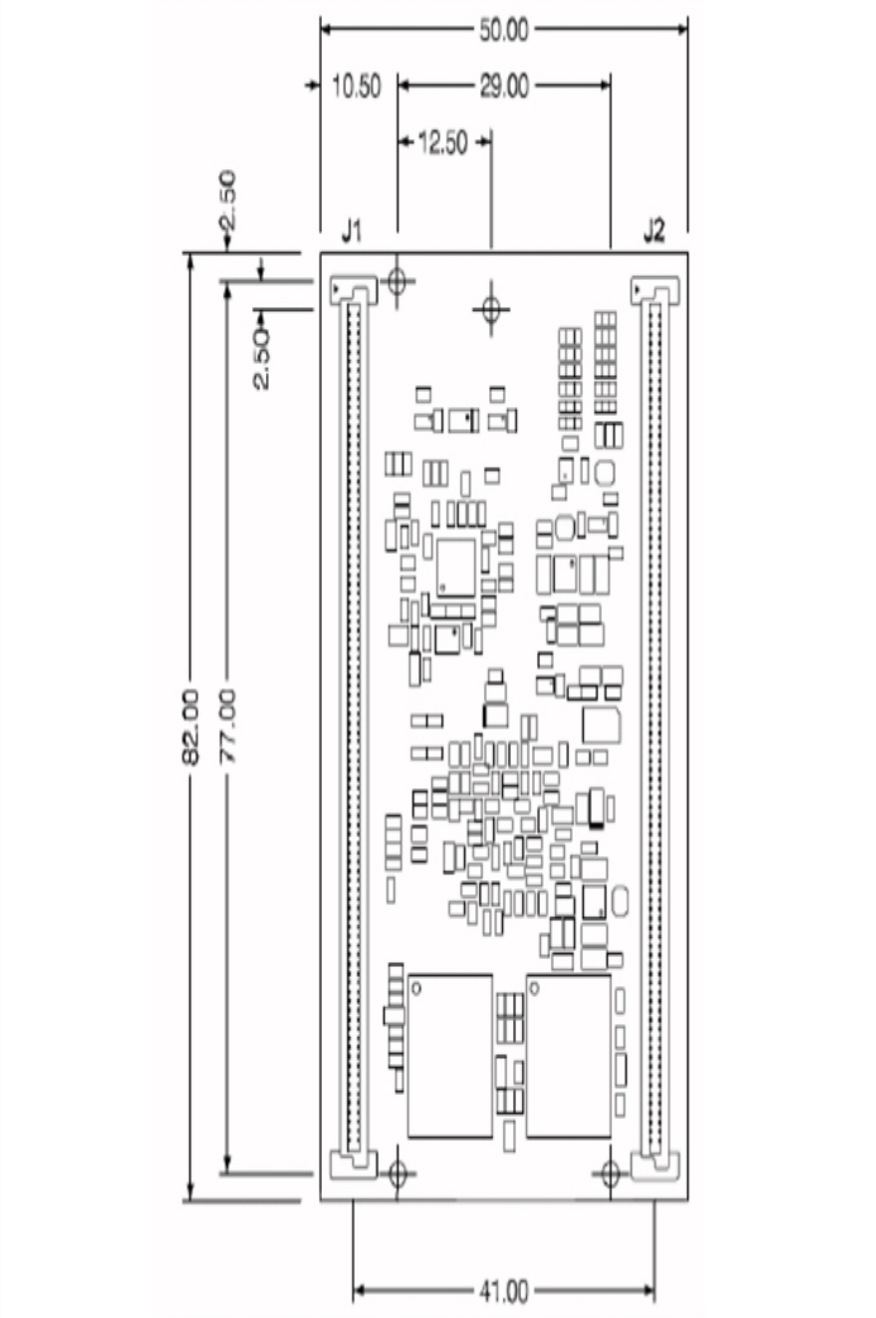
Module dimensions

This section shows the dimensions of the ConnectCore for i.MX51 module, dimensions are in millimeters.

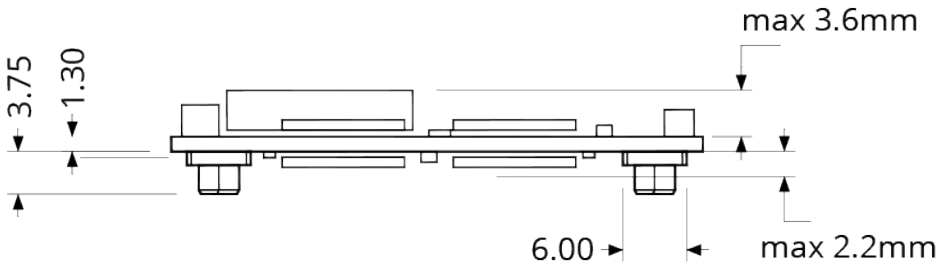
Top view



Bottom view



Side view



Connectors

The ConnectCore for i.MX51 module uses two Berg/FCI connectors. The following table shows the reference number of the connectors used on the module and the reference number of the connectors used in the development board. The mated height of the module and the development board is 5mm.

Device	Berg/FCI Connector
ConnectCore for i.MX51 module	61082-181409LF
ConnectCore for i.MX51 development board	61083-184409LF

Regulatory information

The ConnectCore for i.MX51 product complies with the following standards.

Federal Communication (FCC) regulatory information (USA only)

Radio Frequency Interface (RFI) (FCC 15.105)

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet that is on a circuit different from the receiver.
- Consult the dealer or an experienced radio/TV technician for help.

Labeling Requirements (FCC 15.19)

This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

If the FCC ID is not visible when installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module FCC ID.

RF exposure

RF Exposure considerations require that a 20cm separation distance between users and the installed antenna location shall be maintained at all times when the module is energized. OEM installers must consider suitable module and antenna installation locations in order to assure this in 20cm separation, and end users be also be advised to the requirement.

Modifications (FCC 15.21)

Changes or modifications to this equipment not expressly approved by Digi may void the user's authority to operate this equipment.

Industry Canada

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the Radio Interference Regulations of the Canadian Department of Communications.

Le present appareil numerique n'emet pas de bruits radioelectriques depassant les limites applicables aux appareils numeriques de la class B prescrites dans le Reglement sur le brouillage radioelectrique edicte par le ministere des Communications du Canada.

The maximum antenna gain permitted in the bands 5250-5350 MHz and 5470-5725 MHz to comply with the e.i.r.p limit is, according to RSS-210 section A9.2(2)

- 250mW conducted power
- 1.0W max EIRP

This limit is met with the highest gain antenna listed, antennafactor ANT-DB1-RAF-RPS.

The maximum antenna gain permitted in the band 5725-5825 MHz to comply with the e.i.r.p limit specified for non point-to-point operation is, according to RSS-210 section A9.2(3):

- 1W conducted power
- 4.0W max EIRP

This limit is met with the highest gain antenna listed,antennafactor ANT-DB1-RAF-RPS.

OEM installers and users are cautioned to take note that high-power radars are allocated as primary users (meaning they have priority) of the bands 5250-5330 MHz and 5650-5850 MHz and these radars could cause interference and /or damage to devices operating in these frequency bands.

Indoor/outdoor

When the ConnectCore for i.MX51 module is installed in devices that can be used outdoors, the channels in the band 5150-5250 MHz must be disabled to comply with US and Canadian regulatory requirements. The OEM users are encouraged to inform end users of this restriction as well.

Japan certification

この製品は、周波数帯域 5.15 ~ 5.35 GHz で動作しているときは、
屋内においてのみ使用可能です。

This device has been granted a designation number by Ministry of Internal Affairs and Communications according to:
Ordinance concerning Technical Regulations Conformity Certification etc. of Specified Radio Equipment (特定無線設備の技術基準適合証明等に関する規)

Article 2 clause 1 item 19
Approval n°: 202WW09115541
Article 2 clause 1 item 19 (2)
Approval n°: 202GZ09115541
Article 2 clause 1 item 19 (3)
Approval n°: 202XW09115541
Article 2 clause 1 item 19 (3) (2)

Approval n°: 202YW09115541

This device should not be modified (otherwise the granted designation number will be invalid).

Declaration of Conformity (DoC)

Digi has issued Declarations of Conformity for the ConnectCore for i.MX51 concerning emissions, EMC, and safety. For more information, see www.digi.com/resources/certifications.

Important note

Digi customers assume full responsibility for learning and meeting the required guidelines for each country in their distribution market. Refer to the radio regulatory agency in the desired countries of operation for more information.

CE mark (Europe)

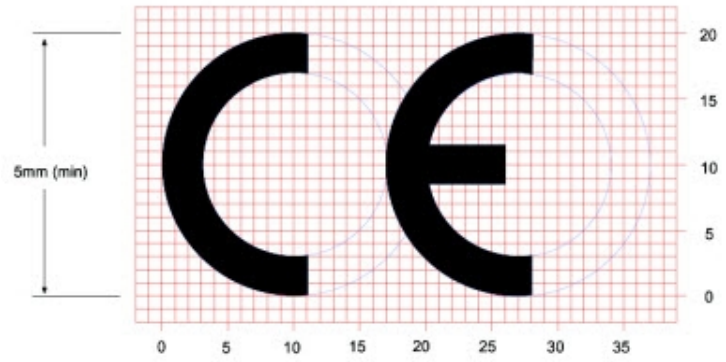
The ConnectCore for i.MX51 is certified for use in several European countries. For information, visit www.digi.com/resources/certifications.

If the ConnectCore for i.MX51 is incorporated into a product, the manufacturer must ensure compliance of the final product with articles 3.1a and 3.1b of the RE Directive (Radio Equipment Directive). A Declaration of Conformity must be issued for each of these standards and kept on file as described in the RE Directive (Radio Equipment Directive). Furthermore, the manufacturer must maintain a copy of the ConnectCore for i.MX51 user manual documentation and ensure the final product does not exceed the specified power ratings, antenna specifications, and/or installation requirements as specified in the user manual.

OEM labeling requirements

The 'CE' marking must be affixed to a visible location on the OEM product.

CE labeling requirements



The CE mark shall consist of the initials “CE” taking the following form:

- If the CE marking is reduced or enlarged, the proportions given in the above graduated drawing must be respected.
- The CE marking must have a height of at least 5mm except where this is not possible on account of the nature of the apparatus.
- The CE marking must be affixed visibly, legibly, and indelibly.

International EMC standards

The ConnectCore for i.MX51 meets the following standards:

Standards	
Emissions	FCC Part 15 Subpart B IS-003
Immunity	EN 55022 EN 55024
Safety	UL 60950-1 CSA C22.2, No. 60950-1 EN 60950-1

Maximum power and frequency specifications

Maximum power	Associated frequencies
88 mW	13 overlapping channels each 22MHz wide and spaced at 5MHz. Centered at 2.412 to 2.472MHz.
28 mW	165 overlapping channels each 22 or 40MHz wide and spaced at 5MHz. Centered at 5180 to 5825MHz.