EVALUATION KIT AVAILABLE

MAX2021

High-Dynamic-Range, Direct Up-/Downconversion 650MHz to 1200MHz Quadrature Mod/Demod

General Description

The MAX2021 low-noise, high-linearity, direct upconversion/downconversion quadrature modulator/demodulator is designed for RFID handheld and portal readers, as well as single and multicarrier 650MHz to 1200MHz GSM/EDGE, cdma2000®, WCDMA, and iDEN® base-station applications. Direct conversion architectures are advantageous since they significantly reduce transmitter or receiver cost, part count, and power consumption as compared to traditional IF-based double conversion systems.

In addition to offering excellent linearity and noise performance, the MAX2021 also yields a high level of component integration. This device includes two matched passive mixers for modulating or demodulating in-phase and quadrature signals, two LO mixer amplifier drivers, and an LO quadrature splitter. On-chip baluns are also integrated to allow for single-ended RF and LO connections. As an added feature, the baseband inputs have been matched to allow for direct interfacing to the transmit DAC, thereby eliminating the need for costly I/Q buffer amplifiers.

The MAX2021 operates from a single +5V supply. It is available in a compact 36-pin TQFN package (6mm x 6mm) with an exposed pad. Electrical performance is guaranteed over the extended -40°C to +85°C temperature range.

Applications

RFID Handheld and Portal Readers

Single and Multicarrier WCDMA 850 Base Stations

Single and Multicarrier cdmaOne™ and cdma2000 Base Stations

GSM 850/GSM 900 EDGE Base Stations

Predistortion Transmitters and Receivers

WiMAX Transmitters and Receivers

Fixed Broadband Wireless Access

Military Systems

Microwave Links

Digital and Spread-Spectrum Communication Systems

Video-on-Demand (VOD) and DOCSIS Compliant Edge QAM Modulation

Cable Modem Termination Systems (CMTS)

Features

- **650MHz to 1200MHz RF Frequency Range**
- **Scalable Power: External Current-Setting Resistors Provide Option for Operating Device in Reduced-Power/Reduced-Performance Mode**
- **36-Pin, 6mm x 6mm TQFN Provides High Isolation in a Small Package**

Modulator Operation:

- **Meets 4-Carrier WCDMA 65dBc ACLR**
- **+21dBm Typical OIP3**
- **+58dBm Typical OIP2**
- **+16.7dBm Typical OP_{1dB}**
- **-32dBm Typical LO Leakage**
- **43.5dBc Typical Sideband Suppression**
- **-174dBm/Hz Output Noise Density**
- **DC to 550MHz Baseband Input Allows a Direct Launch DAC Interface, Eliminating the Need for Costly I/Q Buffer Amplifiers**
- **DC-Coupled Input Allows Ability for Customer Offset Voltage Control**

Demodulator Operation:

- **+35.2dBm Typical IIP3**
- **+76dBm Typical IIP2**
- **> 30dBm IP_{1dB}**
- **9.2dB Typical Conversion Loss**
- **9.3dB Typical NF**
- **0.06dB Typical I/Q Gain Imbalance**
- **0.15° I/Q Typical Phase Imbalance**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2021ETX+	-40°C to +85°C	36 TQFN-EP* (6mm x 6mm)
MAX2021ETX+T	-40°C to +85°C	36 TQFN-EP* (6mm x 6mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and reel.

cdma2000 is a registered certification mark and registered service mark of the Telecommunications Industry Association.
iDEN is a registered trademark of Motorola Trademark Holdings, LLC.
cdmaOne is a trademark of CDMA Development Group.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-3918; Rev 2; 4/13

ABSOLUTE MAXIMUM RATINGS

VCC_ to GND .....-0.3V to +5.5V
BBI+, BBI-, BBQ+, BBQ- to GND.....-3.5V to (V_{CC} + 0.3V)
LO, RF to GND Maximum Current 30mA
RF Input Power .....+30dBm
Baseband Differential I/Q Input Power.....+20dBm
LO Input Power.....+10dBm
RBIASLO1 Maximum Current 10mA
RBIASLO2 Maximum Current 10mA
RBIASLO3 Maximum Current 10mA
Continuous Power Dissipation (Note 1) 7.6W
Operating Case Temperature Range (Note 2) ....-40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Based on junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.

Note 2: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS

TQFN

Junction-to-Ambient
Thermal Resistance (θ_{JA}) (Notes 3, 4) .....+34°C/W

Junction-to-Case
Thermal Resistance (θ_{JC}) (Notes 1, 4) .....+8.5°C/W

Note 3: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$. This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.

Note 4: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

(MAX2021 *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, GND = 0V, I/Q inputs terminated into 50Ω to GND, LO input terminated into 50Ω, RF output terminated into 50Ω, 0V common-mode input, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_C = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V, T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Total Supply Current	I_{TOTAL}	Pins 3, 13, 15, 31, 33 all connected to V_{CC}	230	271	315	mA
Total Power Dissipation				1355	1654	mW

RECOMMENDED AC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
RF Frequency (Note 5)	f_{RF}		650		1200	MHz
LO Frequency (Note 5)	f_{LO}		750		1200	MHz
IF Frequency (Note 5)	f_{IF}				550	MHz
LO Power Range	P_{LO}		-6		+3	dBm

AC ELECTRICAL CHARACTERISTICS (Modulator)

(MAX2021 *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, GND = 0V, I/Q differential inputs driven from a 100Ω DC-coupled source, 0V common-mode input, P_{LO} = 0dBm, 750MHz ≤ f_{LO} ≤ 1200MHz, 50Ω LO and RF system impedance, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5V, V_{BBI} = 1.4V_{P-P} differential, V_{BBQ} = 1.4V_{P-P} differential, f_{IQ} = 1MHz, f_{LO} = 900MHz, T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BASEBAND INPUT							
Baseband Input Differential Impedance		f_{IQ} = 1MHz			53		Ā
BB Common-Mode Input Voltage Range				-3.5	0	+3.5	V
LO INPUT							
LO Input Return Loss		RF and IF terminated (Note 7)			12		dB
I/Q MIXER OUTPUTS							
Output IP3	OIP3	f_{BB1} = 1.8MHz, f_{BB2} = 1.9MHz	f_{LO} = 900MHz		21.1		dBm
			f_{LO} = 1000MHz		22.3		
Output IP2	OIP2	f_{BB1} = 1.8MHz, f_{BB2} = 1.9MHz			57.9		dBm
Output P1dB		f_{BB} = 25MHz, P_{LO} = 0dBm			16.7		dBm
Output Power	P_{OUT}				0.7		dBm
Output Power Variation Over Temperature		T_C = -40°C to +85°C			-0.016		dB/°C
Output-Power Flatness		Sweep f_{BB}, P_{RF} flatness for f_{BB} from 1MHz to 50MHz			0.15		dB
ACLR (1st Adjacent Channel 5MHz Offset)		Single-carrier WCDMA (Note 8)			65		dBc
LO Leakage		No external calibration, with each baseband input terminated in 50Ā			-32		dBm
Sideband Suppression		No external calibration, f_{LO} = 920MHz	P_{LO} = 0dBm	30	39.6		dBc
			P_{LO} = -3dBm		43.5		
Output Noise Density		Each baseband input terminated in 50Ā (Note 9)			-174		dBm/Hz
Output Noise Floor		P_{OUT} = 0dBm, f_{LO} = 900MHz (Note 10)			-168		dBm/Hz
RF Return Loss		(Note 7)			15		dB

AC ELECTRICAL CHARACTERISTICS (Demodulator)

(MAX2021 *Typical Application Circuit* when operated as a demodulator, V_{CC} = 4.75V to 5.25V, GND = 0V, I/Q outputs are recombined using network shown in Figure 5. Losses of combining network not included in measurements. V_{DC} for BBI+. BBI-, BBQ+, BBQ- = 0V, P_{RF} = P_{LO} = 0dBm, 750MHz ≤ f_{LO} ≤ 1200MHz, 50Ω LO and RF system impedance, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5V, T_C = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF INPUT						
Conversion Loss	L_C	f_{BB} = 25MHz (Note 11)		9.2		dB
Noise Figure	NF	f_{LO} = 900MHz		9.3		dB
Noise Figure Under-Blocking	NF_{BLOCK}	$f_{BLOCKER}$ = 900MHz, P_{RF} = 11dBm, f_{RF} = f_{LO} = 890MHz (Note 12)		17.8		dB
Input Third-Order Intercept	IIP3	f_{RF1} = 925MHz, f_{RF2} = 926MHz, f_{LO} = 900MHz, P_{RF} = P_{LO} = 0dBm, f_{SPUR} = 24MHz		35.2		dBm
Input Second-Order Intercept	IIP2	f_{RF1} = 925MHz, f_{RF2} = 926MHz, f_{LO} = 900MHz, P_{RF} = P_{LO} = 0dBm, f_{SPUR} = 51MHz		76		dBm
Input 1dB Compression	P_{1dB}	f_{IF} = 50MHz, f_{LO} = 900MHz, P_{LO} = 0dBm		30		dBm
I/Q Gain Mismatch		f_{BB} = 1MHz, f_{LO} = 900MHz, P_{LO} = 0dBm		0.06		dB
I/Q Phase Mismatch		f_{BB} = 1MHz, f_{LO} = 900MHz, P_{LO} = 0dBm		1.1		Degrees
		f_{BB} = 1MHz, f_{LO} = 900MHz, P_{LO} = -3dBm		0.15		Degrees
Minimum Demodulation 3dB Bandwidth		LO = 1160MHz LO > RF		> 550		MHz
Minimum 1dB Gain Flatness		LO = 1160MHz LO > RF		> 450		MHz

AC ELECTRICAL CHARACTERISTICS (Demodulator LO = 965MHz)

(*Typical Application Circuit* when operated as a demodulator. I/Q outputs are recombined using network shown in Figure 5. Losses of combining network not included in measurements. RF and LO ports are driven from 50Ω sources. Typical values are for T_A = +25°C, V_{CC} = 5.0V, I/Q DC voltage return = 0V, P_{RF} = 0dBm, P_{LO} = 0dBm, f_{RF} = 780MHz, f_{LO} = 965MHz, f_{IF} = 185MHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Loss	Lc			10.1		dB
Noise Figure	NF_{SSB}			10.4		dB
Noise Figure Under Blocking	NF_{BLOCK}	$f_{BLOCKER}$ = 700MHz, $P_{BLOCKER}$ = 11dBm, f_{LO} = 965MHz, f_{RF} = 865MHz, (Note 12)		19		dB
Input Third-Order Intercept Point	IIP3	f_{RF1} = 780MHz, f_{RF2} = 781MHz, P_{RF1} = P_{RF2} = 0dBm, f_{IF1} = 185MHz, f_{IF2} = 184MHz		34.5		dBm
		f_{RF1} = 780MHz, f_{RF2} = 735MHz, P_{RF1} = P_{RF2} = 0dBm, f_{IF1} = 185MHz, f_{IF2} = 230MHz		34.6		dBm

AC ELECTRICAL CHARACTERISTICS (Demodulator LO = 965MHz) (continued)

(*Typical Application Circuit* when operated as a demodulator. I/Q outputs are recombined using network shown in Figure 5. Losses of combining network not included in measurements. RF and LO ports are driven from 50Ω sources. Typical values are for T_A = +25°C, V_{CC} = 5.0V, I/Q DC voltage return = 0V, P_{RF} = 0dBm, P_{LO} = 0dBm, f_{RF} = 780MHz, f_{LO} = 965MHz, f_{IF} = 185MHz, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Second-Order Intercept Point	IIP2	f_{RF1} = 780MHz, f_{RF2} = 781MHz, P_{RF1} = P_{RF2} = 0dBm, f_{IF1} = 185MHz, f_{IF2} = 184MHz, f_{IF1}+ f_{IF2} term		70.1		dBm
		f_{RF1} = 780MHz, f_{RF2} = 735MHz, P_{RF1} = P_{RF2} = 0dBm, f_{IF1} = 185MHz, f_{IF2} = 230MHz, f_{IF1}+ f_{IF2} term		70.2		
Spurious Relative to a Fundamental at 780MHz		2LO - 2RF, f_{RF} = 872.5MHz, P_{RF} = -10dBm		84		dBc
		3LO - 3RF, f_{RF} = 903.333MHz, P_{RF} = -10dBm		99		
		3RF - 2LO, f_{RF} = 705MHz, P_{RF} = -10dBm		105		
		4RF - 3LO, f_{RF} = 770MHz, P_{RF} = -10dBm		114		
		5RF - 4LO, f_{RF} = 809MHz, P_{RF} = -10dBm		115		
Input Compression from Linear		P_{RF} = 0dBm to 21dBm		0.17		dB
I/Q Gain Mismatch				0.05		dB
I/Q Phase Mismatch				0.4		Degrees
1dB Conversion Loss Flatness		f_{LO} = 965MHz, f_{LO} > f_{RF}		400		MHz
RF Return Loss				17		dB
LO Return Loss				12		dB

Note 5: Recommended functional range. Not production tested. Operation outside this range is possible, but with degraded performance of some parameters.

Note 6: Guaranteed by design and characterization.

Note 7: Parameter also applies to demodulator topology.

Note 8: Single-carrier WCDMA with 10.5dB peak-to-average ratio at 0.1% complementary cumulative distribution function, P_{RF} = -10dBm (P_{RF} is chosen to give -65dBc ACLR).

Note 9: No baseband drive input. Measured with the inputs terminated in 50Ω. At low output levels, the output noise is thermal.

Note 10: The output noise versus P_{OUT} curve has the slope of LO noise (Ln dBc/Hz) due to reciprocal mixing.

Note 11: Conversion loss is measured from the single-ended RF input to single-ended combined baseband output.

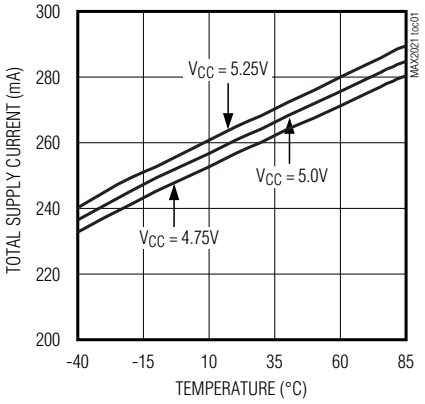
Note 12: The LO noise ($L = 10^{(Ln/10)}$), determined from the modulator measurements can be used to deduce the noise figure under-blocking at operating temperature (Tp in Kelvin), F_{BLOCK} = 1 + (Lcn - 1) Tp / To + LP_{BLOCK} / (1000kTo), where To = 290K, P_{BLOCK} in mW, k is Boltzmann's constant = 1.381 x $10^{(-23)}$ J/K, and $Lcn = 10^{(Lc/10)}$, Lc is the conversion loss. Noise figure under-blocking in dB is NF_{BLOCK} = 10 x log (F_{BLOCK}). Refer to Application Note 3632: *Wideband LO Noise in Passive Transmit-Receive Mixer ICs*.

Typical Operating Characteristics

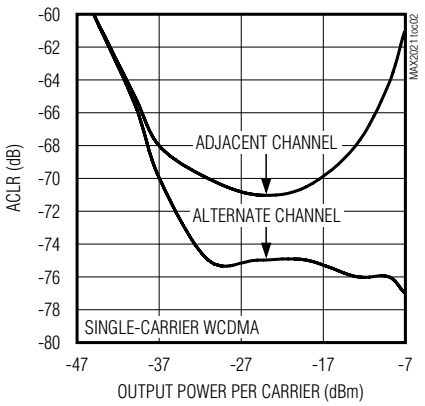
(MAX2021 *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, GND = 0V, I/Q differential inputs driven from a 100Ω DC-coupled source, 0V common-mode input, P_{LO} = 0dBm, 750MHz ≤ f_{LO} ≤ 1200MHz, 50Ω LO and RF system impedance, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5V, V_{BBI} = 1.4V_{P-P} differential, V_{BBQ} = 1.4V_{P-P} differential, f_{IQ} = 1MHz, f_{LO} = 900MHz, T_C = +25°C, unless otherwise noted.)

MODULATOR

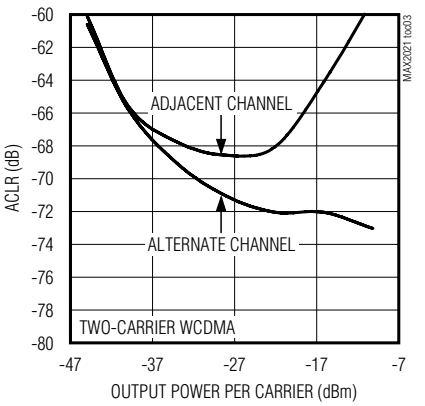
TOTAL SUPPLY CURRENT vs. TEMPERATURE (T_C)



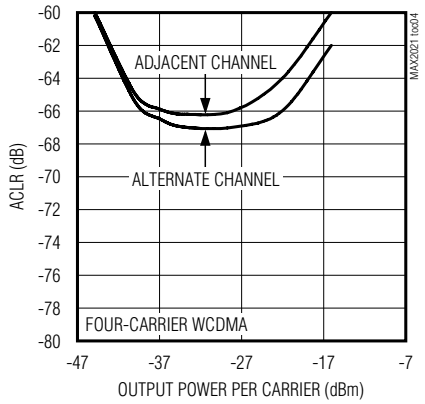
ACLR vs. OUTPUT POWER PER CARRIER



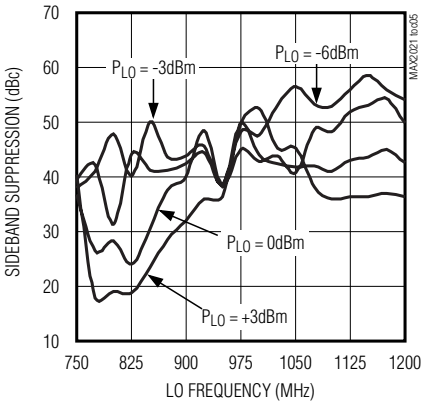
ACLR vs. OUTPUT POWER PER CARRIER



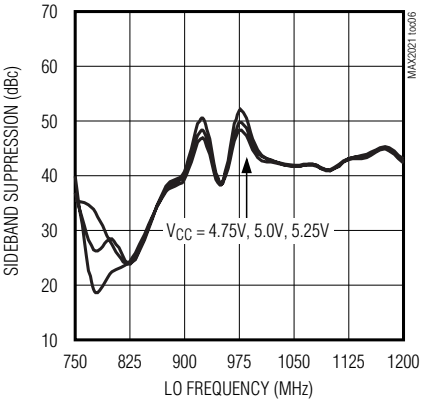
ACLR vs. OUTPUT POWER PER CARRIER



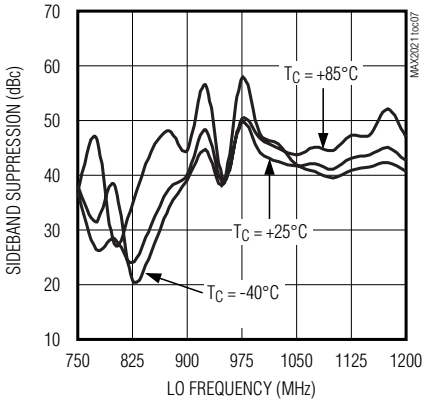
SIDEBAND SUPPRESSION vs. LO FREQUENCY



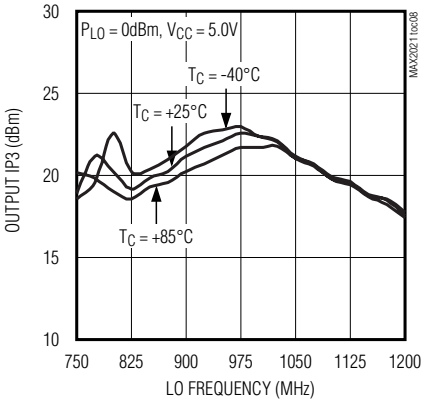
SIDEBAND SUPPRESSION vs. LO FREQUENCY



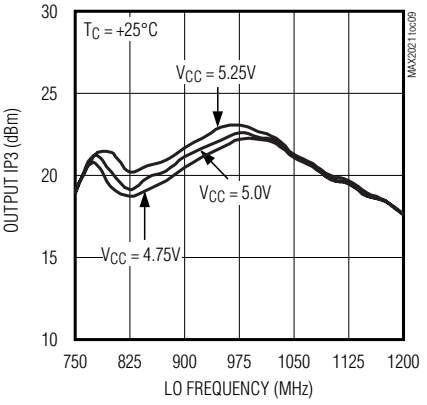
SIDEBAND SUPPRESSION vs. LO FREQUENCY



OUTPUT IP3 vs. LO FREQUENCY



OUTPUT IP3 vs. LO FREQUENCY



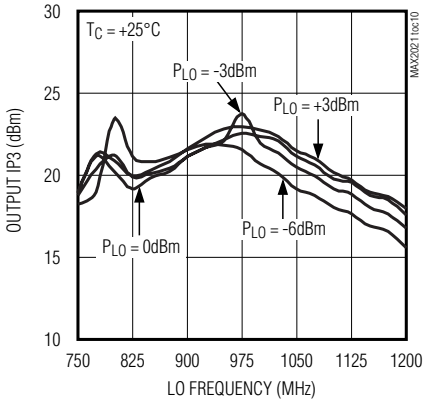
High-Dynamic-Range, Direct Up-/Downconversion 650MHz to 1200MHz Quadrature Mod/Demod

Typical Operating Characteristics (continued)

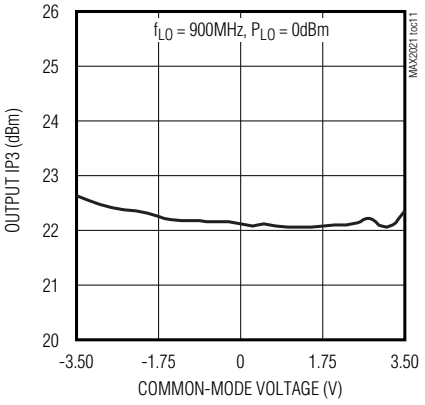
(MAX2021 *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, GND = 0V, I/Q differential inputs driven from a 100Ω DC-coupled source, 0V common-mode input, P_{LO} = 0dBm, 750MHz ≤ f_{LO} ≤ 1200MHz, 50Ω LO and RF system impedance, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5V, V_{BBI} = 1.4V_{P-P} differential, V_{BBQ} = 1.4V_{P-P} differential, f_{IQ} = 1MHz, f_{LO} = 900MHz, T_C = +25°C, unless otherwise noted.)

MODULATOR

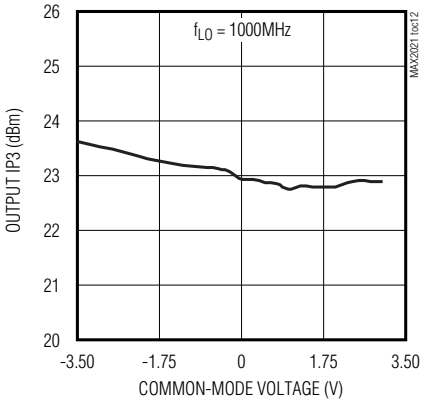
OUTPUT IP3 vs. LO FREQUENCY



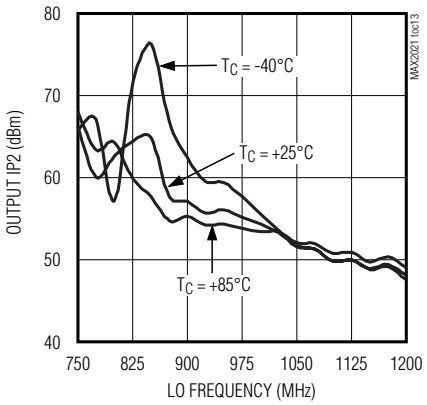
OUTPUT IP3 vs. COMMON-MODE VOLTAGE



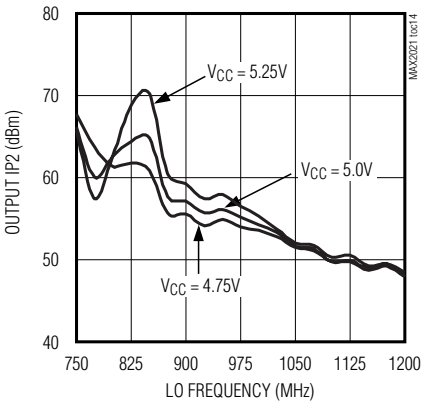
OUTPUT IP3 vs. COMMON-MODE VOLTAGE



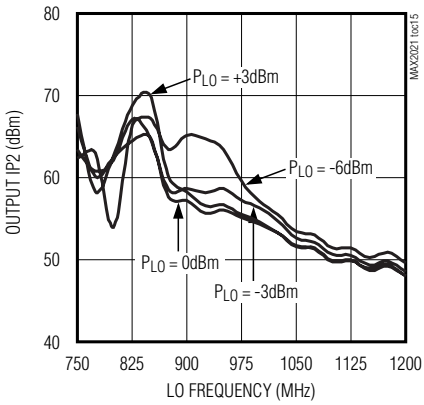
OUTPUT IP2 vs. LO FREQUENCY



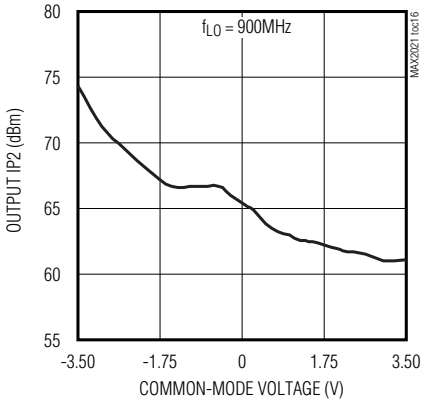
OUTPUT IP2 vs. LO FREQUENCY



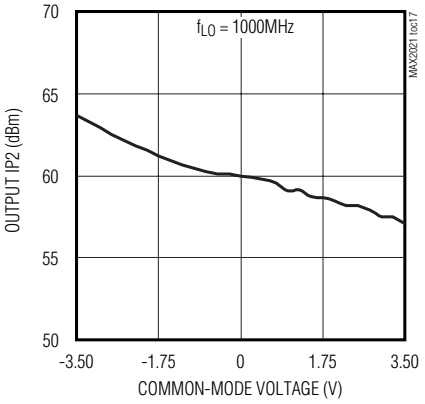
OUTPUT IP2 vs. LO FREQUENCY



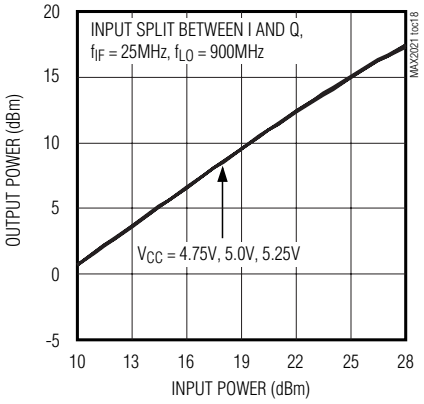
OUTPUT IP2 vs. COMMON-MODE VOLTAGE



OUTPUT IP2 vs. COMMON-MODE VOLTAGE



MODULATOR OUTPUT POWER vs. INPUT POWER

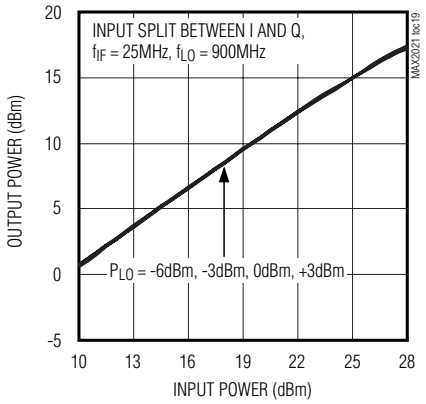


Typical Operating Characteristics (continued)

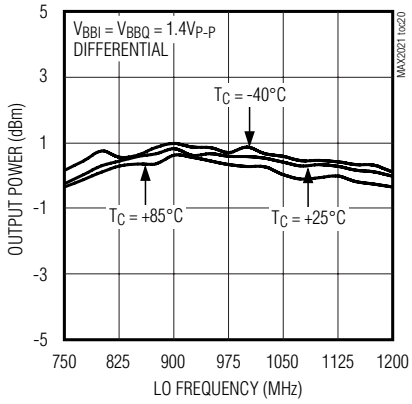
(MAX2021 *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, GND = 0V, I/Q differential inputs driven from a 100Ω DC-coupled source, 0V common-mode input, P_{LO} = 0dBm, 750MHz ≤ f_{LO} ≤ 1200MHz, 50Ω LO and RF system impedance, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5V, V_{BBI} = 1.4V_{P-P} differential, V_{BBQ} = 1.4V_{P-P} differential, f_{IQ} = 1MHz, f_{LO} = 900MHz, T_C = +25°C, unless otherwise noted.)

MODULATOR

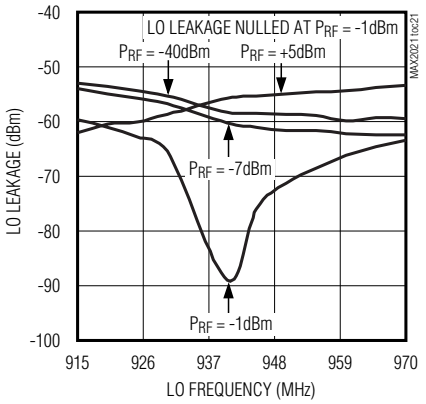
MODULATOR OUTPUT POWER vs. INPUT POWER



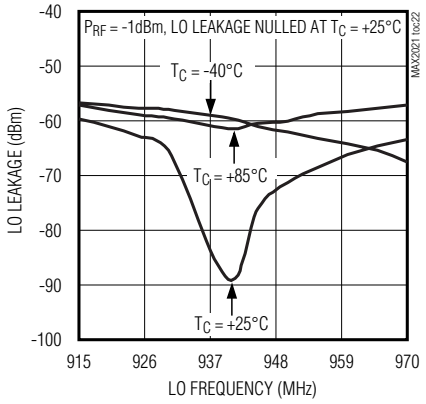
MODULATOR OUTPUT POWER vs. LO FREQUENCY



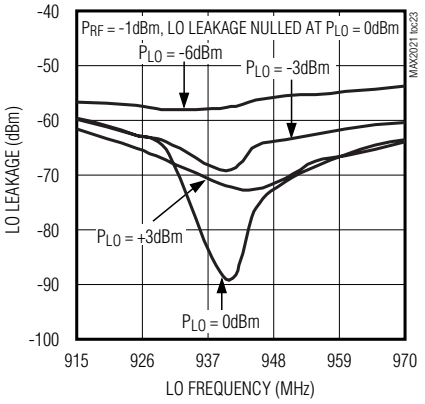
LO LEAKAGE vs. LO FREQUENCY



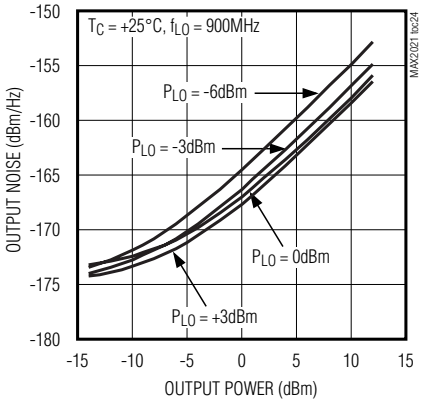
LO LEAKAGE vs. LO FREQUENCY



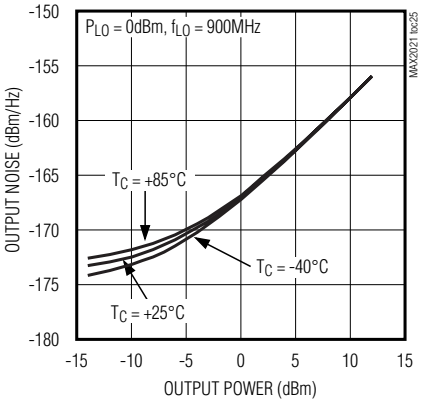
LO LEAKAGE vs. LO FREQUENCY



OUTPUT NOISE vs. OUTPUT POWER



OUTPUT NOISE vs. OUTPUT POWER

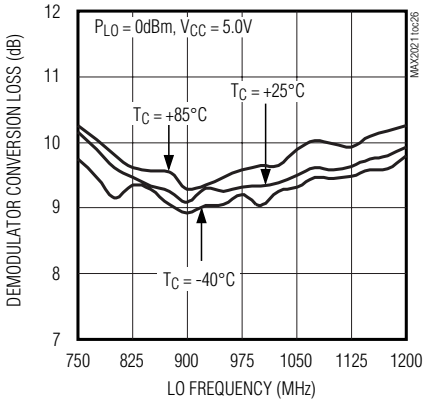


Typical Operating Characteristics

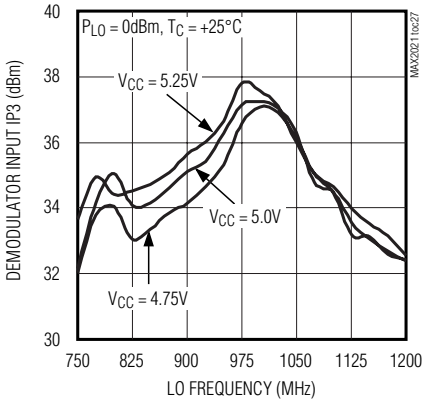
(MAX2021 *Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, GND = 0V, I/Q outputs are recombined using network shown in Figure 5. Losses of combining network not included in measurements. P_{RF} = 5dBm, P_{LO} = 0dBm, 750MHz ≤ f_{LO} ≤ 1200MHz, 50Ω LO and RF system impedance, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5V, f_{LO} = 900MHz, T_C = +25°C, unless otherwise noted.)

DEMODULATOR (VARIABLE LO)

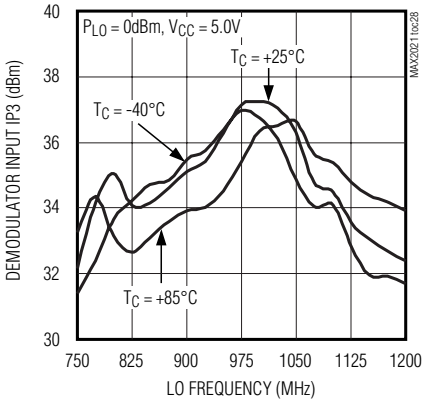
DEMODULATOR CONVERSION LOSS vs. LO FREQUENCY



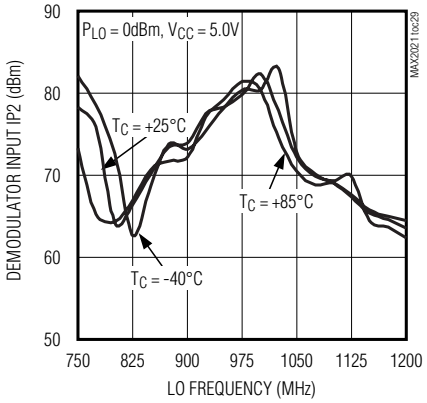
DEMODULATOR INPUT IP3 vs. LO FREQUENCY



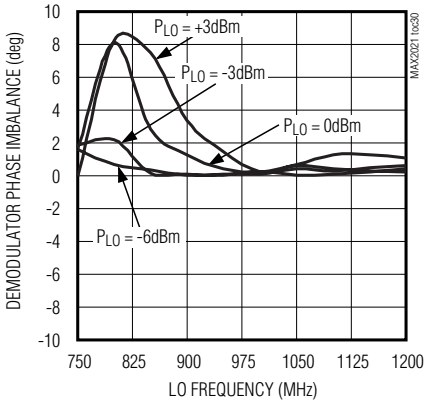
DEMODULATOR INPUT IP3 vs. LO FREQUENCY



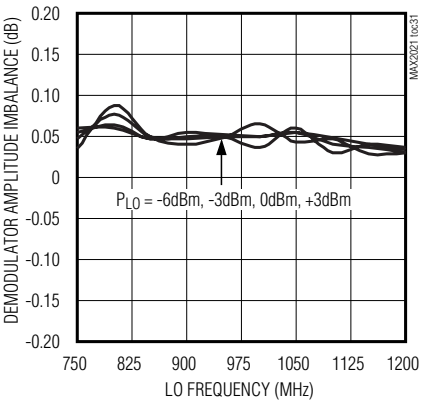
DEMODULATOR INPUT IP2 vs. LO FREQUENCY



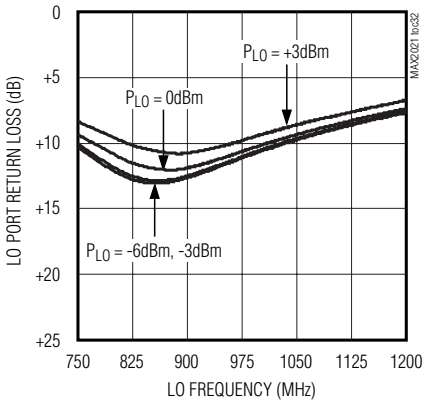
DEMODULATOR PHASE IMBALANCE vs. LO FREQUENCY



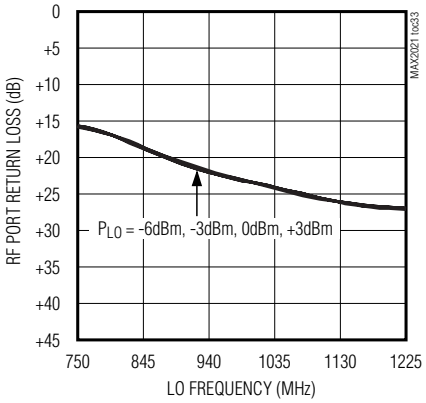
DEMODULATOR AMPLITUDE IMBALANCE vs. LO FREQUENCY



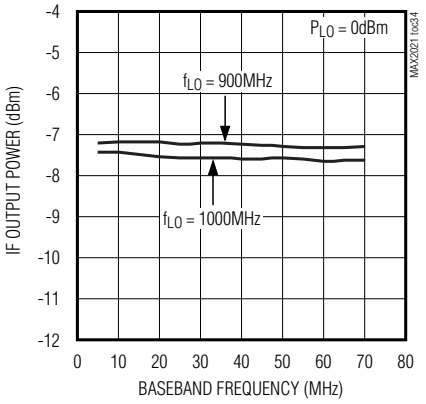
LO PORT RETURN LOSS vs. LO FREQUENCY



RF PORT RETURN LOSS vs. LO FREQUENCY



IF FLATNESS vs. BASEBAND FREQUENCY

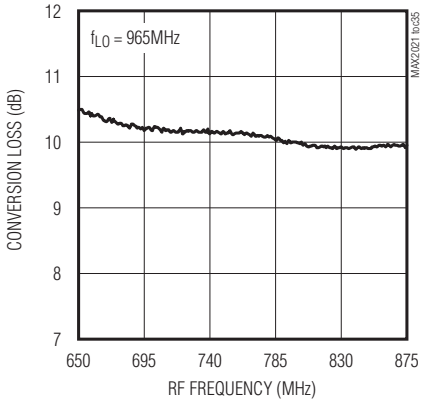


Typical Operating Characteristics

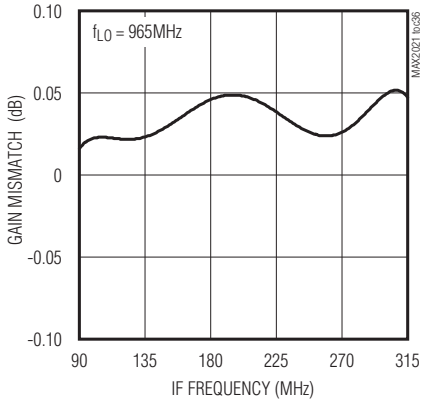
(MAX2021 *Typical Application Circuit*, V_{CC} = 5.0V, GND = 0V, I/Q outputs are recombined using network shown in Figure 5. Losses of combining network not included in measurements. P_{RF} = 0dBm, P_{LO} = 0dBm, f_{LO} = 965MHz, f_{IF} = f_{LO} - f_{RF}, 50Ω LO and RF system impedance, R1 = 432Ω, R2 = 619Ω, R3 = 332Ω, T_A = +25°C, unless otherwise noted.)

DEMODULATOR (FIXED LO)

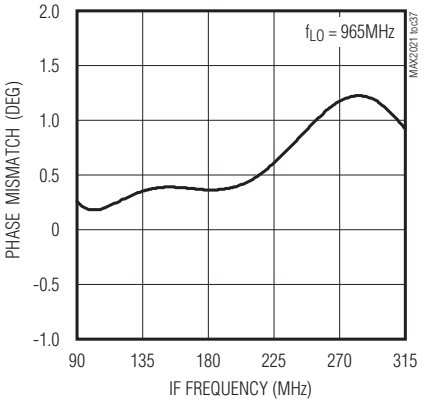
CONVERSION LOSS vs. RF FREQUENCY



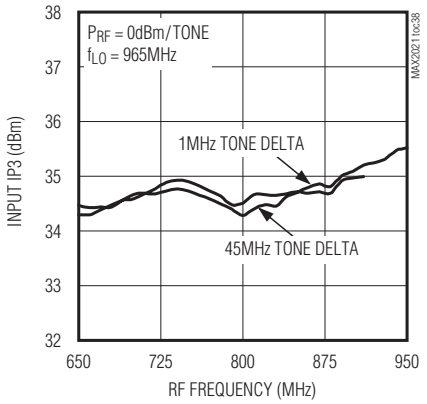
I/Q GAIN MISMATCH vs. IF FREQUENCY



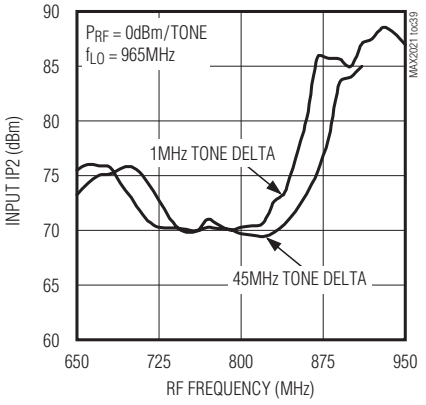
I/Q PHASE MISMATCH vs. IF FREQUENCY



INPUT IP3 vs. RF FREQUENCY



INPUT IP2 vs. RF FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1, 5, 9–12, 14, 16–19, 22, 24, 27–30, 32, 34–36	GND	Ground
2	RBIASLO3	3rd LO Amplifier Bias. Connect a 332Ω resistor to ground.
3	VCCLOA	LO Input Buffer Amplifier Supply Voltage. Bypass to GND with 33pF and 0.1µF capacitors as close as possible to the pin.
4	LO	Local Oscillator Input. 50Ω input impedance. Requires a DC-blocking capacitor.
6	RBIASLO1	1st LO Input Buffer Amplifier Bias. Connect a 432Ω resistor to ground.
7	N.C.	No Connection. Leave unconnected.
8	RBIASLO2	2nd LO Amplifier Bias. Connect a 619Ω resistor to ground.
13	VCCLOI1	I-Channel 1st LO Amplifier Supply Voltage. Bypass to GND with 33pF and 0.1µF capacitors as close as possible to the pin.
15	VCCLOI2	I-Channel 2nd LO Amplifier Supply Voltage. Bypass to GND with 33pF and 0.1µF capacitors as close as possible to the pin.
20	BBI+	Baseband In-Phase Noninverting Port
21	BBI-	Baseband In-Phase Inverting Port
23	RF	RF Port. This port is matched to 50Ω. Requires a DC-blocking capacitor.
25	BBQ-	Baseband Quadrature Inverting Port
26	BBQ+	Baseband Quadrature Noninverting Port
31	VCCLOQ2	Q-Channel 2nd LO Amplifier Supply Voltage. Bypass to GND with 33pF and 0.1µF capacitors as close as possible to the pin.
33	VCCLOQ1	Q-Channel 1st LO Amplifier Supply Voltage. Bypass to GND with 33pF and 0.1µF capacitors as close as possible to the pin.
EP	GND	Exposed Ground Pad. The exposed pad **MUST** be soldered to the ground plane using multiple vias.

Detailed Description

The MAX2021 is designed for upconverting differential in-phase (I) and quadrature (Q) inputs from baseband to a 650MHz to 1200MHz RF frequency range. The device can also be used as a demodulator, downconverting an RF input signal directly to baseband. Applications include RFID handheld and portal readers, as well as single and multicarrier GSM/EDGE, cdma2000, WCDMA, and iDEN base stations. Direct conversion architectures are advantageous since they significantly reduce transmitter or receiver cost, part count, and power consumption as compared to traditional IF-based double conversion systems.

The MAX2021 integrates internal baluns, an LO buffer, a phase splitter, two LO driver amplifiers, two matched double-balanced passive mixers, and a wideband quadrature combiner. The MAX2021's high-linearity mixers, in conjunction with the part's precise in-phase and quadrature channel matching, enable the device to possess excellent dynamic range, ACLR, 1dB compression point, and LO and sideband suppression characteristics. These features make the MAX2021 ideal for four-carrier WCDMA operation.

LO Input Balun, LO Buffer, and Phase Splitter

The MAX2021 requires a single-ended LO input, with a nominal power of 0dBm. An internal low-loss balun at the LO input converts the single-ended LO signal to a differential signal at the LO buffer input. In addition, the internal balun matches the buffer's input impedance to 50Ω over the entire band of operation.

The output of the LO buffer goes through a phase splitter, which generates a second LO signal that is shifted by 90° with respect to the original. The 0° and 90° LO signals drive the I and Q mixers, respectively.

LO Driver

Following the phase splitter, the 0° and 90° LO signals are each amplified by a two-stage amplifier to drive the I and Q mixers. The amplifier boosts the level of the LO

signals to compensate for any changes in LO drive levels. The two-stage LO amplifier allows a wide input power range for the LO drive. The MAX2021 can tolerate LO level swings from -6dBm to +3dBm.

I/Q Modulator

The MAX2021 modulator is composed of a pair of matched double-balanced passive mixers and a balun. The I and Q differential baseband inputs accept signals from DC to 550MHz with differential amplitudes up to $4V_{P-P}$. The wide input bandwidths allow operation of the MAX2021 as either a direct RF modulator or as an image-reject mixer. The wide common-mode compliance range allows for direct interface with the baseband DACs. No active buffer circuitry is required between the baseband DACs and the MAX2021 for cdma2000 and WCDMA applications.

The I and Q signals directly modulate the 0° and 90° LO signals and are upconverted to the RF frequency. The outputs of the I and Q mixers are combined through a balun to produce a singled-ended RF output.

Applications Information

LO Input Drive

The LO input of the MAX2021 is internally matched to 50Ω, and requires a single-ended drive at a 750MHz to 1200MHz frequency range. An integrated balun converts the singled-ended input signal to a differential signal at the LO buffer differential input. An external DC-blocking capacitor is the only external part required at this interface. The LO input power should be within the -6dBm to +3dBm range. An LO input power of -3dBm is recommended for best overall peformance.

Modulator Baseband I/Q Input Drive

Drive the MAX2021 I and Q baseband inputs differentially for best performance. The baseband inputs have a 53Ω differential input impedance. The optimum source impedance for the I and Q inputs is 100Ω differential. This source impedance achieves the optimal signal transfer to the I and Q inputs, and the optimum output RF impedance match. The MAX2021 can accept input power levels of up to +20dBm on the I and Q inputs. Operation with complex waveforms, such as CDMA carriers or GSM signals, utilize input power levels that are far lower. This lower power operation is made necessary by the high peak-to-average ratios of these complex waveforms. The peak signals must be kept below the compression level of the MAX2021.

The four baseband ports need some form of DC return to establish a common mode that the on-chip circuitry drives. This can be achieved by directly DC-coupling to the baseband ports (staying within the ±3.5V common-mode range), through an inductor to ground, or through a low-value resistor to ground.

The MAX2021 is designed to interface directly with Maxim high-speed DACs. This generates an ideal total transmitter lineup, with minimal ancillary circuit elements. Such DACs include the MAX5875 series of dual DACs, and the MAX5895 dual interpolating DAC. These DACs have ground-referenced differential current outputs. Typical termination of each DAC output into a 50Ω load resistor to ground, and a 10mA nominal DC output current results in a 0.5V common-mode DC level into the modulator I/Q inputs. The nominal signal level provided by the DACs will be in the -12dBm range for a single CDMA or WCDMA carrier, reducing to -18dBm per carrier for a four-carrier application.

The I/Q input bandwidth is greater than 50MHz at -0.1dB response. The direct connection of the DAC to the MAX2021 ensures the maximum signal fidelity, with no performance-limiting baseband amplifiers required. The DAC output can be passed through a lowpass filter to remove the image frequencies from the DAC's output response. The MAX5895 dual interpolating DAC can be operated at interpolation rates up to x8. This has the benefit of moving the DAC image frequencies to a very high, remote frequency, easing the design of the baseband filters. The DAC's output noise floor and interpolation filter stopband attenuation are sufficiently good to ensure that the 3GPP noise floor requirement is met for large frequency offsets, 60MHz for example, with no filtering required on the RF output of the modulator.

Figure 1 illustrates the ease and efficiency of interfacing the MAX2021 with a Maxim DAC (in this case the MAX5895 dual 16-bit interpolating-modulating DAC) and with Maxim VGA and VCO/Synth ICs.

The MAX5895 DAC has programmable gain and differential offset controls built in. These can be used to optimize the LO leakage and sideband suppression of the MAX2021 quadrature modulator.

RF Output

The MAX2021 utilizes an internal passive mixer architecture that enables the device to possess an exceptionally low-output noise floor. With such architectures, the total output noise is typically a power summation of the theoretical thermal noise (KTB) and the noise contribution from the on-chip LO buffer circuitry. As demonstrated in the *Typical Operating Characteristics*, the MAX2021's output noise approaches the thermal limit of -174dBm/Hz for lower output power levels. As the output power increases, the noise level tracks the noise contribution from the LO buffer circuitry, which is approximately -168dBc/Hz.

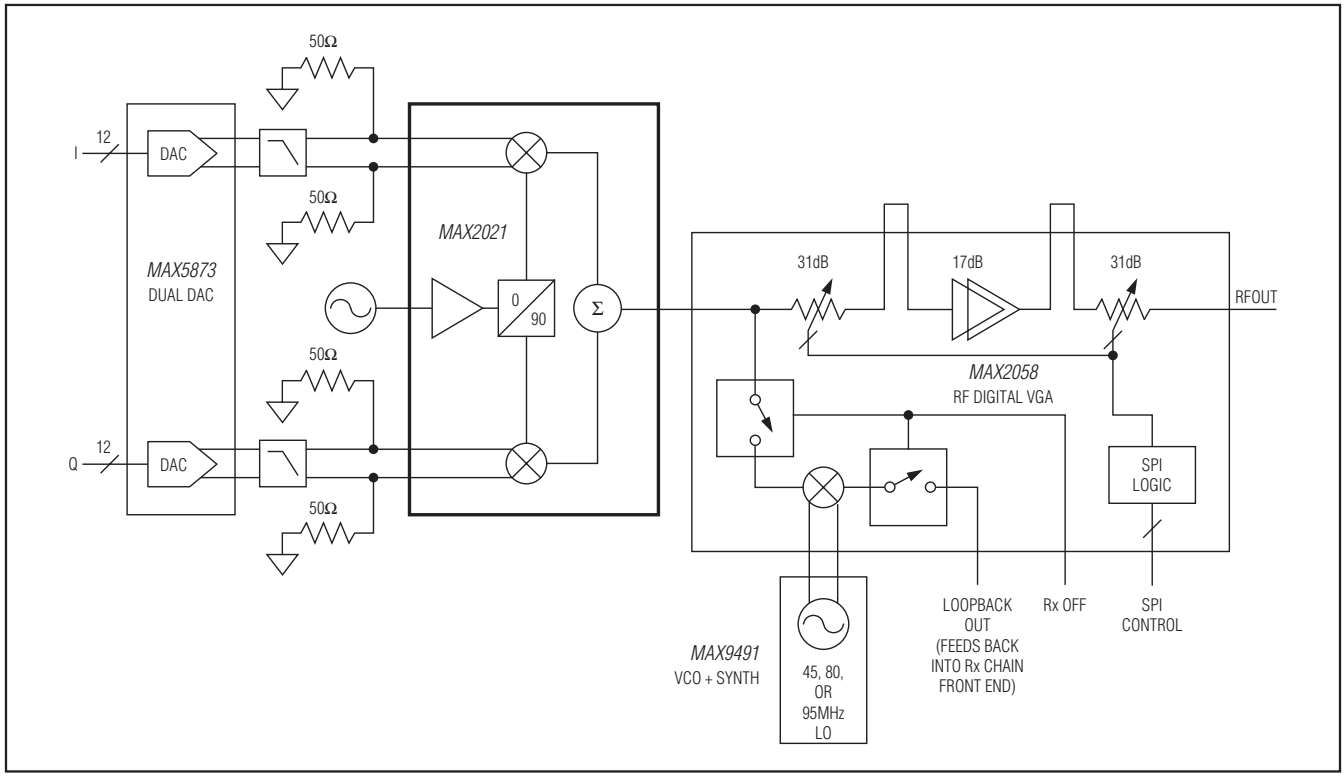


Figure 1. Transmitter Lineup

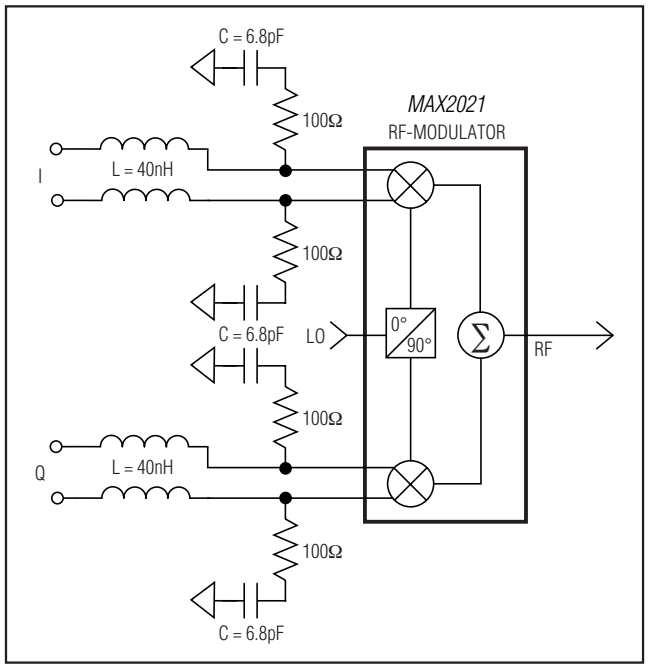


Figure 2. Diplexer Network Recommended for GSM 900 Transmitter Applications

The I/Q input power levels and the insertion loss of the device determine the RF output power level. The input power is a function of the delivered input I and Q voltages to the internal 50Ω termination. For simple sinusoidal baseband signals, a level of 89mV$_{P-P}$ differential on the I and the Q inputs results in a -17dBm input power level delivered to the I and Q internal 50Ω terminations. This results in an RF output power of -23.2dBm.

External Diplexer

LO leakage at the RF port can be nulled to a level less than -80dBm by introducing DC offsets at the I and Q ports. However, this null at the RF port can be compromised by an improperly terminated I/Q IF interface. Care must be taken to match the I/Q ports to the driving DAC circuitry. Without matching, the LO's second-order (2f$_{LO}$) term may leak back into the modulator's I/Q input port where it can mix with the internal LO signal to produce additional LO leakage at the RF output. This leakage effectively counteracts against the LO nulling. In addition, the LO signal reflected at the I/Q IF port produces a residual DC term that can disturb the nulling condition.

As demonstrated in Figure 2, providing an RC termination on each of the I+, I-, Q+, Q- ports reduces the amount of LO leakage present at the RF port under

varying temperature, LO frequency, and baseband drive conditions. See the *Typical Operating Characteristics* for details. Note that the resistor value is chosen to be 100Ω with a corner frequency 1 / (2πRC) selected to adequately filter the f_{LO} and $2f_{LO}$ leakage, yet not affecting the flatness of the baseband response at the highest baseband frequency. The common-mode f_{LO} and $2f_{LO}$ signals at I+/I- and Q+/Q- effectively see the RC networks and thus become terminated in 50Ω (R/2). The RC network provides a path for absorbing the $2f_{LO}$ and f_{LO} leakage, while the inductor provides high impedance at f_{LO} and $2f_{LO}$ to help the diplexing process.

RF Demodulator

The MAX2021 can also be used as an RF demodulator (see Figure 3), downconverting an RF input signal directly to baseband. The single-ended RF input accepts signals from 650MHz to 1200MHz with power levels up to +30dBm. The passive mixer architecture produces a conversion loss of typically 9.2dB. The downconverter is optimized for high linearity and excellent noise performance, typically with a +35.2dBm IIP3, a P1dB of greater than +30dBm, and a 9.3dB noise figure.

A wide I/Q port bandwidth allows the port to be used as an image-reject mixer for downconversion to a quadrature IF frequency.

The RF and LO inputs are internally matched to 50Ω. Thus, no matching components are required, and only DC-blocking capacitors are needed for interfacing.

Demodulator Output Port Considerations

Much like in the modulator case, the four baseband ports require some form of DC return to establish a common mode that the on-chip circuitry drives. This can be achieved by directly DC-coupling to the baseband ports (staying within the ±3.5V common-mode range), through an inductor to ground, or through a low-value resistor to ground. Figure 4 shows a typical network that would be used to connect to each baseband port for demodulator operation. This network provides a common-mode DC return, implements a high-frequency diplexer to terminate unwanted RF terms, and also provides an impedance transformation to a possible higher impedance baseband amplifier.

The network C_a, R_a, L_a and C_b form a highpass/lowpass network to terminate the high frequencies into a load while passing the desired lower IF frequencies. Elements L_a, C_b, L_b, C_c, L_c, and C_d provide a possible impedance transformer. Depending on the impedance being transformed and the desired bandwidth, a fewer number of elements could be used. It is suggested that L_a and C_b always be used since they are part of the high frequency diplexer. If power matching is not a concern then this would reduce the elements to just the diplexer.

Resistor R_b provides a DC return to set the common mode voltage. In this case, due to the on-chip circuitry, the voltage would be approx 0V DC. It can also be used to reduce the load impedance of the next stage. Inductor L_d can provide a bit of high frequency gain peaking for wideband IF systems. Capacitor C_e is a DC block.

Typical values for C_a, R_a, L_a, and C_b would be 1.5pF, 50Ω, 11nH, and 4.7pF, respectively. These values can change depending on the LO, RF, and IF frequencies used. Resistor R_b is in the 50Ω to 200Ω range

The circuitry presented in Figure 4 does not allow for LO leakage at RF port nulling. Depending on the LO at RF leakage requirement, a trim voltage might need to be introduced on the baseband ports to null the LO leakage.

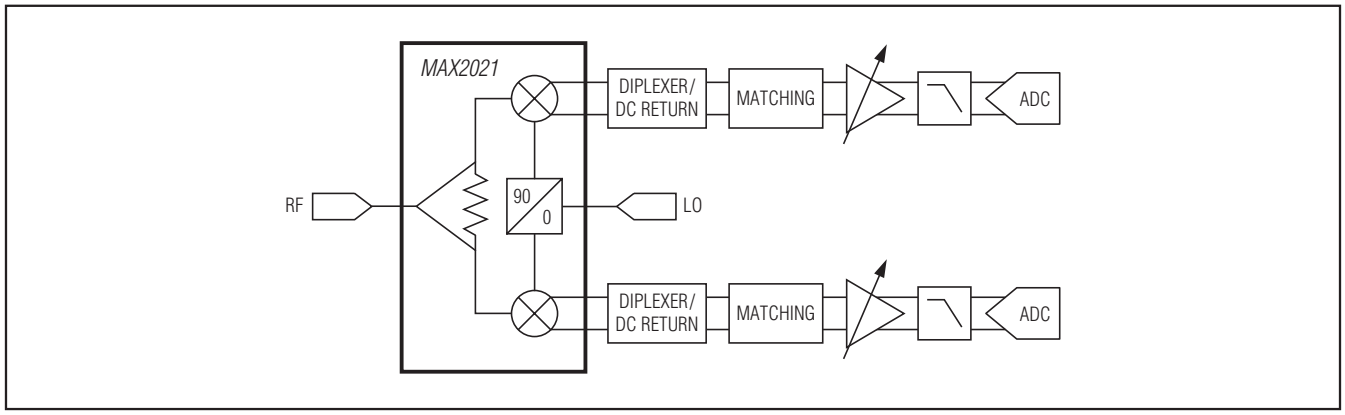


Figure 3. MAX2021 Demodulator Configuration

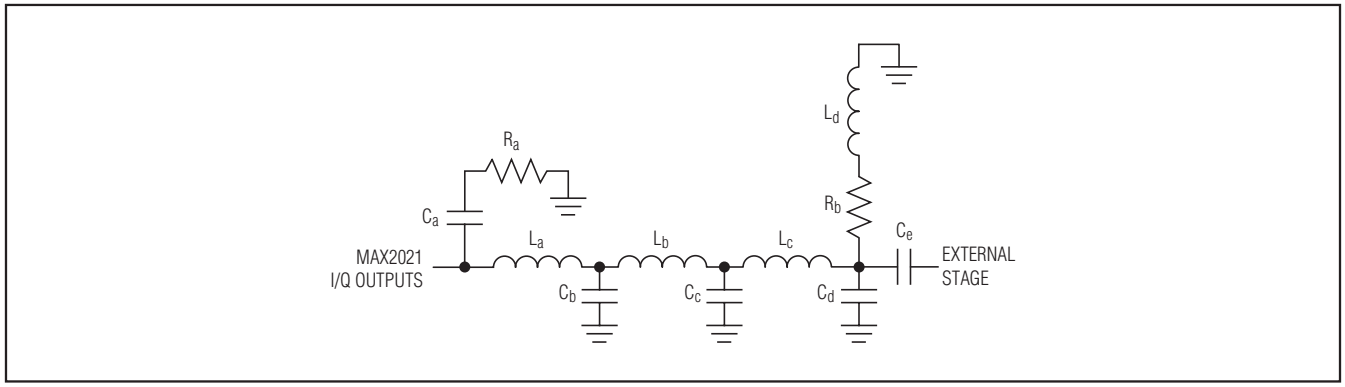


Figure 4. Baseband Port Typical Filtering and DC Return Network

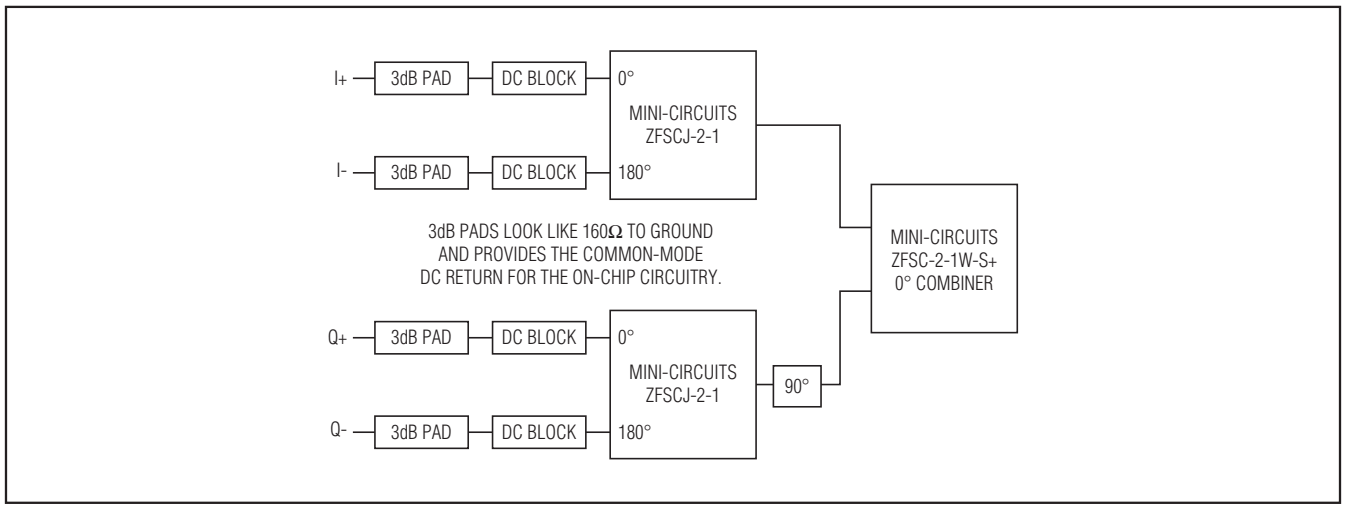


Figure 5. Demodulator Combining Diagram

Power Scaling with Changes to the Bias Resistors

Bias currents for the LO buffers are optimized by fine tuning resistors R1, R2, and R3. Maxim recommends using ±1%-tolerance resistors; however, standard ±5% values can be used if the ±1% components are not readily available. The resistor values shown in the *Typical Application Circuit* were chosen to provide peak performance for the entire 650MHz to 1200MHz band. If desired, the current can be backed off from this nominal value by choosing different values for R1, R2, and R3. Tables 1 and 2 outline the performance trade-offs that can be expected for various combinations of these bias resistors. As noted within the tables, the performance trade-offs may be more pronounced for different operating frequencies. Contact the factory for additional details.

Layout Considerations

A properly designed PCB is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For the best performance, route the ground pin traces directly to the exposed pad under the package. The PCB exposed pad **MUST** be connected to the ground plane of the PCB. It is suggested that multiple vias be used to connect this pad to the lower-level ground planes. This method provides a good RF/thermal conduction path for the device. Solder the exposed pad on the bottom of the device package to the PCB. The MAX2021 evaluation kit can be used as a reference for board layout. Gerber files are available upon request at **www.maximintegrated.com**.

Table 1. Typical Performance Trade-Offs as a Function of Current Draw—Modulator Mode

LO FREQ (MHz)	RF FREQ (MHz)	R1 (Ω)	R2 (Ω)	R3 (Ω)	I_{CC} (mA)	OIP3 (dBm)	LO LEAK (dBm)	IMAGE REJ (dBc)	OIP2 (dBm)
800	801.8	420	620	330	271	19.6	-32.1	23.9	50.5
		453	665	360	253	21.9	-32.7	34.0	51.0
		499	698	402	229	18.9	-33.7	30.0	52.6
		549	806	464	205	15.7	-34.4	23.7	46.0
		650	1000	550	173	13.6	-34.2	23.3	32.3
900	901.8	420	620	330	271	20.7	-31.4	43.4	54.0
		453	665	360	253	21.6	-31.6	42.4	55.4
		499	698	402	229	20.6	-31.8	42.7	59.8
		549	806	464	205	19.0	-31.9	40.3	50.7
		650	1000	550	173	14.9	-30.5	25.0	34.6
1000	1001.8	420	620	330	271	22.4	-32.8	39.3	55.5
		453	665	360	253	22.2	-33.2	39.1	56.3
		499	698	402	229	19.9	-33.8	43.5	55.0
		549	806	464	205	17.6	-34.8	40.5	51.4
		650	1000	550	173	14.6	-33.9	36.8	32.8

Note: *V_{CC} = 5V, P_{LO} = 0dBm, T_A = +25°C, I/Q voltage levels = 1.4V_{P-P} differential.*

Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass all VCC_ pins with 33pF and 0.1µF capacitors placed as close to the pins as possible. The smallest capacitor should be placed closest to the device.

To achieve optimum performance, use good voltage-supply layout techniques. The MAX2021 has several RF processing stages that use the various VCC_ pins, and while they have on-chip decoupling, off-chip interaction between them may degrade gain, linearity, carrier suppression, and output power-control range. Excessive coupling between stages may degrade stability.

Exposed Pad RF/Thermal Considerations

The EP of the MAX2021's 36-pin TQFN-EP package provides a low thermal-resistance path to the die. It is important that the PCB on which the IC is mounted be designed to conduct heat from this contact. In addition, the EP provides a low-inductance RF ground path for the device.

The exposed pad (EP) **MUST** be soldered to a ground plane on the PCB either directly or through an array of plated via holes. An array of 9 vias, in a 3 x 3 array, is suggested. Soldering the pad to ground is critical for efficient heat transfer. Use a solid ground plane wherever possible.

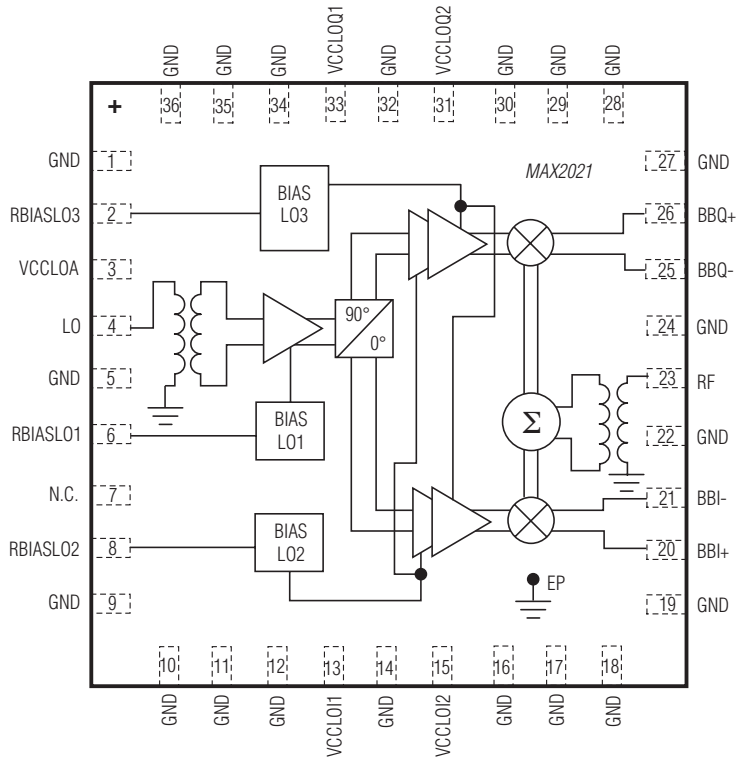
Table 2. Typical Performance Trade-Offs as a Function of Current Draw—Demodulator Mode

LO FREQ (MHz)	RF FREQ (MHz)	R1 (Ω)	R2 (Ω)	R3 (Ω)	I_{CC} (mA)	CONVERSION LOSS (dB)	IIP3 (dBm)	57MHz IIP2 (dBm)
800	771	420	620	330	269	9.8	33.85	62.1
		453	665	360	254	9.83	33.98	62.9
		499	698	402	230	9.81	32.2	66.6
		549	806	464	207	9.84	31.1	66.86
		650	1000	550	173	9.95	29.87	65.25
900	871	420	620	330	269	9.21	33.1	68
		453	665	360	254	9.25	33.9	66.87
		499	698	402	230	9.36	34.77	66.7
		549	806	464	207	9.39	35.3	66.6
		650	1000	550	173	9.46	32	64.64
1000	971	420	620	330	269	9.47	34.9	> 77.7
		453	665	360	254	9.5	35.4	> 77.5
		499	698	402	230	9.53	34.58	> 76.5
		549	806	464	207	9.5	33.15	> 76.5
		650	1000	550	173	9.61	31.5	76

Note: *Used on PCB 180° combiners and off PCB quadrature combiner with V_{CC} = 5V, P_{RF} = -3dBm, P_{LO} = 0dBm, T_A = +25°C, IF1 = 28MHz, IF2 = 29MHz.*

High-Dynamic-Range, Direct Up-/Downconversion 650MHz to 1200MHz Quadrature Mod/Demod

Pin Configuration/Functional Diagram



TQFN
(6mm x 6mm)

Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
TQFN	T3666+2	21-0141	90-0049

Typical Application Circuit

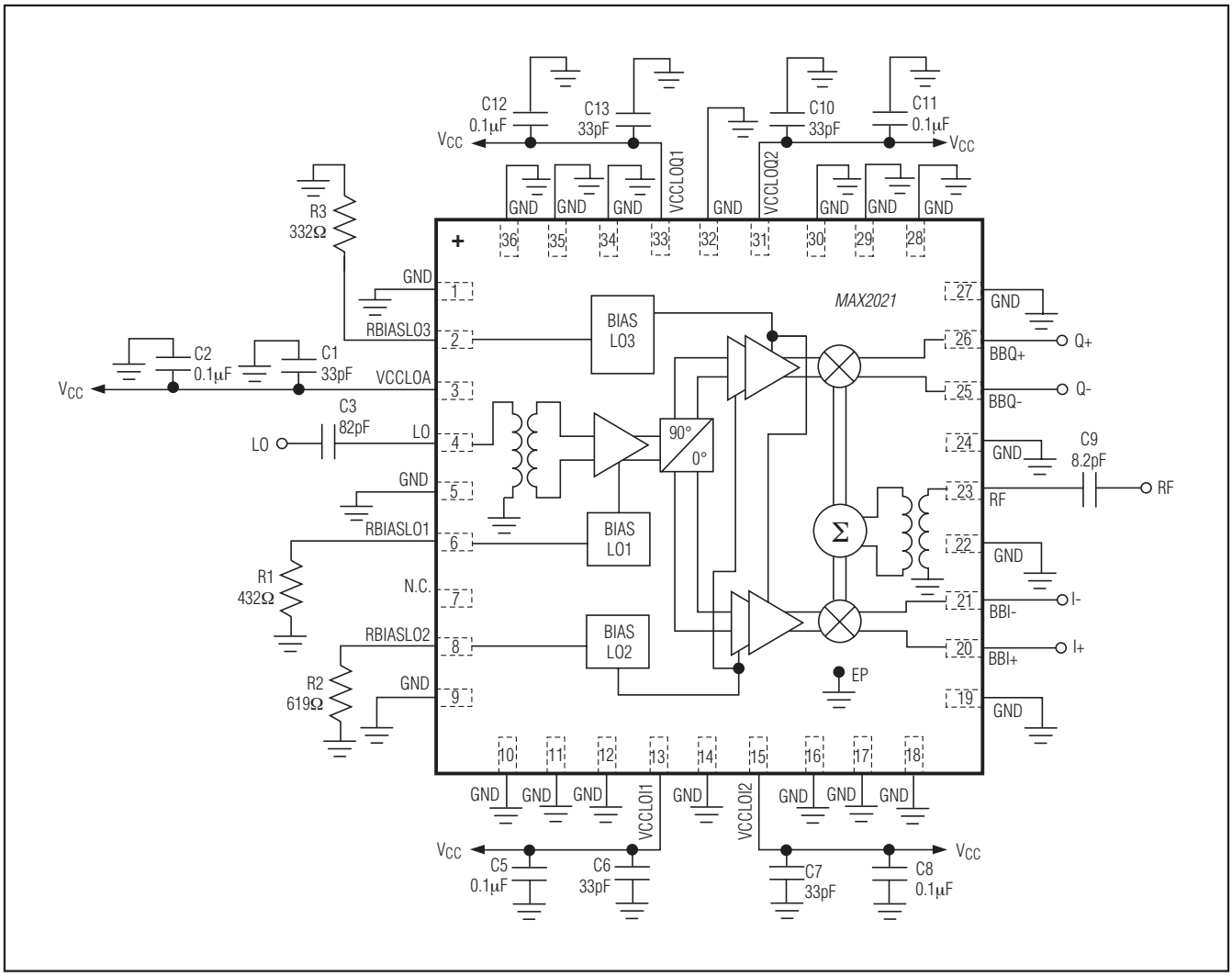


Table 3. Component List Referring to the *Typical Application Circuit*

COMPONENT	VALUE	DESCRIPTION
C1, C6, C7, C10, C13	33pF	33pF ±5%, 50V C0G ceramic capacitors (0402)
C2, C5, C8, C11, C12	0.1µF	0.1µF ±10%, 16V X7R ceramic capacitors (0603)
C3	82pF	82pF ±5%, 50V C0G ceramic capacitor (0402)
C9	8.2pF	8.2pF ±0.1pF, 50V C0G ceramic capacitor (0402)
R1	432Ω	432Ω ±1% resistor (0402)
R2	619Ω	619Ω ±1% resistor (0402)
R3	332Ω	332Ω ±1% resistor (0402)

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/06	Initial release	—
1	6/12	Updated *Features* section; updated *Ordering Information*, *Absolute Maximum Ratings*, *DC Electrical Characteristics*, *Pin Description*, *AC Electrical Characteristics* table, *Typical Operating Characteristics* globals, *Detailed Description* section, *I/Q Modulator* section, *Baseband I/Q Input Drive* section, *Power Scaling with the Changes to the Bias Resistors* section, *Typical Application Circuit*, Figures 1–3, and Table 1	1–3, 9–11, 14
2	4/13	Updated *Electrical Characteristics* table; updated TOCs 35–39; updated title and *Features* section	1, 2, 4, 8, 9, 12, 13