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January 2014

# FQD13N10L / FQU13N10L

# N-Channel QFET® MOSFET

100 V, 10 A, 180 mΩ

# **Description**

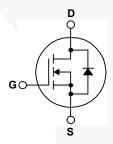
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching • Low Level Gate Drive Requirement Allowing power applications.

### **Features**

- 10 A, 100 V,  $R_{DS(on)}$  = 180 m $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_D = 5.0 A$
- Low Gate Charge (Typ. 8.7 nC)
- · Low Crss (Typ. 20 pF)
- 100% Avalanche Tested
- **Direct Operation Form Logic Drivers**







# Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQD13N10LTM / FQU13N10LTU	Unit
$V_{DSS}$	Drain-Source Voltage		100	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		10	Α
	- Continuous (T <sub>C</sub> = 100°C)		6.3	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	40	Α
V <sub>GSS</sub>	Gate-Source Voltage		± 20	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (N		95	mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	10	Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note		6.0	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *		2.5	W
	Power Dissipation (T <sub>C</sub> = 25°C)		40	W
	- Derate above 25°C		0.32	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

### **Thermal Characteristics**

Symbol	Parameter	FQD13N10LTM / FQU13N10LTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max. 3.13		
	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

# **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD13N10LTM	FQD13N10L	D-PAK	Tape and Reel	330 mm	16 mm	2500 units
FQU13N10LTU	FQU13N10L	I-PAK	Tube	N/A	N/A	70 units

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
$\Delta BV_{DSS}$ / $\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to 25°C		0.09		V/°C
Inss	Zana Cata Valtana Busin Comment	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 80 V, T <sub>C</sub> = 125°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.0		2.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_D = 5.0 \text{ A}$ $V_{GS} = 5 \text{ V}, I_D = 5.0 \text{ A}$		0.142 0.158	0.18 0.2	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 30 \text{ V}, I_{D} = 5.0 \text{ A}$		8.7		S
	ic Characteristics			400	500	
Ciss	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ $f = 1.0 \text{ MHz}$		400	520	pF
Coss	Output Capacitance			95	125	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			20	25	pF
Switchi	ing Characteristics					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, I_{D} = 12.8 \text{ A},$		7.5	25	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$		220	450	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			22	55	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4	)	72	150	ns
Qg	Total Gate Charge	$V_{DS} = 80 \text{ V}, I_{D} = 12.8 \text{ A},$		8.7	12	nC
$Q_{gs}$	Gate-Source Charge	V <sub>GS</sub> = 5 V	/	2.0		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4	.)	5.3		nC
Drain-S	Source Diode Characteristics a	nd Maximum Ratings				
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				10	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F	ce Diode Forward Current			40	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 10 A			1.5	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 12.8 A,		75	//	ns
		dI <sub>F</sub> / dt = 100 A/μs				

**Notes:**1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. L = 1.43 mH,  $I_{AS}$  = 10 A,  $V_{DD}$  = 25 V,  $R_{G}$  = 25  $\Omega$ , Starting  $T_{J}$  = 25°C.
3.  $I_{SD}$  ≤ 12.8 A, di/dt ≤ 300 A/ $\mu$ s,  $V_{DD}$  ≤ BV $_{DSS}$ , Starting  $T_{J}$  = 25°C.
4. Essentially independent of operating temperature.

# **Typical Characteristics**

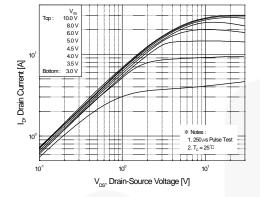


Figure 1. On-Region Characteristics

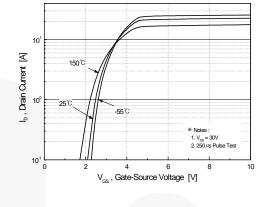


Figure 2. Transfer Characteristics

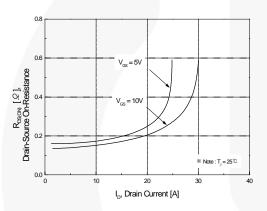


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

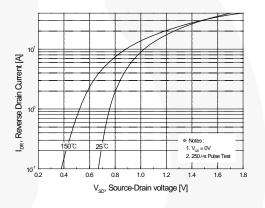


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

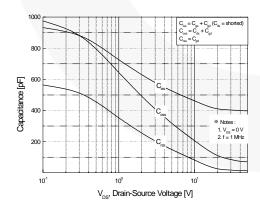


Figure 5. Capacitance Characteristics

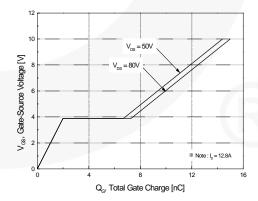
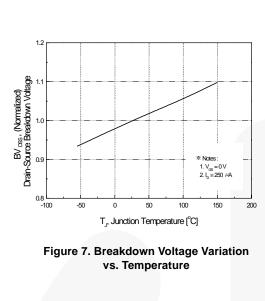


Figure 6. Gate Charge Characteristics



Typical Characteristics (Continued)

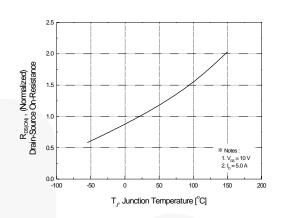
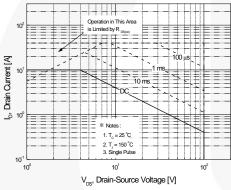


Figure 8. On-Resistance Variation vs. Temperature



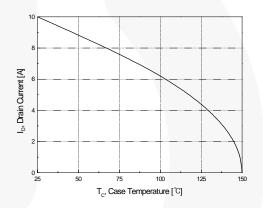


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

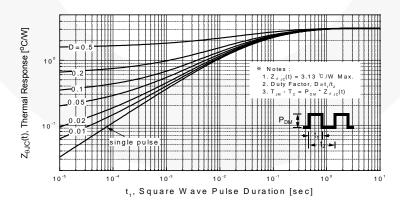


Figure 11. Transient Thermal Response Curve

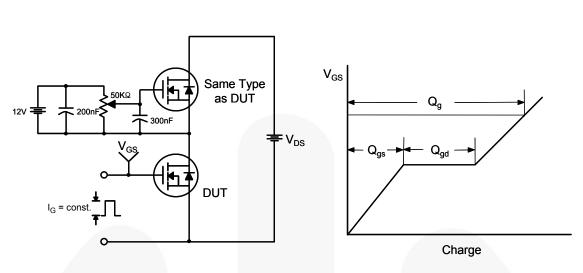


Figure 12. Gate Charge Test Circuit & Waveform

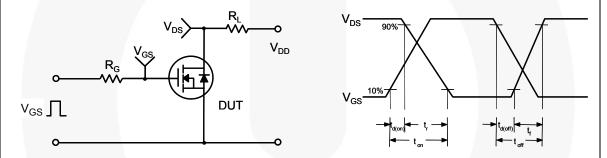


Figure 13. Resistive Switching Test Circuit & Waveforms

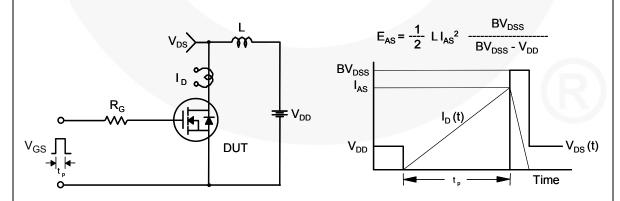
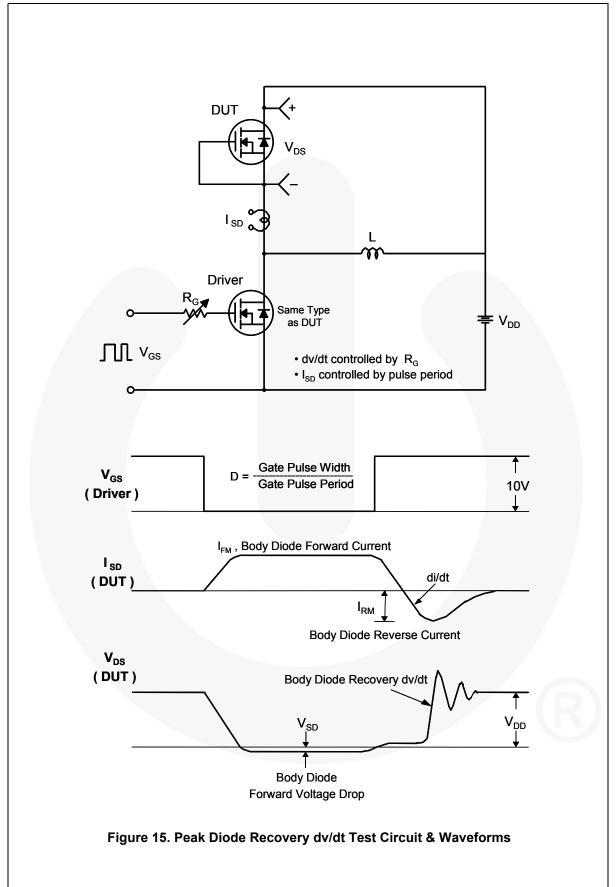


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



### **Mechanical Dimensions** 5.46 -5.55 MIN→ 1.27 6.22 5.97 6.50 MIN -1.02 MAX Ċ 2 (0.59)0.89 2.29 2.28 ⊕ 0.25 A A C 4.57 LAND PATTERN RECOMMENDATION 2.39 SEE 2.18 4.32 MIN NOTE D 0.58 0.45 5.21 MIN 10.41 9.40 SEE DETAIL A △ 0.10 B 0.51 GAGE PLANE NOTES: UNLESS OTHERWISE SPECIFIED THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA. ALL DIMENSIONS ARE IN MILLIMETERS. 10 (1.54)DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009. SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION. PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL. .78 .40 0.127 MAX DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS. SEATING PLANE (2.90)LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD DETAIL TO228P991X239-3N.

Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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DRAWING NUMBER AND REVISION: MKT-T0252A03REV9.

FAIRCHILD SEMICONDUCTOR.

(ROTATED -90°) SCALE: 12X

## **Mechanical Dimensions**

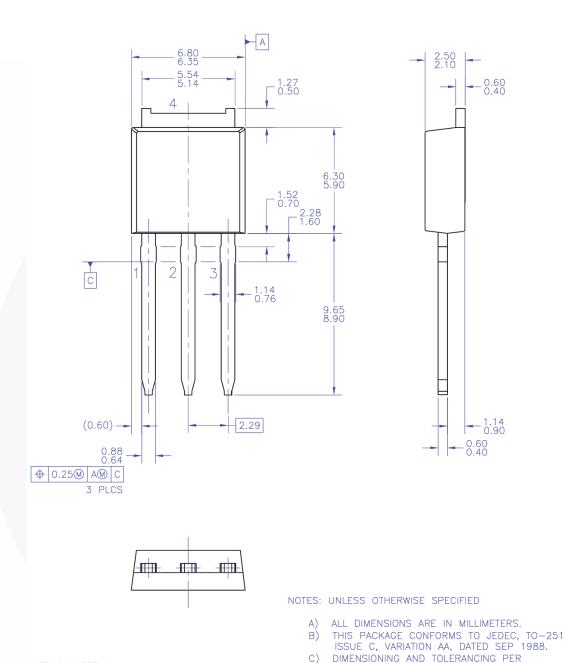


Figure 17. TO251 (I-PAK), Molded, 3-Lead

ASME Y14.5M-1994.

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