

GaAs pHEMT MMIC 1 WATT POWER AMPLIFIER, DC - 22 GHz



Typical Applications

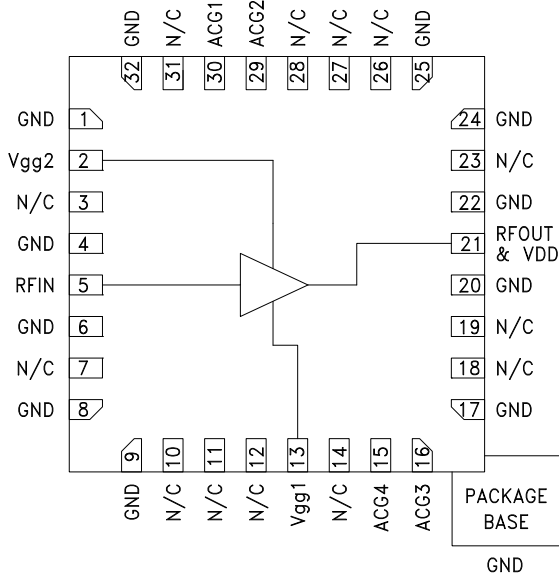
The HMC797LP5E is ideal for:

- Test Instrumentation
- Microwave Radio & VSAT
- Military & Space
- Telecom Infrastructure
- Fiber Optics

Features

- High P1dB Output Power: 28 dBm
- High Psat Output Power: 29.5 dBm
- High Gain: 13.5 dB
- High Output IP3: 39 dBm
- Supply Voltage: +10 V @ 400 mA
- 50 Ohm Matched Input/Output
- 32 Lead 5x5 mm SMT Package: 25 mm²

Functional Diagram



General Description

The HMC797LP5E is a GaAs MMIC pHEMT Distributed Power Amplifier which operates between DC and 22 GHz. The amplifier provides 13.5 dB of gain, 39 dBm output IP3 and +28 dBm of output power at 1 dB gain compression while requiring 400 mA from a +10 V supply. This versatile PA exhibits a positive gain slope from 4 to 20 GHz making it ideal for EW, ECM, Radar and test equipment applications. The HMC797LP5E amplifier I/Os are internally matched to 50 Ohms facilitating integration into multi-chip-modules (MCMs), is packaged in a leadless QFN 5x5 mm surface mount package, and requires no external matching components.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $V_{dd} = +10\text{V}$, $V_{gg2} = +3.5\text{V}$, $I_{dd} = 400\text{mA}^*$

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range	DC - 12			12 - 18			18 - 22			GHz
Gain	11	12.5		11	13.5		11	13.5		dB
Gain Flatness		±0.7			±0.5			±0.5		dB
Gain Variation Over Temperature		0.012			0.008			0.008		dB/°C
Input Return Loss		13			15			15		dB
Output Return Loss		12			16			13		dB
Output Power for 1 dB Compression (P1dB)	26	28		25	27		23.5	25.5		dBm
Saturated Output Power (Psat)		29.5			29			27		dBm
Output Third Order Intercept (IP3)		39			37			35		dBm
Noise Figure		3.5			4			6		dB
Supply Current (Idd) (Vdd= 10V, Vgg1= -0.8V Typ.)		400	440		400	440		400	440	mA

* Adjust Vgg1 between -2 to 0 V to achieve Idd = 400 mA typical.

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HMC797* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- HMC797LP5E Evaluation Board

DOCUMENTATION

Data Sheet

- HMC797 Die Data Sheet
- HMC797LP5E Data Sheet

TOOLS AND SIMULATIONS

- HMC797 Die S-Parameters
- HMC797LP5E S-Parameters

REFERENCE MATERIALS

Quality Documentation

- Package/Assembly Qualification Test Report: 32L 5x5mm QFN Package (QTR: 10009 REV: 05)
- Package/Assembly Qualification Test Report: LP5 & LP5G (QTR: 2014-00150 REV: 02)
- Semiconductor Qualification Test Report: PHEMT-H (QTR: 2013-00260)

DESIGN RESOURCES

- HMC797 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all HMC797 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

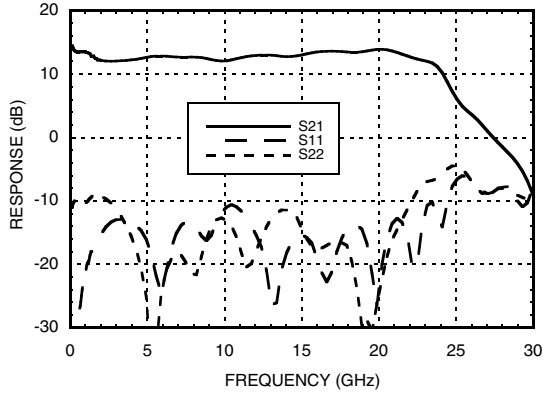
DOCUMENT FEEDBACK

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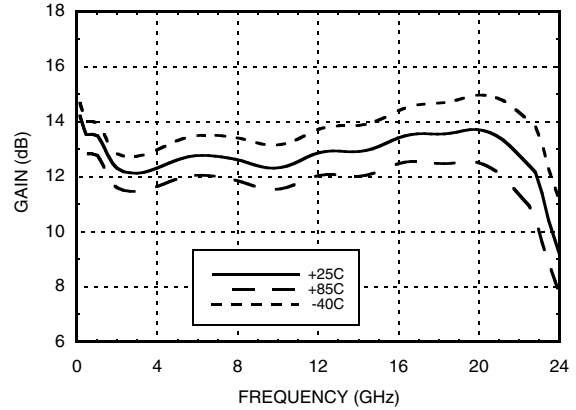


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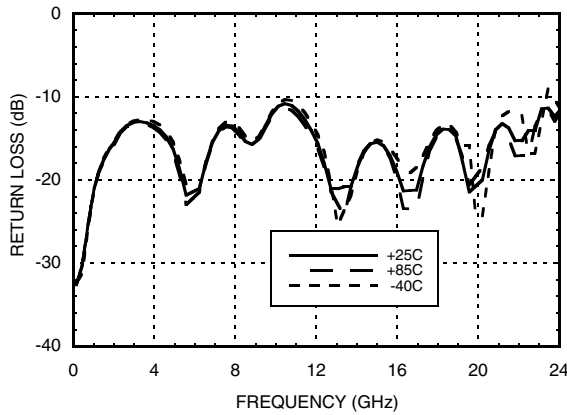
Gain & Return Loss



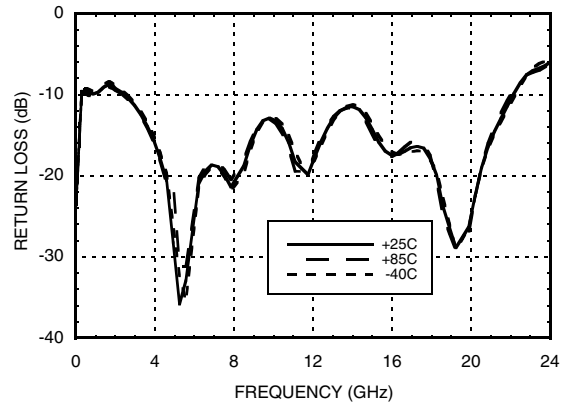
Gain vs. Temperature



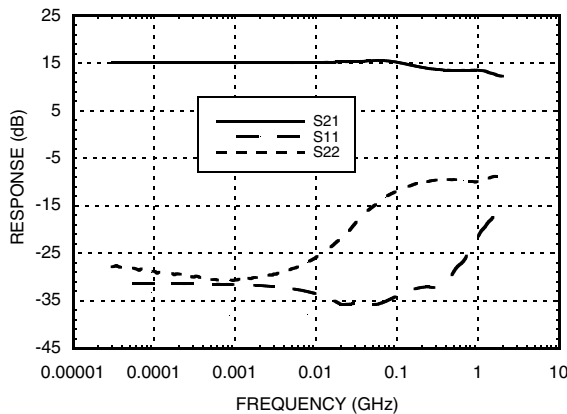
Input Return Loss vs. Temperature



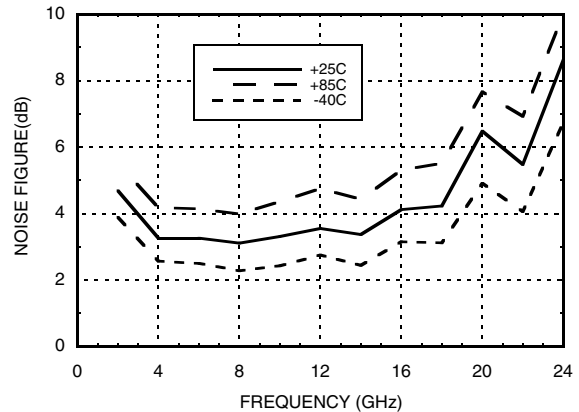
Output Return Loss vs. Temperature



Low Frequency Gain & Return Loss



Noise Figure vs. Temperature



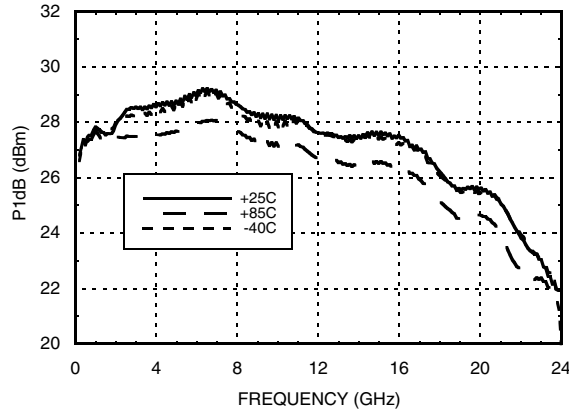
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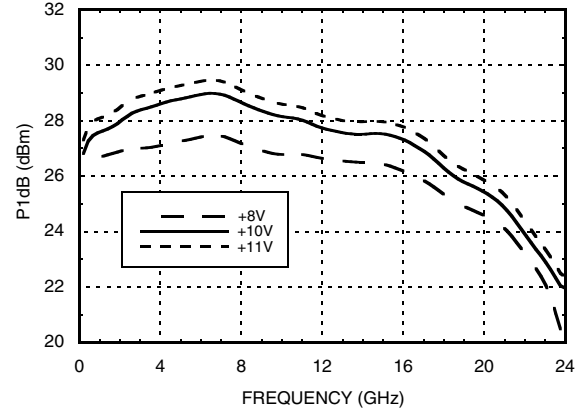


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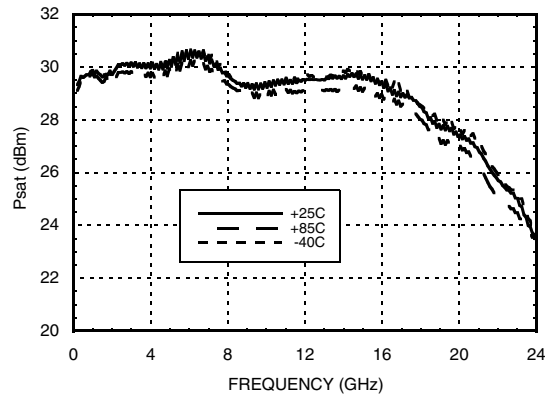
P1dB vs. Temperature



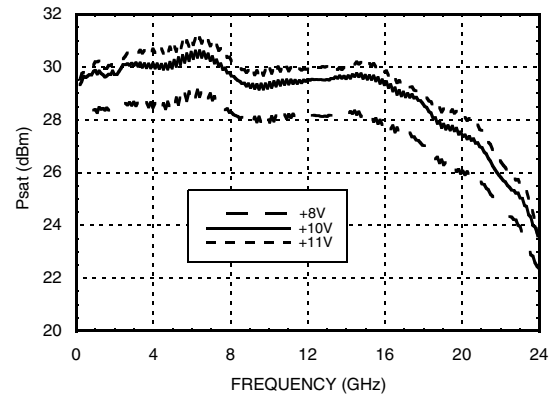
P1dB vs. Supply Voltage



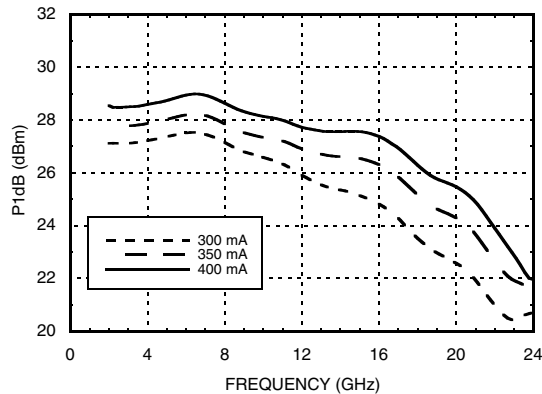
Psat vs. Temperature



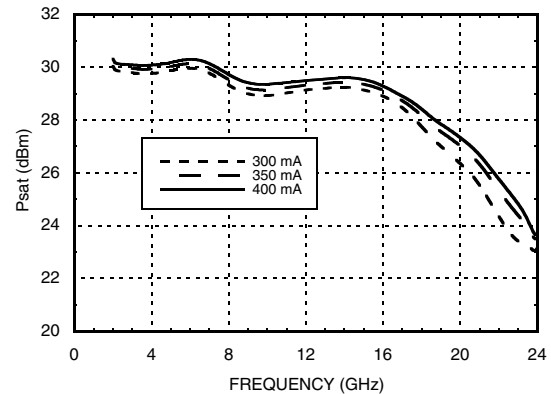
Psat vs. Supply Voltage



P1dB vs. Supply Current



Psat vs. Supply Current



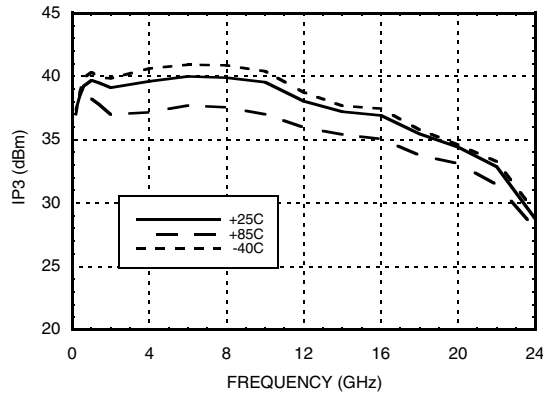
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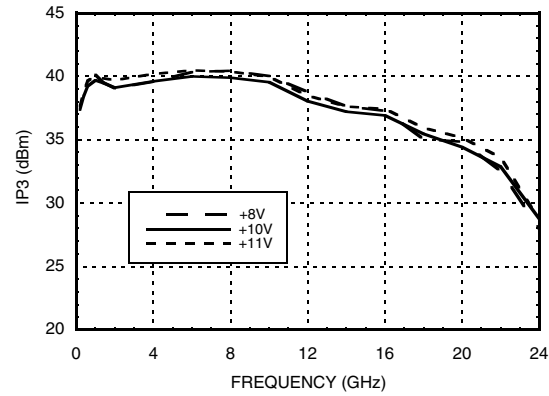
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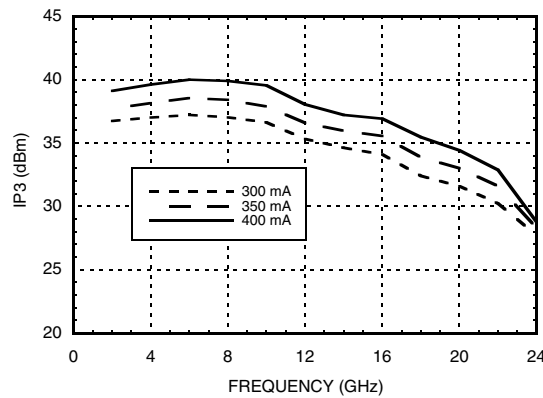
**Output IP3 vs.
Temperature @ Pout = 18 dBm / Tone**



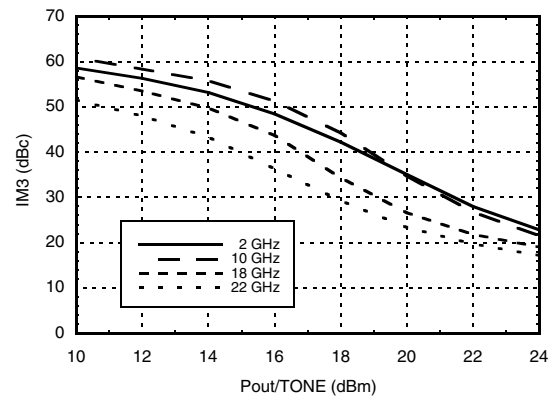
**Output IP3 vs.
Supply Voltage @ Pout = 18 dBm / Tone**



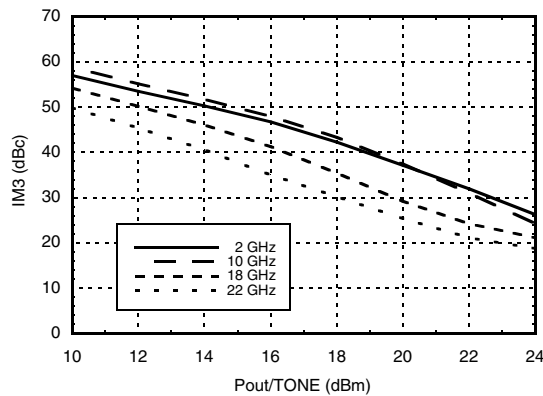
**Output IP3 vs.
Supply Currents @ Pout = 18 dBm / Tone**



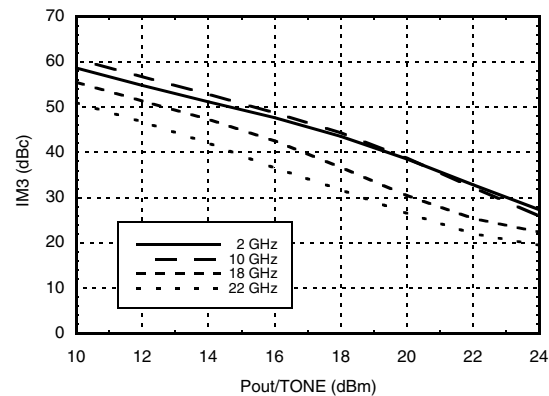
Output IM3 @ Vdd = +8V



Output IM3 @ Vdd = +10V



Output IM3 @ Vdd = +11V



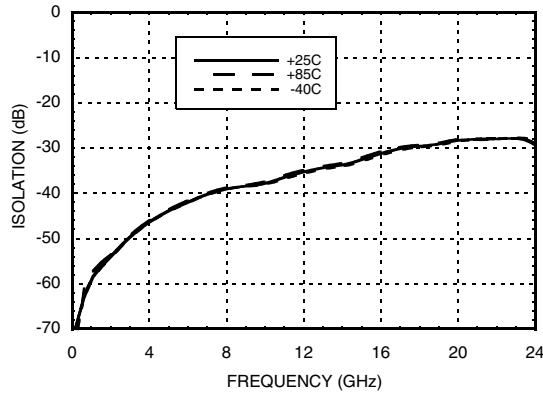
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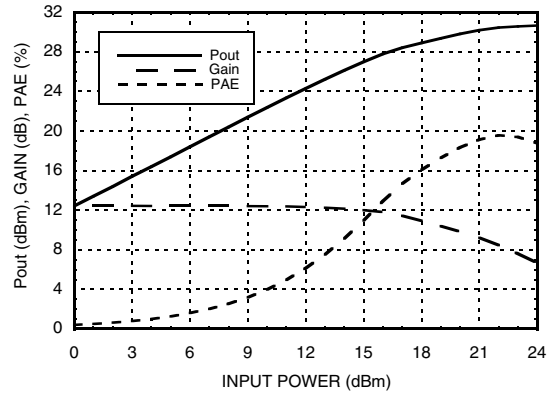


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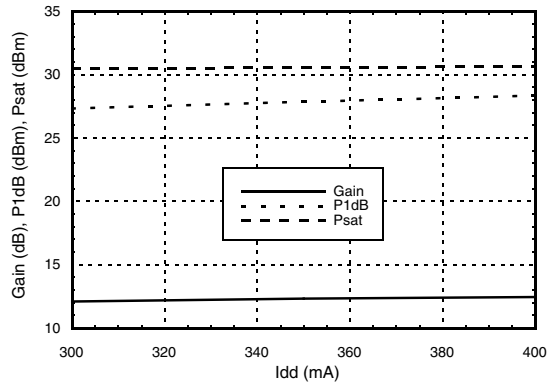
Reverse Isolation vs. Temperature



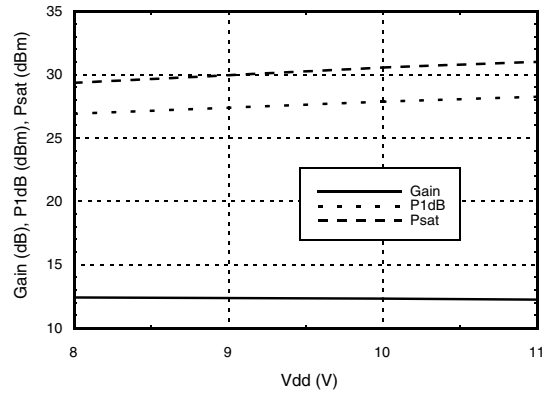
Power Compression @ 10 GHz



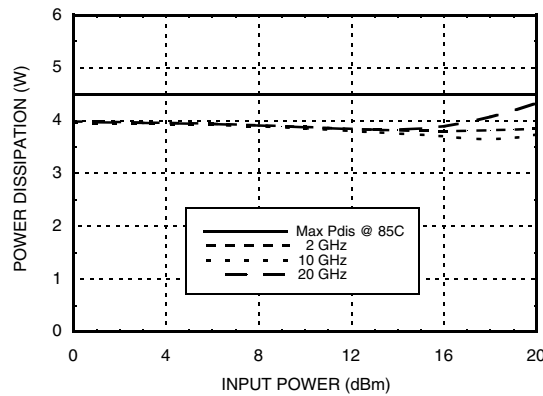
Gain & Power vs. Supply Current @ 10 GHz



Gain & Power vs. Supply Voltage @ 10 GHz



Power Dissipation



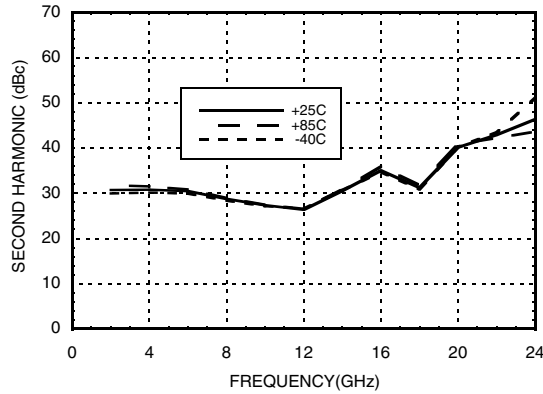
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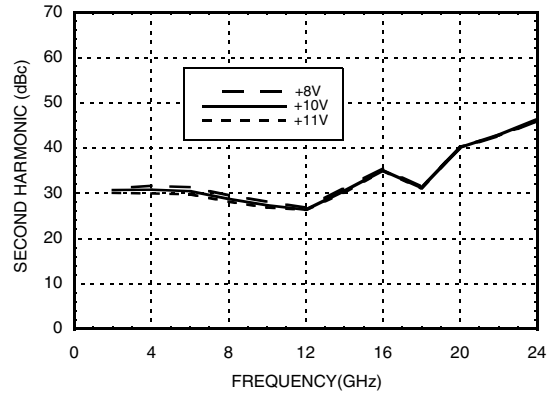


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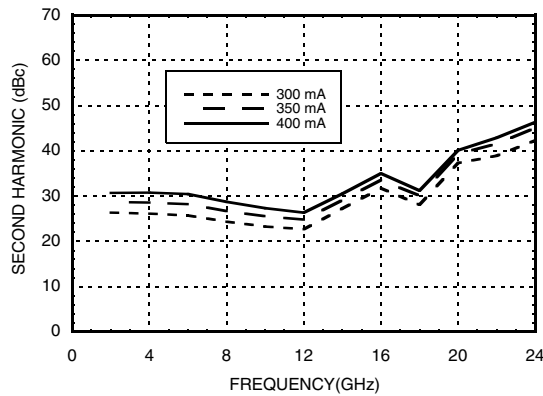
Second Harmonics vs. Temperature
@ $P_{out} = 18\text{ dBm}$, $V_{dd} = 10\text{V}$ & $V_{gg} = 3.5\text{V}$



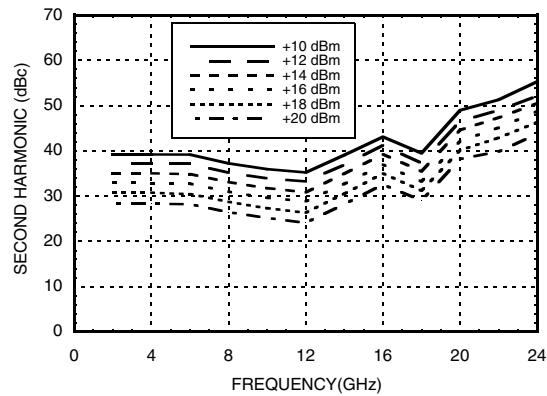
Second Harmonics vs. V_{dd}
@ $P_{out} = 18\text{ dBm}$, $I_{dd} = 400\text{ mA}$ [1]



Second Harmonics vs. I_{dd}
@ $P_{out} = 18\text{ dBm}$, $V_{gg2} = 3.5\text{V}$



Second Harmonics vs. P_{out}
 $V_{dd} = 10\text{V}$ & $V_{gg} = 3.5\text{V}$ & $I_{dd} = 400\text{ mA}$



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Absolute Maximum Ratings

Nominal Drain Supply to GND	+12.0 V
Gate Bias Voltage (V _{gg1})	-3.0 to 0 Vdc
Gate Bias Current (I _{gg1})	< +10 mA
Gate Bias Voltage (V _{gg2})	+2.0 V to (V _{dd} - 6.5 V)
Gate Bias Current (I _{gg2})	< +10 mA
Continuous P _{diss} (T = 85 °C) (derate 69 mW/°C above 85 °C)	4.5 W
RF Input Power	+27 dBm
Output Power into VSWR >7:1	+29 dBm
Storage Temperature	-65 to 150 °C
Max Peak Reflow Temperature	260 °C
ESD Sensitivity (HBM)	Class 1A

Reliability Information

Junction Temperature to Maintain 1 Million Hour MTTF	150 °C
Nominal Junction Temperature (T=85 °C, V _{dd} = 10 V)	144 °C
Thermal Resistance (channel to ground paddle)	14.6 °C/W
Operating Temperature	-40 to +85 °C

9

AMPLIFIERS - LINEAR & POWER - SMT

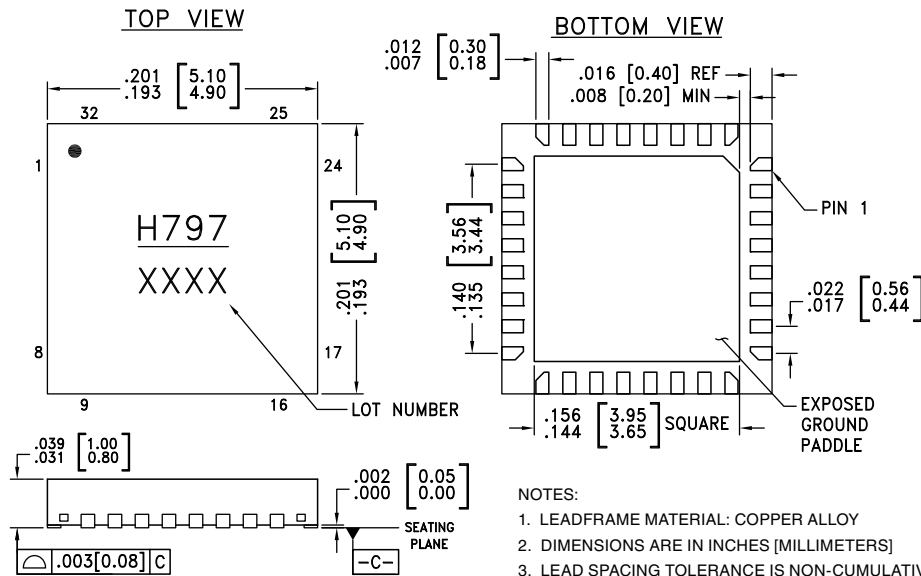


ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Typical Supply Current vs. V_{dd}

V _{dd} (V)	I _{dd} (mA)
+9	400
+10	400
+11	400

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[1]
HMC797LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 ^[2]	H797 XXXX

[1] 4-Digit lot number XXXX

[2] Max peak reflow temperature of 260 °C

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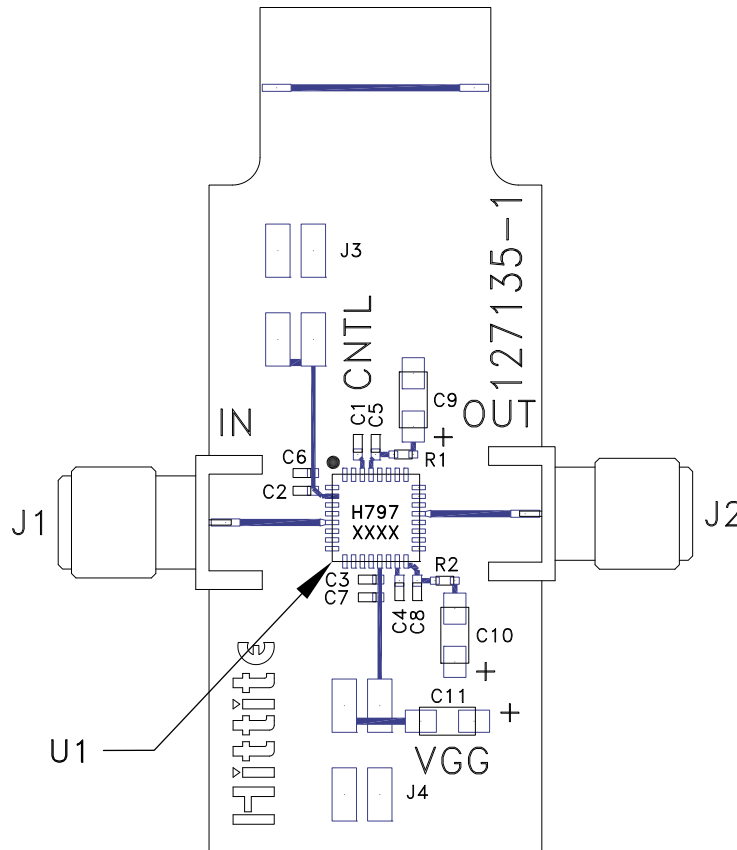
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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 6, 8, 9, 17, 20, 22, 24, 25, 32 Package Bottom	GND	These pins & exposed ground paddle must be connected to RF/DC ground.	
2	VGG2	Gate control 2 for amplifier. Attach bypass capacitor per application circuit herein. For nominal operation +3.5V should be applied to Vgg2.	
3, 7, 10 - 12, 14, 18, 19, 23, 26 - 28, 31	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
5	RFIN	This pad is DC coupled and matched to 50 Ohms. Blocking capacitor is required.	
13	VGG1	Gate control 1 for amplifier. Attach bypass capacitor per application circuit herein. Please follow "MMIC Amplifier Biasing Procedure" application note.	
15	ACG4	Low frequency termination. Attach bypass capacitor per application circuit herein.	
16	ACG3		
21	RFOUT & VDD	RF output for amplifier. Connect DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
29	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
30	ACG1		


**GaAs pHEMT MMIC
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Evaluation PCB

List of Materials for Evaluation PCB 130784 [1]

Item	Description
J1, J2	SMA Connectors
J3, J4	DC Pins
C1 - C4	100 pF Capacitor, 0402 Pkg.
C5, C8	10 kpF Capacitor, 0402 Pkg.
C9 - C11	4.7 µF Capacitor, Tantalum
R1, R2	0 OHM Resistor, 0402 Pkg
U1	HMC797LP5E Power Amplifier
PCB [2]	127135 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

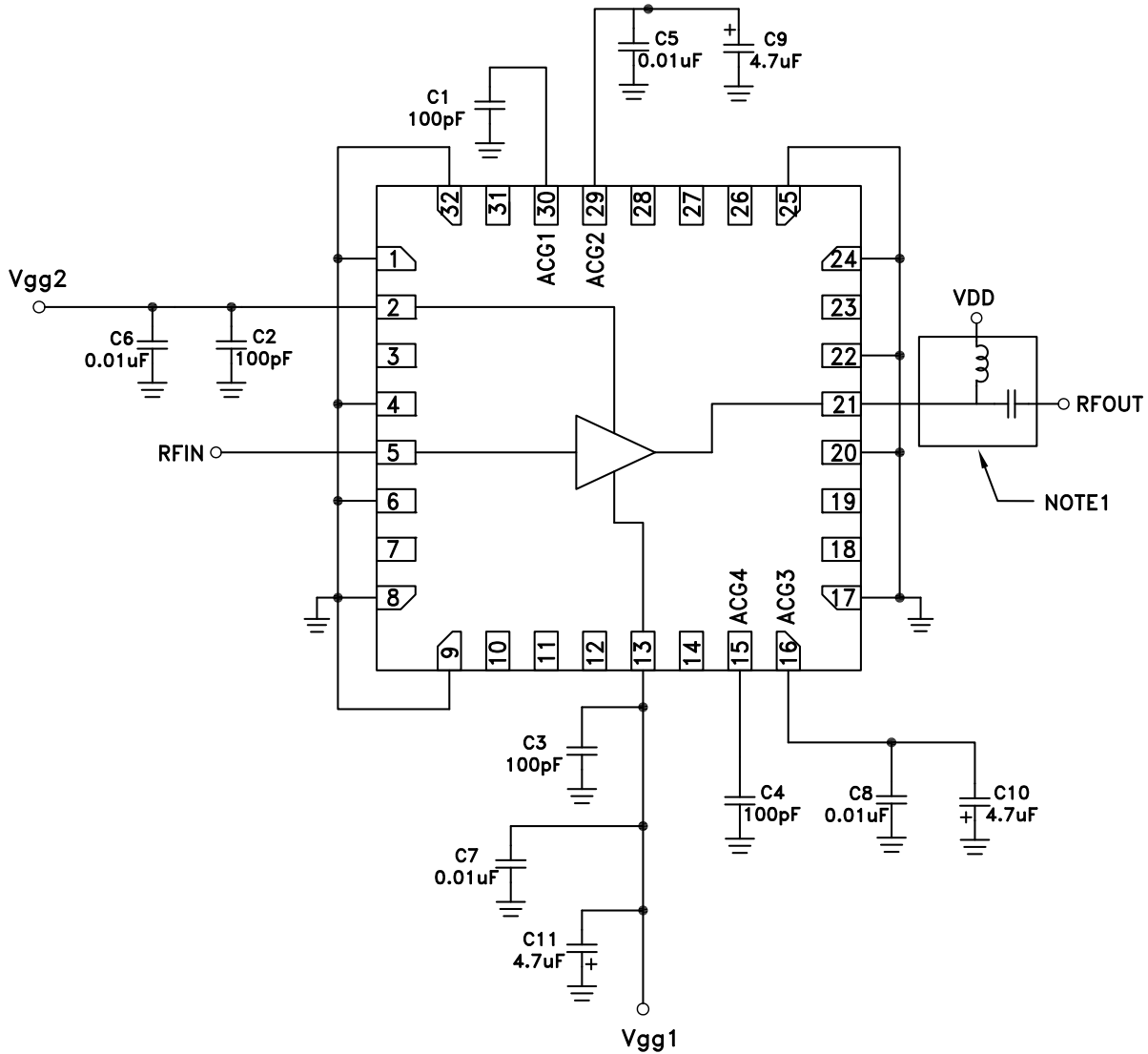
[2] Circuit Board Material: Rogers 4350 or Arlon FR4

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.



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Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

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