MAX44291/MAX44292/ MAX44294

36V, Single/Dual/Quad, Low-Noise Amplifiers with Maximum 0.5µV/°C Offset Drift

General Description

The MAX44291/MAX44292/MAX44294 are single/dual/quad low-noise, precision operational amplifiers. The low offset and low noise specifications and high supply range make the MAX44291/MAX44292/MAX44294 ideal for sensor interfaces, loop-powered systems, and various types of medical and data acquisition instruments.

The MAX44291/MAX44292/MAX44294 operate with a wide supply voltage range from a 4.5V to 36V single supply or dual ±2.25V to ±18V supplies, and consume only 1.2mA/channel (typ). The MAX44291 features a shutdown input that reduces the supply current to 1µA/channel (typ) when in shutdown mode.

The rail-to-rail output swing maximizes the dynamic range when driving high-resolution ADCs even with low supply voltage. These devices achieve 10MHz of gain-bandwidth product.

The MAX44291/MAX44292/MAX44294 are available in 8-pin µMAX® (single), 8-pin SO (dual), and 14-pin SO (quad) packages and are specified over the -40°C to +125°C automotive temperature range.

***Ordering Information* appears at end of data sheet.**

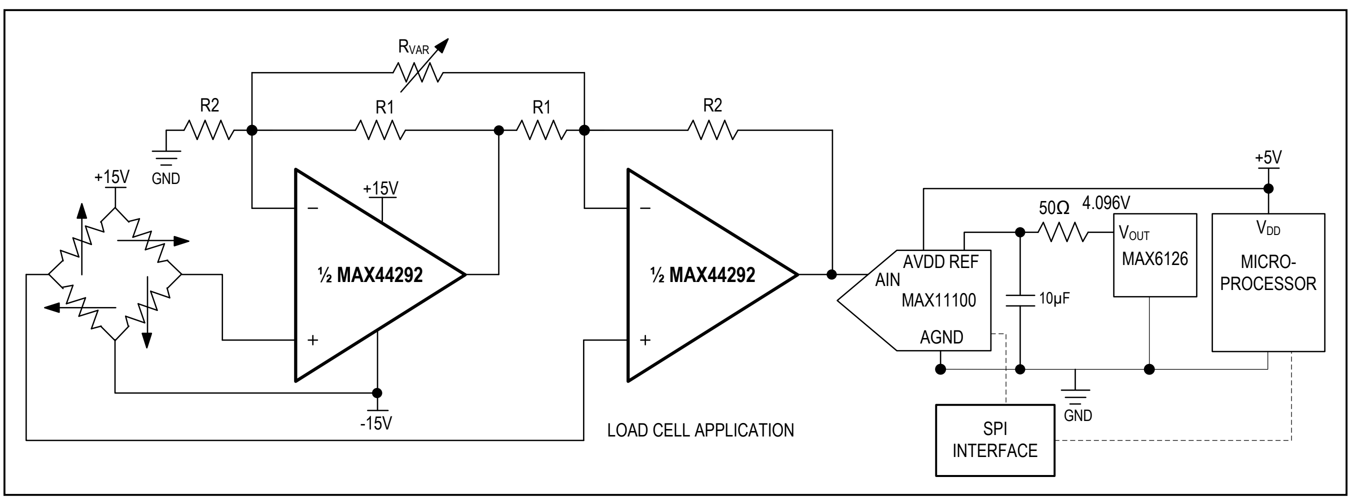
Benefits and Features

- Low Input Noise and High Bandwidth to Drive Precision ADCs
  - 4.9nV/√Hz Low Input Noise
  - 10MHz Gain-Bandwidth Product
- Low Input Offset Ensures Accurate Results Over Temperature
  - 125µV (max) Low Input Offset Voltage
  - 0.5µV/°C (max) Offset Drift
- Low 1.2mA Quiescent Current (Per Channel) Does Not Break the Power Budget
- ESD Protection Provides Robust Front-End
  - ±8kV Human Body Model
  - ±1kV Charged Device Model
- Wide Supply for High-Voltage Front-Ends
  - Single 4.5V to 36V or Dual ±2.25V to ±18V Supply Ranges
- 8-Pin µMAX and 8-/14-Pin SO Packages Save Board Space

Applications

- Portable Logic Controllers
- Instrumentation
- Test and Measurement Systems
- Sensor Interfaces

Typical Application Circuit



Absolute Maximum Ratings

V_{DD} to V_{SS} .... -0.3V to +40V
Common-Mode Input Voltage .... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
SHDN .... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Differential Input Voltage (IN_+ - IN_-) 10V
OUT_ to V_{SS} .... -0.3V to (V_{DD} + 0.3V)
Continuous Input Current (any pin) .... ±20mA
Output Short-Circuit Duration (OUT_) 1s
Continuous Power Dissipation (T_A = +70°C)
μMAX (derate 4.8mW/°C above + 70°C) 387.8mW
8-Pin SO (derate 7.40mW/°C above + 70°C) 588.20mW
14-Pin SO (derate 12.2mW/°C above + 70°C) 975.60mW
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

μMAX
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 206.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 42°C/W
8-SO
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 136°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 38°C/W
14-SO
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 82°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 32°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = +15V, V_{SS} = -15V, R_L = 10kΩ to V_{GND} = 0V, V_{IN_+} = V_{IN_-} = V_{GND} = 0V, V_{SHDN} = 0V (MAX44291 only), T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage Range	V_{DD}	Guaranteed by PSRR		4.5		36	V
Supply Current	I_{DD}	R_L = ∞	T_A = +25°C		1.2	1.9	mA
			-40°C ≤ T_A ≤ +125°C			2.1	
Power-Supply Rejection Ratio	PSRR	T_A = +25°C		125	140		dB
		-40°C ≤ T_A ≤ +125°C		120			
SHUTDOWN (MAX44291 Only)							
Shutdown Input Voltage	V_{SHDN}	Device disabled		V_{DD} - 0.35		V_{DD}	V
		Device enabled		V_{SS}		V_{DD} - 3.0	
Shutdown Current	I_{SHDN}	V_{SHDN} = V_{DD}			1		μA
DC SPECIFICATIONS							
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test		V_{SS} + 1.8		V_{DD} - 1.4	V
Common-Mode Rejection Ratio	CMRR	V_{SS} + 1.8V ≤ V_{CM} ≤ V_{DD} - 1.4V, T_A = +25°C		120	135		dB
		V_{SS} + 2V ≤ V_{CM} ≤ V_{DD} - 1.6V, -40°C ≤ T_A ≤ +125°C		110			

Electrical Characteristics (continued)

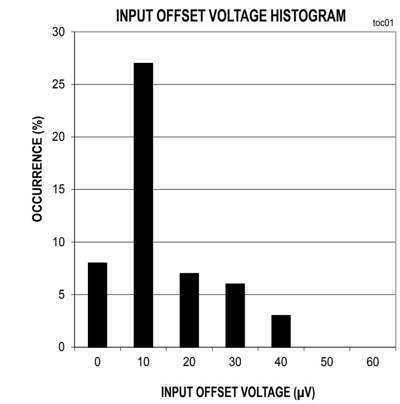
(V_{DD} = +15V, V_{SS} = -15V, R_L = 10kΩ to V_{GND} = 0V, V_{IN_+} = V_{IN_-} = V_{GND} = 0V, V_{SHDN} = 0V (MAX44291 only), T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

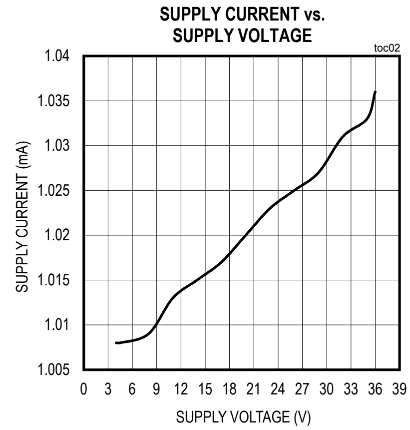
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C			30	125	μV
		-40°C ≤ T_A ≤ +125°C				165	
Input Offset Voltage Drift	TCV_{OS}	(Note 3)			0.2	0.5	μV/°C
Input Bias Current	I_B	T_A = +25°C			6	25	nA
		-40°C ≤ T_A ≤ +125°C				55	
Input Offset Current	I_{OS}	T_A = +25°C			4	12	nA
		-40°C ≤ T_A ≤ +125°C				30	
Open-Loop Gain	A_{VOL}	V_{SS} + 0.2V ≤ V_{OUT} ≤ V_{DD} - 0.2V, R_L = 10kΩ	T_A = +25°C	130	140		dB
			-40°C ≤ T_A ≤ +125°C	125			
Output Voltage Swing	V_{OH}	V_{DD} - V_{OUT}	T_A = +25°C		100	160	mV
			-40°C ≤ T_A ≤ +125°C			220	
	V_{OL}	V_{OUT} - V_{SS}	T_A = +25°C		100	160	
			-40°C ≤ T_A ≤ +125°C			220	
Output Short-Circuit Current	I_{SC}	To V_{DD} or V_{SS} (1s max)			60		mA
AC SPECIFICATIONS							
Input Voltage-Noise Density	e_N	f = 1kHz			4.9		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f ≤ 10Hz			288		nV_{P-P}
Input Current-Noise Density	i_N	f = 1kHz			0.89		pA/√Hz
Gain-Bandwidth Product	GBW	V_{IN} = $100mV_{P-P}$			10		MHz
Slew Rate	SR	A_V = 1V/V, V_{OUT} = $2V_{P-P}$			5		V/μs
Settling Time	t_S	To 0.01%, V_{OUT} = $10V_{P-P}$, C_L = 100pF, A_V = 1V/V			2		μs
Total Harmonic Distortion Plus Noise	THD+N	f = 1kHz, V_{OUT} = $2V_{P-P}$, A_V = 1V/V			-110		dB
Capacitive Loading	C_L	No sustained oscillation, A_V = 1V/V			100		pF

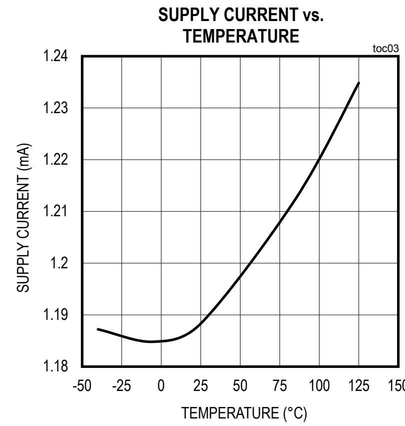
Note 2: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 3: Guaranteed by design.

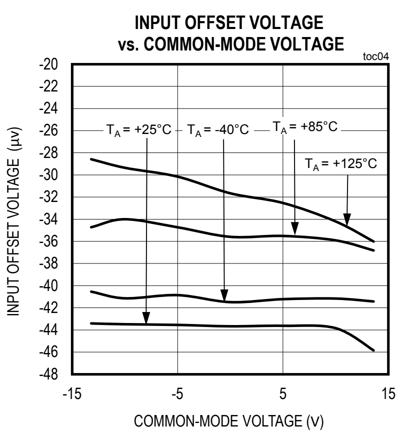
Typical Operating Characteristics

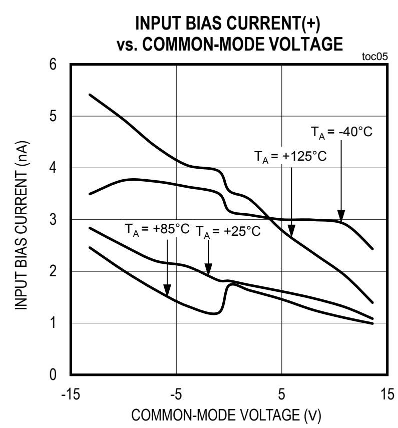
(V_{DD} = +15V, V_{SS} = -15V, R_L = 10kΩ connected to GND. V_{IN_+} = V_{IN_-} = V_{GND} = 0V, V_{SHDN} = 0V, T_A = +25°C, unless otherwise specified.)

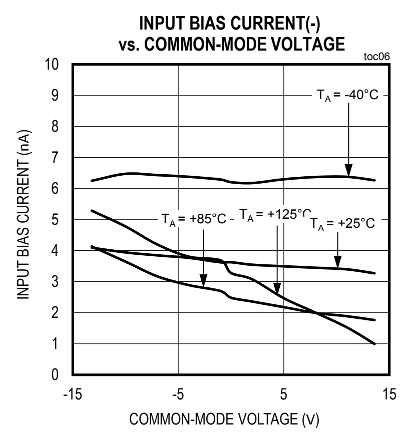


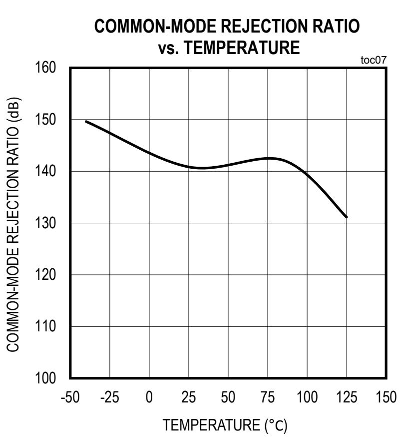


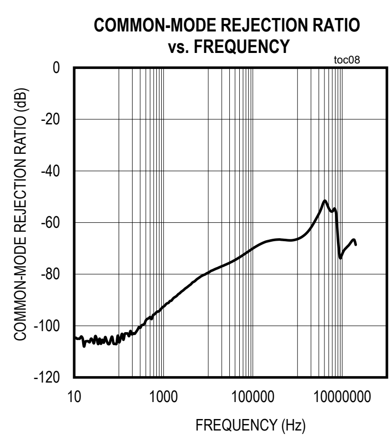








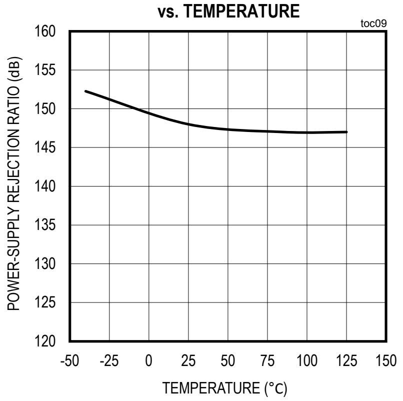




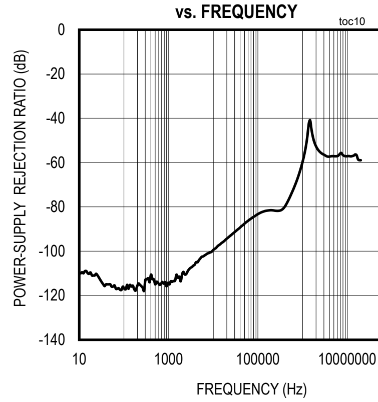
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V, R_L = 10kΩ connected to GND. V_{IN_+} = V_{IN_-} = V_{GND} = 0V, V_{SHDN} = 0V, T_A = +25°C, unless otherwise specified.)

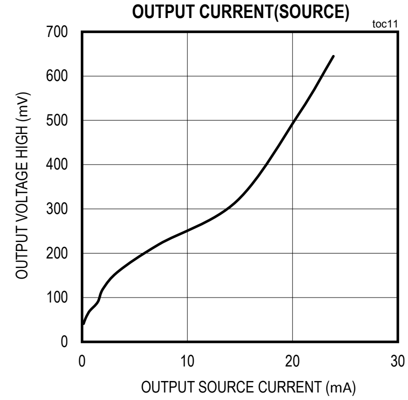
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



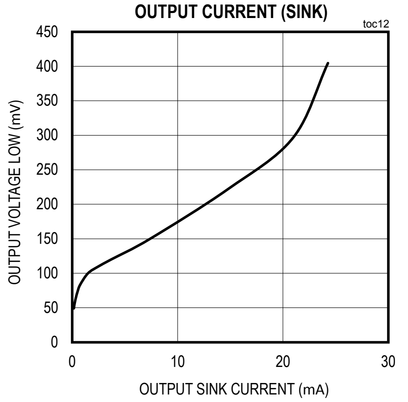
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



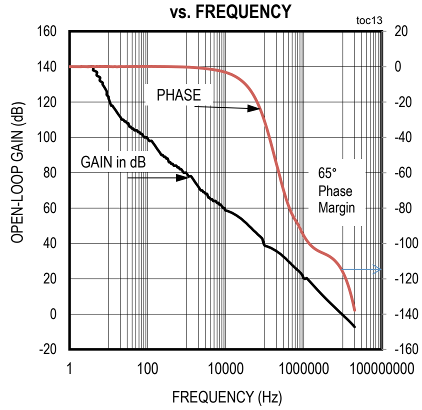
OUTPUT VOLTAGE HIGH vs. OUTPUT CURRENT(SOURCE)



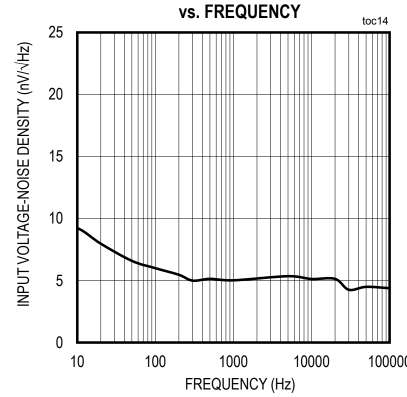
OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT (SINK)



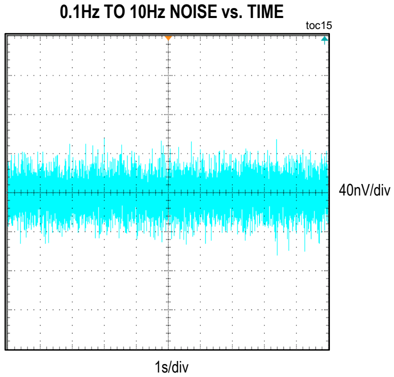
OPEN-LOOP GAIN vs. FREQUENCY



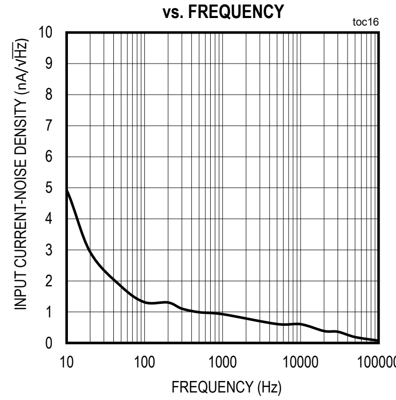
INPUT VOLTAGE-NOISE DENSITY vs. FREQUENCY



0.1Hz TO 10Hz NOISE vs. TIME



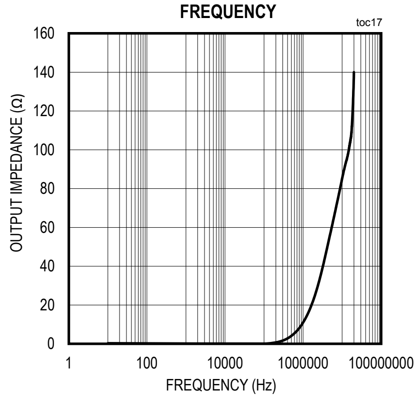
INPUT CURRENT-NOISE DENSITY vs. FREQUENCY



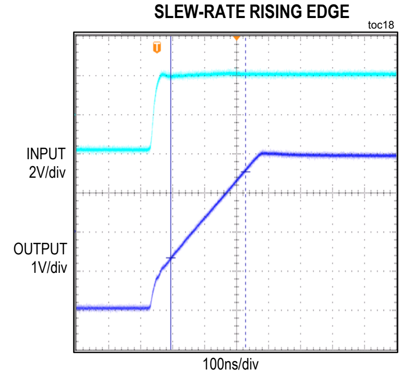
Typical Operating Characteristics (continued)

(V_{DD} = +15V, V_{SS} = -15V, R_L = 10kΩ connected to GND. V_{IN_+} = V_{IN_-} = V_{GND} = 0V, V_{SHDN} = 0V, T_A = +25°C, unless otherwise specified.)

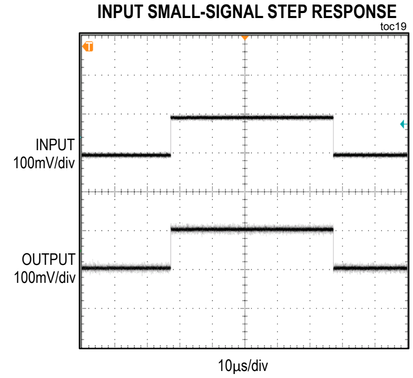
OUTPUT IMPEDANCE vs. FREQUENCY



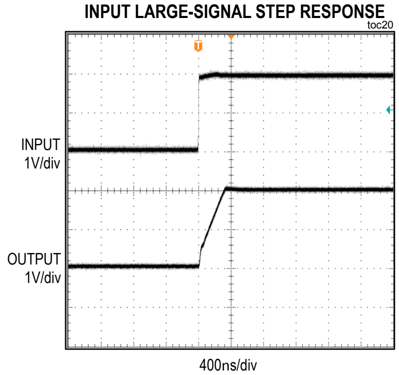
SLEW-RATE RISING EDGE



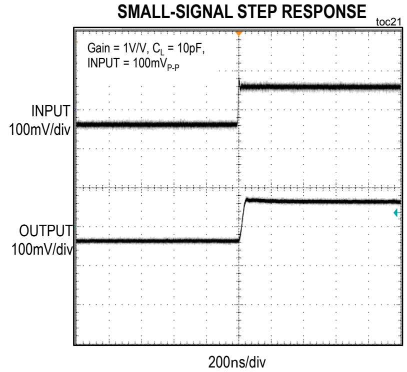
INPUT SMALL-SIGNAL STEP RESPONSE



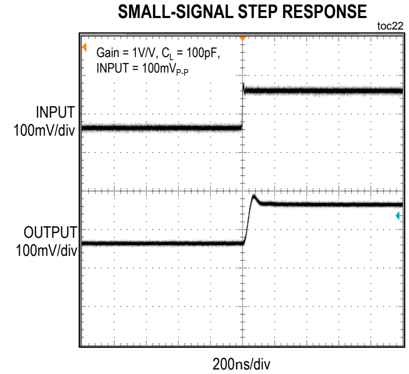
INPUT LARGE-SIGNAL STEP RESPONSE



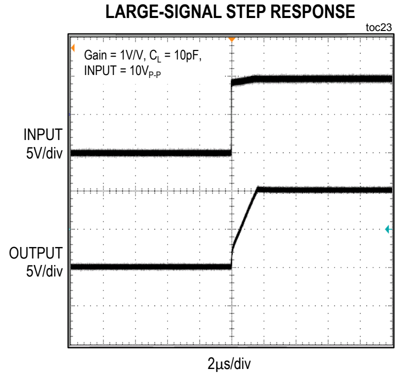
SMALL-SIGNAL STEP RESPONSE



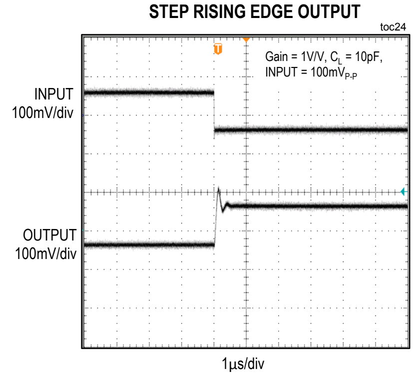
SMALL-SIGNAL STEP RESPONSE



LARGE-SIGNAL STEP RESPONSE

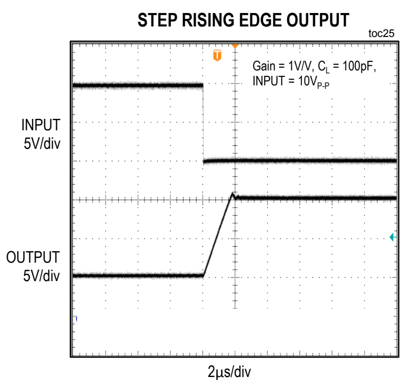


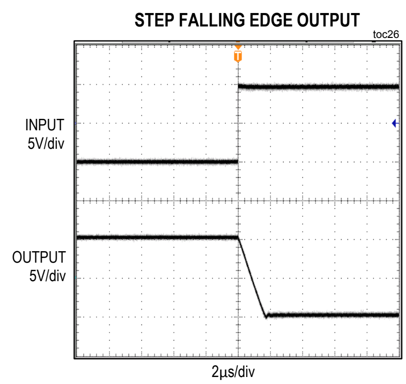
STEP RISING EDGE OUTPUT

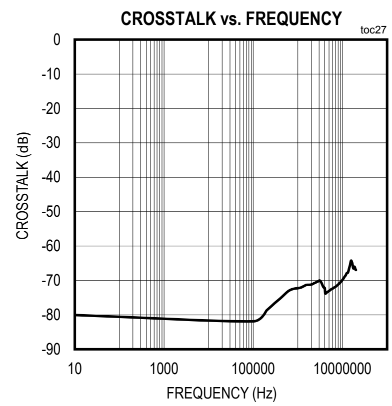


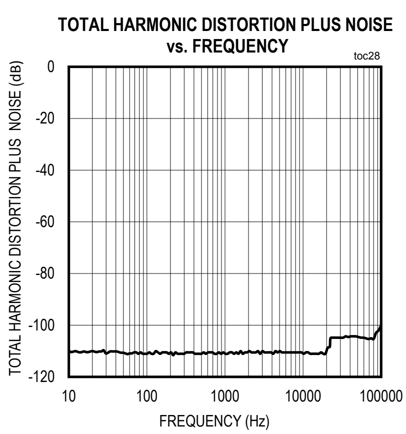
Typical Operating Characteristics (continued)

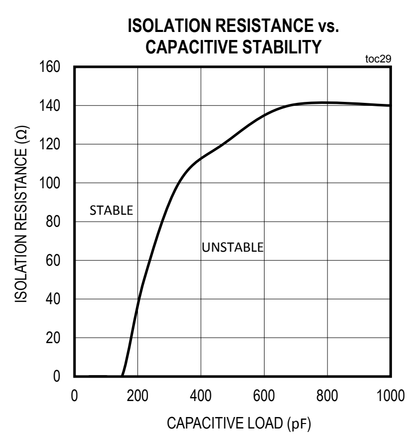
(V_{DD} = +15V, V_{SS} = -15V, R_L = 10kΩ connected to GND. V_{IN_+} = V_{IN_-} = V_{GND} = 0V, V_{SHDN} = 0V, T_A = +25°C, unless otherwise specified.)

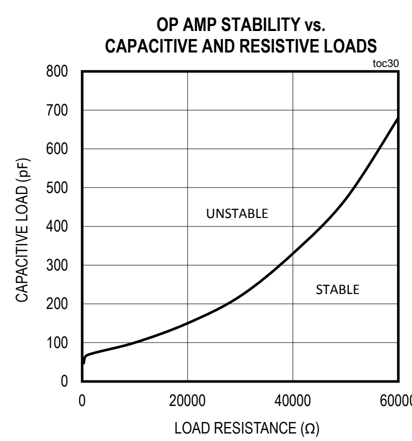


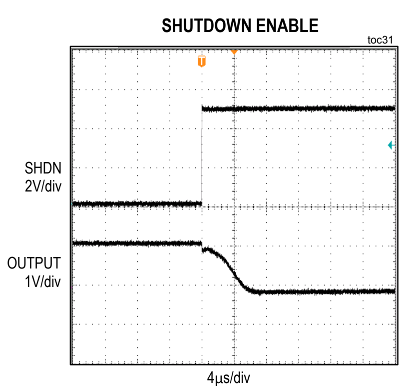


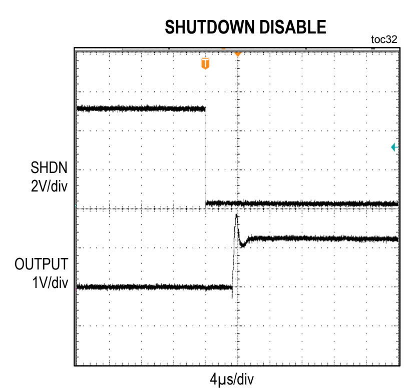




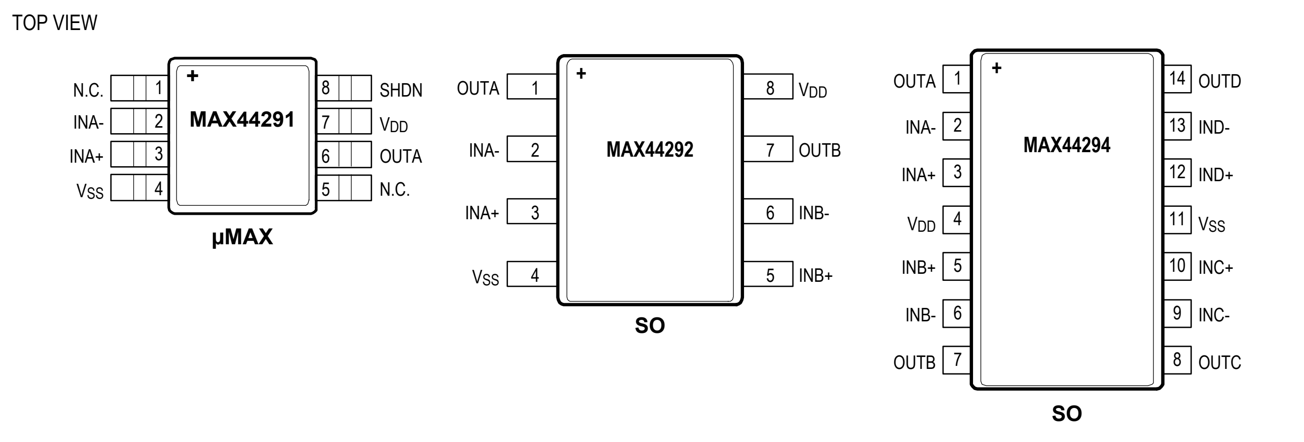








Pin Configurations



Pin Description

PIN			NAME	FUNCTION
MAX44291	MAX44292	MAX44294		
µMAX	8 SO	14 SO		
1, 5	—	—	N.C.	No Connection. Not internally connected.
2	2	2	INA-	Channel A Negative Input
3	3	3	INA+	Channel A Positive Input
4	4	11	V_{SS}	Negative Supply Voltage
6	1	1	OUTA	Channel A Output
7	8	4	V_{DD}	Positive Supply Voltage
8	—	—	SHDN	Active-High Shutdown Input
—	5	5	INB+	Channel B Positive Input
—	6	6	INB-	Channel B Negative Input
—	7	7	OUTB	Channel B Output
—	—	8	OUTC	Channel C Output
—	—	9	INC-	Channel C Negative Input
—	—	10	INC+	Channel C Positive Input
—	—	12	IND+	Channel D Positive Input
—	—	13	IND-	Channel D Negative Input
—	—	14	OUTD	Channel D Output

Detailed Description

The MAX44291/MAX44292/MAX44294 are precision, low-noise, 10MHz bandwidth amplifiers with exceptional distortion performance. They are designed in a new 36V, high-speed complementary BiCMOS process that is optimized for excellent AC dynamic performance combined with high-voltage operation.

The MAX44291/MAX44292/MAX44294 are unity-gain stable and operate either with single-supply voltage from 4.5V to 36V or with dual supplies from ±2.25V to ±18V.

Applications Information

High Operating Supply Voltage Range

The MAX44291/MAX44292/MAX44294 operate with a wide voltage range from single supply +4.5V to +36V or dual supplies from ±2.25V to ±18V. These devices consume only 1.2mA (typical) of supply current per channel. Although the MAX44291/MAX44292/MAX44294 support high-voltage operation with excellent performance, the devices also operate in many battery-operated or portable equipment applications at 5V.

Input Protection

The MAX44291/MAX44292/MAX44294 have a typical ESD protection scheme with diodes from input, output, and shutdown pins to either rails. Also, as shown in Figure 1, the protection scheme shows diodes and a resistor string between the inputs to protect the IC from large differential inputs. Input series resistors act as current-limiting resistors when a large differential voltage is accidentally applied.

Rail-to-Rail Output Stage

The MAX44291/MAX44292/MAX44294 output stage swings to within 100mV (typ) of either power-supply rail with a 10kΩ load to ground and provides a 10MHz GBW with a 5V/μs slew rate. The devices are unity-gain stable, and can drive a 100pF capacitive load without compromising stability. Stability with higher capacitive loads can be improved by adding an isolation resistor in series with the op-amp output. This resistor improves the circuit's phase margin by isolating the load capacitor from the amplifier's output. The graph in the *Typical Operating Characteristics* shows a profile of the isolation resistor and capacitive load values that maintain the devices in the stable region.

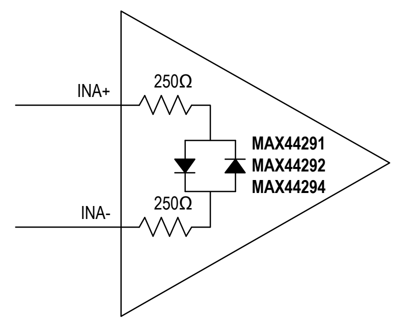


Figure 1. Showing Input Differential Protection Scheme

Shutdown (MAX44291 Only)

The MAX44291 shutdown input is referenced to the positive supply. See the *Electrical Characteristics* table for the proper levels of functionality. A high level (above V_{DD} - 0.35V) disables the op amp and puts the output into high-impedance state. A low level (below V_{DD} - 3V) enables the device. As an example, if the op amp is powered with dual supplies of ±15V, the device is enabled when the shutdown voltage is at or below 12V. The device is disabled when the shutdown voltage is at or above 14.65V. If the op amp is powered with 36V single supply, the device is enabled when the shutdown voltage is at or below 33V. The device is disabled when the shutdown voltage is at or above 35.65V. This input must be connected to either a valid high or low voltage. Do not leave it unconnected.

When in shutdown mode, the amplifier consumes only 1.8μA (typical) of supply current.

Power Supplies and Layout

The MAX44291/MAX44292/MAX44294 operate with dual supplies from ±2.25V to ±18V or with a single supply from +4.5V to +36V with respect to ground. When used with dual supplies, bypass both V_{DD} and V_{SS} with 0.1μF capacitor to ground closer to V_{DD} and 10μF capacitor to ground closer to where the power supply connection is made. When used with a single supply, bypass V_{DD} with a 0.1μF and 10μF capacitors to ground as explained above. Careful layout technique helps optimize performance by decreasing the amount of stray capacitance at the amplifier inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the amplifier pins.

Electrostatic Discharge (ESD)

The MAX44291/MAX44292/MAX44294 have built-in circuits to protect from electrostatic discharge (ESD) events. An ESD event produces a short, high-voltage pulse that is transformed into a short current pulse once it discharges through the device. The built-in protection circuit provides a current path around the op amp that prevents it from being damaged. The energy absorbed by the protection circuit is dissipated as heat.

The MAX44291/MAX44292/MAX44294 guarantee ESD protection up to 8kV with Human Body Model (HBM). The Human Body Model simulates the ESD phenomenon wherein a charged body directly transfers its accumulated electrostatic charge to the ESD-sensitive device. A common example of this phenomenon is when a person accumulates static charge by walking across a carpet and then transferring all of the charge to an ESD-sensitive device by touching it.

Not all ESD events involve the transfer of charge into the device. Electrostatic discharge from a charged device to another conductive body at lower potential is also a form of ESD. Such an ESD event is known as Charged Device Model (CDM) ESD, which can be even more destructive than HBM ESD (despite its shorter pulse duration) because of its high current. The MAX44291/MAX44292/MAX44294 guarantee CDM ESD protection up to 1kV.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX44291AUA+	-40°C to +125°C	8 μMAX
MAX44292ASA+	-40°C to +125°C	8 SO
MAX44294ASD+	-40°C to +125°C	14 SO

+Denotes lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 μMAX	U8+1	**21-0036**	**90-0092**
8 SO	S8+2	**21-0041**	**90-0096**
14 SO	S14M+4	**21-0041**	**90-0112**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/14	Initial release	—
1	5/15	Added the MAX44292 and MAX44294 to data sheet.	1–12

