International IR Rectifier

IRF3707ZCSPbF
IRF3707ZCLPbF

Applications

- High Frequency Synchronous Buck
  Converters for Computer Processor Power
- Lead-Free

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ max	Q_g
30V	9.5mΩ	9.7nC

Benefits

- Low $R_{DS(on)}$ at 4.5V V_{GS}
- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage
  and Current

D²Pak   TO-262
IRF3707ZCSPbF   IRF3707ZCLPbF
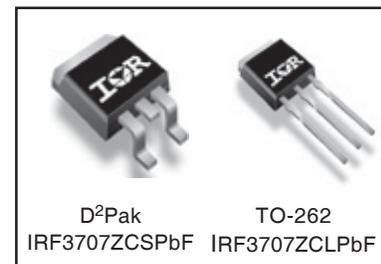
Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	± 20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	59⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	42⑥	
I_{DM}	Pulsed Drain Current ①	230	
P_D @T_C = 25°C	Maximum Power Dissipation	57	W
P_D @T_C = 100°C	Maximum Power Dissipation	28	
	Linear Derating Factor	0.38	W/°C
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	2.653	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ⑤	——	40	

Notes ① through ⑥ are on page 11

Static @ T$_J$ = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV$_{DSS}$	Drain-to-Source Breakdown Voltage	30	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔBV$_{DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.023	——	mV/°C	Reference to 25°C, I$_D$ = 1mA
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	7.5	9.5	mΩ	V$_{GS}$ = 10V, I$_D$ = 21A ③
		——	10	12.5		V$_{GS}$ = 4.5V, I$_D$ = 17A ③
V$_{GS(th)}$	Gate Threshold Voltage	1.35	1.80	2.25	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 25µA
ΔV$_{GS(th)}$/ΔT$_J$	Gate Threshold Voltage Coefficient	——	-5.3	——	mV/°C	
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	1.0	µA	V$_{DS}$ = 24V, V$_{GS}$ = 0V
		——	——	150		V$_{DS}$ = 24V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	100	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V$_{GS}$ = -20V
gfs	Forward Transconductance	81	——	——	S	V$_{DS}$ = 15V, I$_D$ = 17A
Q$_g$	Total Gate Charge	——	9.7	15		
Q$_{gs1}$	Pre-Vth Gate-to-Source Charge	——	2.8	——		V$_{DS}$ = 15V
Q$_{gs2}$	Post-Vth Gate-to-Source Charge	——	1.0	——	nC	V$_{GS}$ = 4.5V
Q$_{gd}$	Gate-to-Drain Charge	——	3.4	——		I$_D$ = 17A
Q$_{godr}$	Gate Charge Overdrive	——	2.5	——		See Fig. 16
Q$_{sw}$	Switch Charge (Q$_{gs2}$ + Q$_{gd}$)	——	4.4	——		
Q$_{oss}$	Output Charge	——	6.2	——	nC	V$_{DS}$ = 16V, V$_{GS}$ = 0V
t$_{d(on)}$	Turn-On Delay Time	——	9.8	——		V$_{DD}$ = 15V, V$_{GS}$ = 4.5V ③
t$_r$	Rise Time	——	41	——		I$_D$ = 17A
t$_{d(off)}$	Turn-Off Delay Time	——	12	——	ns	Clamped Inductive Load
t$_f$	Fall Time	——	3.6	——		
C$_{iss}$	Input Capacitance	——	1210	——		V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	260	——	pF	V$_{DS}$ = 15V
C$_{rss}$	Reverse Transfer Capacitance	——	130	——		ƒ = 1.0MHz

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E$_{AS}$	Single Pulse Avalanche Energy②	——	40	mJ
I$_{AR}$	Avalanche Current ①	——	23	A
E$_{AR}$	Repetitive Avalanche Energy ①	——	5.7	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	59⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I$_{SM}$	Pulsed Source Current (Body Diode) ①	——	——	230		
V$_{SD}$	Diode Forward Voltage	——	——	1.0	V	T$_J$ = 25°C, I$_S$ = 17A, V$_{GS}$ = 0V ③
t$_{rr}$	Reverse Recovery Time	——	14	21	ns	T$_J$ = 25°C, I$_F$ = 17A, V$_{DD}$ = 15V
Q$_{rr}$	Reverse Recovery Charge	——	5.2	7.8	nC	di/dt = 100A/µs ③

IRF3707ZCS/LPbF

International **IOR** Rectifier
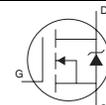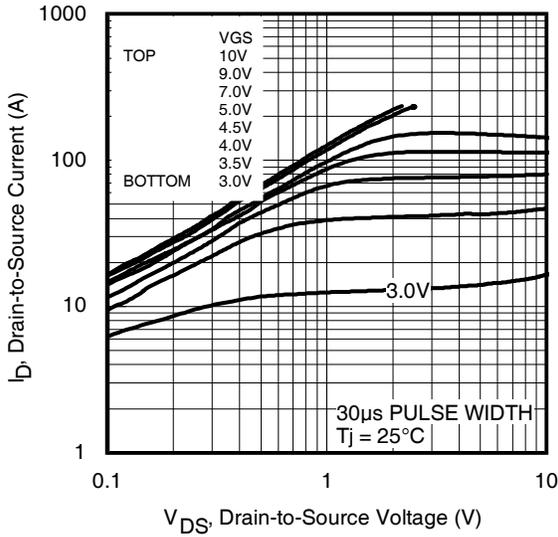
**Fig 1.** Typical Output Characteristics
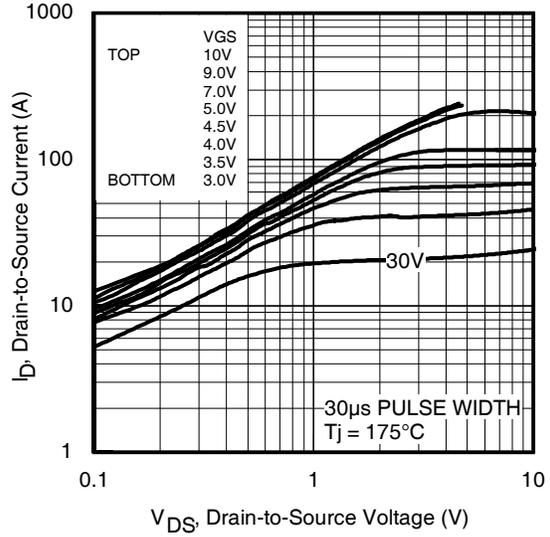
**Fig 2.** Typical Output Characteristics
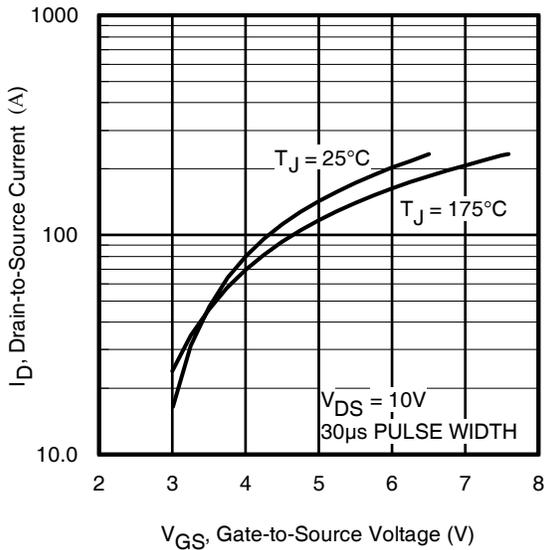
**Fig 3.** Typical Transfer Characteristics
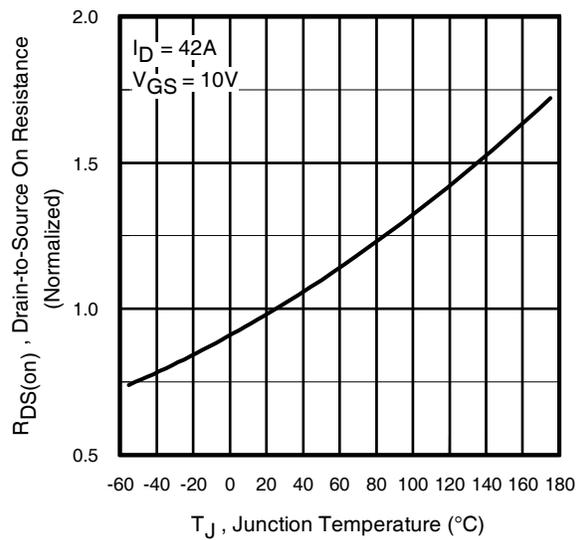
Fig 4. Normalized On-Resistance
vs. Temperature

IRF3707ZCS/LPbF
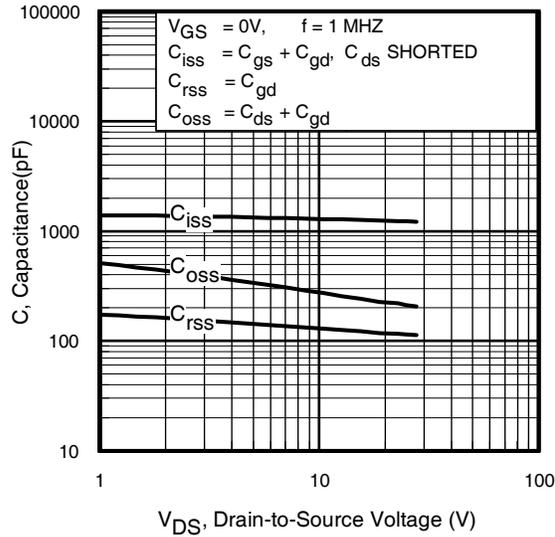
Fig 5. Typical Capacitance vs. Drain-to-Source Voltage
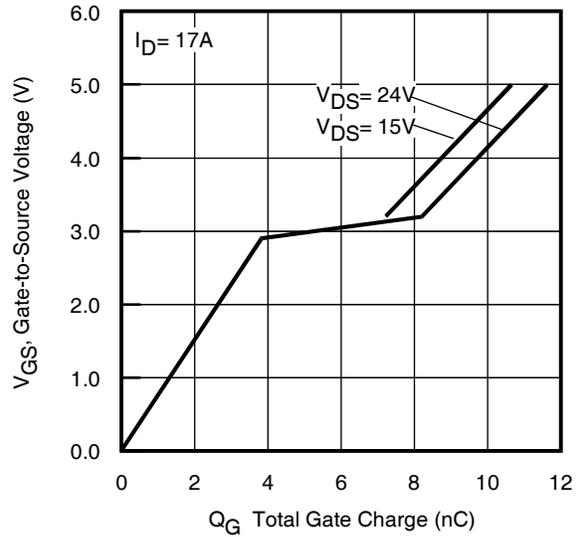


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage
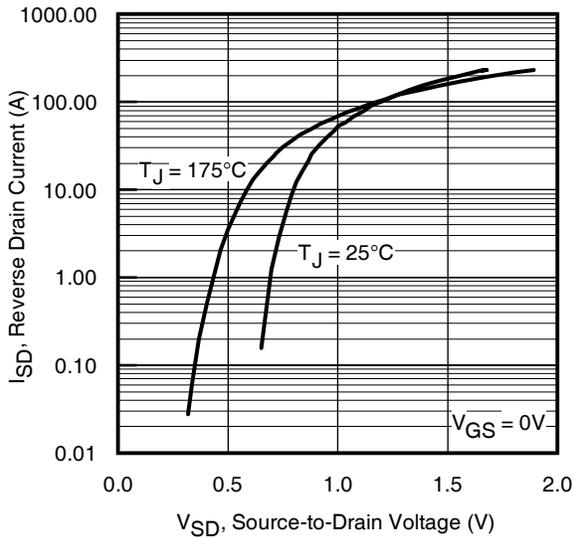


Fig 7. Typical Source-Drain Diode Forward Voltage
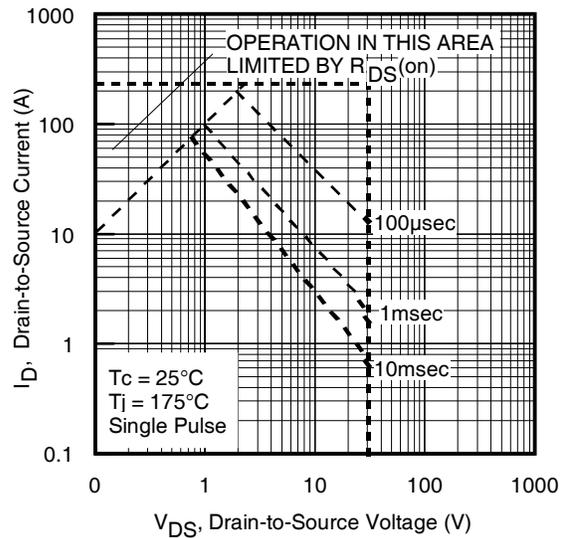
Fig 8. Maximum Safe Operating Area
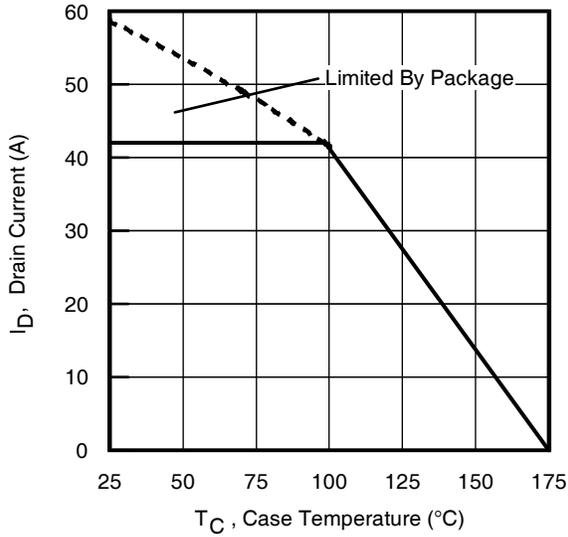
IRF3707ZCS/LPbF

Fig 9. Maximum Drain Current vs. Case Temperature
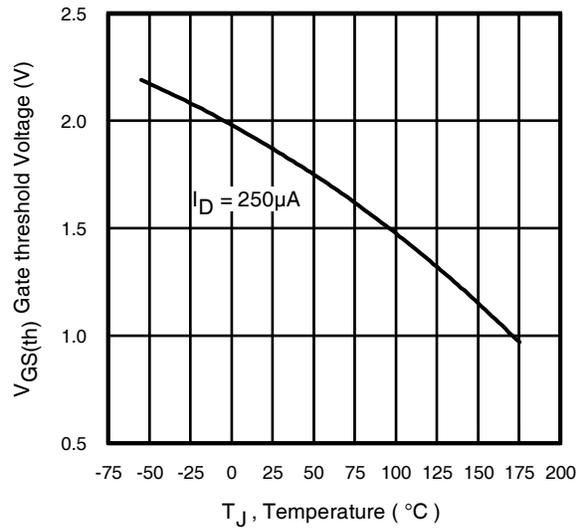
Fig 10. Threshold Voltage vs. Temperature

Ri (°C/W)	τi (sec)
1.163	0.000257
1.073	0.001040
0.419	0.003089

$C_i = \tau_i / R_i$

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc
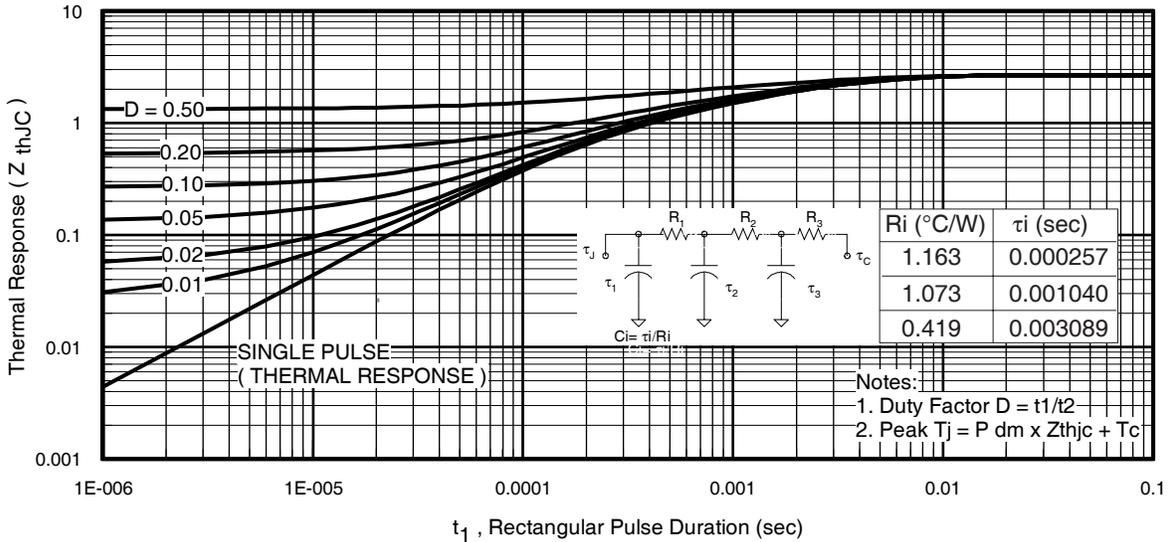
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

IRF3707ZCS/LPbF

Fig 12a. Unclamped Inductive Test Circuit
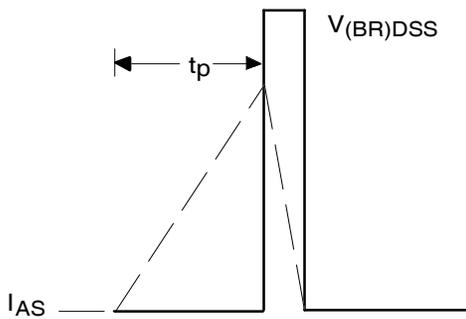
Fig 12b. Unclamped Inductive Waveforms

Starting T_J , Junction Temperature (°C)

Fig 12c. Maximum Avalanche Energy vs. Drain Current
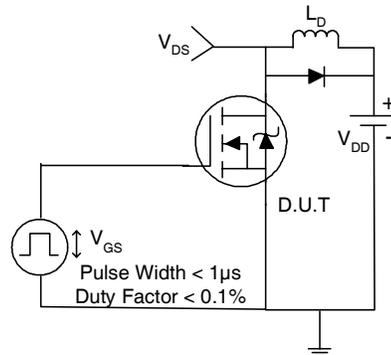
Fig 14a. Switching Time Test Circuit

Fig 13. Gate Charge Test Circuit
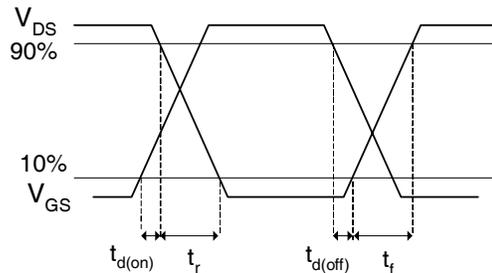
Fig 14b. Switching Time Waveforms

6

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

③

②

④

①

R_G

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

V_{DD}

① Driver Gate Drive

P.W.   Period $D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse Recovery Current

Body Diode Forward Current   di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery dv/dt

V_{DD}

Re-Applied Voltage

Body Diode   Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

Id

V_{ds}

V_{gs}

$V_{gs(th)}$

Qgs1 Qgs2   Qgd   Qgodr

Fig 16. Gate Charge Waveform

Power MOSFET Selection for Non-Isolated DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)} \right)$$
$$+ \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f \right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 16.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to I_{dmax} at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how Q_{oss} is formed by the parallel combination of the voltage dependant (nonlinear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^*$$
$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)} \right)$$
$$+ \left(Q_g \times V_g \times f \right)$$
$$+ \left(\frac{Q_{oss}}{2} \times V_{in} \times f \right) + \left(Q_{rr} \times V_{in} \times f \right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

$$C_{oss} = C_{dg} + C_{ds}$$
$$\Delta Q_{oss} = C_{oss} \times \Delta V_{in}$$
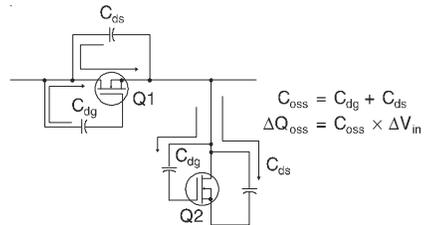
Figure A: Q_{oss} Characteristic

8

D²Pak Package Outline

Dimensions are shown in millimeters (inches)
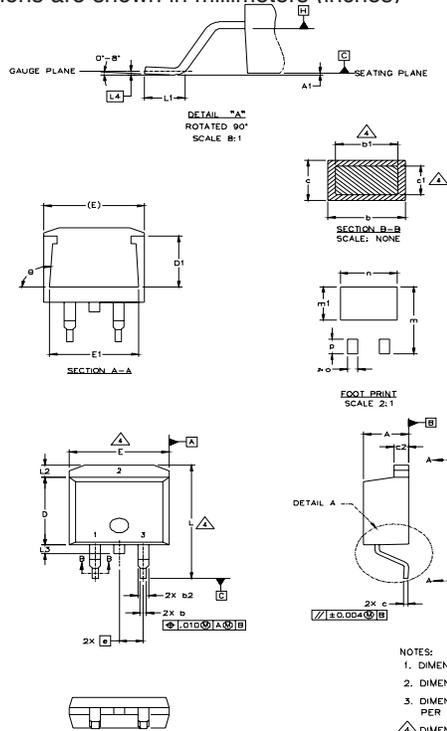
GAUGE PLANE
0°−8°
DETAIL "A"
ROTATED 90°
SCALE 8:1

SECTION B−B
SCALE: NONE

SEATING PLANE

SECTION A−A

FOOT PRINT
SCALE 2:1

DETAIL A

S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	4
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

| HEXFET	IGBTs, CoPACK	DIODES
1.− GATE	1.− GATE	1.− ANODE *
2.− DRAIN	2.− COLLECTOR	2.− CATHODE
3.− SOURCE	3.− EMITTER	3.− ANODE

* PART DEPENDENT.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE 'L'

Note: 'P' in assembly line
position indicates 'Lead-Free'
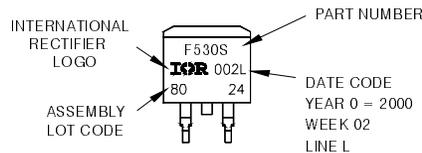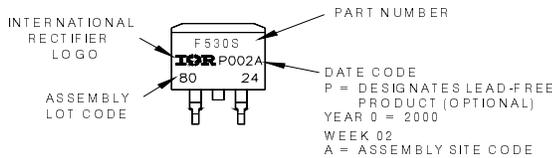
INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

ASSEMBLY
LOT CODE

F530S
IQR 002L
80   24

OR

INTERNATIONAL
RECTIFIER
LOGO

PART NUMBER

F530S
IQR P002A
80   24

ASSEMBLY
LOT CODE

DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

IRF3707ZCS/LPbF

TO-262 Package Outline
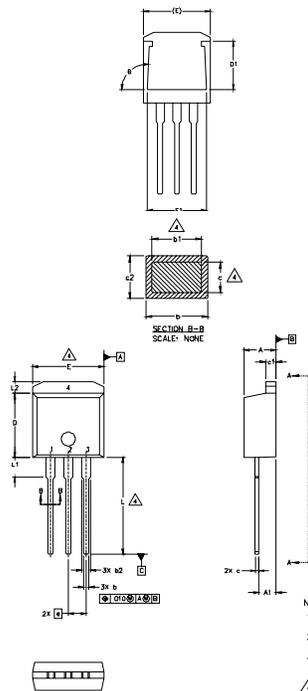
S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBT
1- GATE
2- COLLECTOR
3- EMITTER

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW19, 1997
IN THE ASSEMBLY LINE 'C'

Note: 'P' in assembly line position indicates 'Lead-Free'

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

ASSEMBLY LOT CODE

DATE CODE
P = DESIGNATES LEAD-FREE PRODUCT (OPTIONAL)
YEAR 7 = 1997
WEEK 19
A = ASSEMBLY SITE CODE

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/
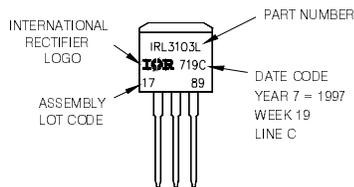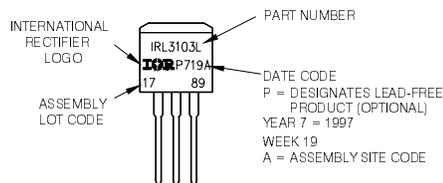
D²Pak Tape & Reel Infomation

Dimensions are shown in millimeters (inches)

TRR

FEED DIRECTION

TRL

FEED DIRECTION

1.60 (.063)
1.50 (.059)

4.10 (.161)
3.90 (.153)

Ø 1.60 (.063)
1.50 (.059)

1.85 (.073)
1.65 (.065)

11.60 (.457)
11.40 (.449)

0.368 (.0145)
0.342 (.0135)

15.42 (.609)
15.22 (.601)

24.30 (.957)
23.90 (.941)

10.90 (.429)
10.70 (.421)

Ø 1.75 (.069)
1.25 (.049)

4.72 (.136)
4.52 (.178)

16.10 (.634)
15.90 (.626)

13.50 (.532)
Ø 12.80 (.504)

Ø 330.00
(14.173)
MAX.

27.40 (1.079)
23.90 (.941)

4

Ø 60.00 (2.362)
MIN.

30.40 (1.197)
MAX.
4

26.40 (1.039)
24.40 (.961)

3

NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
C DIMENSION MEASURED @ HUB.
D INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.15mH, R_G = 25Ω, I_{AS} = 23A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑤ This is applied to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 42A.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IΩR Rectifier