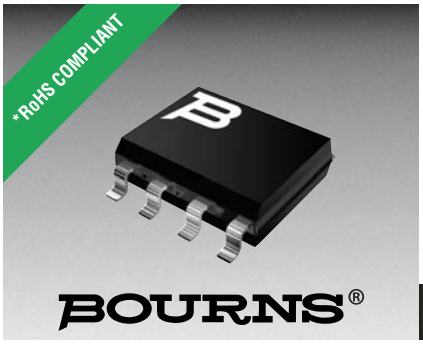


DUAL FORWARD-CONDUCTING UNIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTOR

The Model TISP1120F3D is currently available, but not recommended for new designs.

TISP1120F3D Overvoltage Protector

Ion-Implanted Breakdown Region
- Precise and Stable Voltage

Planar Passivated Junctions
- Low Off-State Current <10 μA

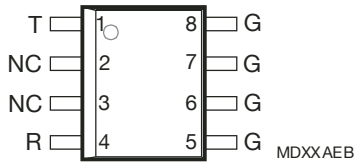
Low Voltage Overshoot Under Surge

Device Name	V_{DRM} V	$V_{(BO)}$ V
TISP1120F3D	-97	-120

Rated for International Surge Wave Shapes

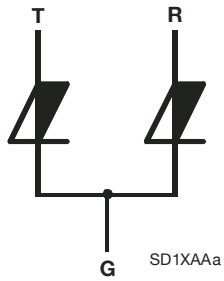
Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	120
8/20	IEC 61000-4-5	70
10/160	TIA-968-A	60
10/700	ITU-T K.20/21/45	50
10/560	TIA-968-A	45
10/1000	GR-1089-CORE	35

8-SOIC Package (Top View)



NC - No internal connection

Device Symbol



Description

This dual forward-conducting unidirectional overvoltage protector is designed for the overvoltage protection of ICs used for the SLIC (Subscriber Line Interface Circuit) function. The IC line driver section is typically powered with 0 V and a negative supply. The TISP1120F3D limits voltages that exceed these supply rails.

High voltages can occur on the line as a result of exposure to lightning strikes and a.c. power surges. Negative transients are initially limited by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar. The high crowbar holding current helps prevent d.c. latchup as the current subsides. Positive transients are limited by diode forward conduction. These protectors are designed to suppress and withstand the listed international lightning surges on any terminal pair.

This monolithic protection device is fabricated in an ion-implanted planar structure to ensure precise and matched breakover control, and is virtually transparent to the system in normal operation.

How to Order

Device	Package	Carrier	Order As	Marking Code	Standard Quantity
TISP1120F3D	8-SOIC	Embossed Tape Reeled	TISP1120F3DR-S	1120F3	2500

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
JULY 2005 – REVISED KLSBJ?BO /-.4
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage	V_{DRM}	-97	V
Non-repetitive peak impulse current (see Note 1) 2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape) 8/20 µs (IEC 61000-4-5, combination wave generator, 1.2/50 µs voltage waveshape) 10/160 µs (TIA-968-A, 10/160 µs voltage wave shape) 5/310 µs (ITU-T K.44, 10/700 µs voltage wave shape used in K.20/21/45) 5/320 µs (TIA-968-A, 9/720 µs voltage waveshape) 10/560 µs (TIA-968-A, 10/560 µs voltage wave shape) 10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)	I_{PPSM}	 2 x ±120 2 x ±70 2 x ±60 2 x ±50 2 x ±50 2 x ±45 2 x ±35	A
Non-repetitive peak on-state current, 0 °C < T_A < 70 °C 1 s, 50 Hz	I_{TSM}	 2 x 4.3	A
Initial rate of rise of on-state current, linear current ramp, maximum ramp value < 38 A	di_T/dt	250	A/µs
Junction temperature	T_J	-65 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTE: 1. Initially the device must be in thermal equilibrium with 0 °C < T_J < 70 °C. The surge may be repeated after the device returns to its initial conditions.

Electrical Characteristics for Terminals T and R, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	V_D = ±V_{DRM}	T_A = 25 °C			±5	µA
			T_A = 70 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = -250 V/ms, R_{SOURCE} = 300 Ω				±123	V
I_H	Holding current	I_T = ±5 A, di/dt = ±30 mA/ms		±150			mA

Electrical Characteristics for Terminals T and G or R and G, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	V_D = V_{DRM}	T_A = 25 °C			-5	µA
			T_A = 70 °C			-10	
$V_{(BO)}$	Breakover voltage	dv/dt = -250 V/ms, R_{SOURCE} = 300 Ω				-120	V
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ -1000 V/µs, Linear voltage ramp, Maximum ramp value = -500 V di/dt ≤ -20 A/µs, Linear current ramp, Maximum ramp value = -10 A				-130	V
$I_{(BO)}$	Breakover current	dv/dt = -250 V/ms, R_{SOURCE} = 300 Ω		-100		-600	mA
I_H	Holding current	I_T = -5 A, di/dt = +30 mA/ms		-150			mA
V_T	On-state voltage	I_T = -5 A, t_w = 100 µs				-3	V
V_F	Forward voltage	I_F = +5 A, t_w = 100 µs				+3	V
V_{FRM}	Peak forward recovery voltage	dv/dt ≤ +1000 V/µs, Linear voltage ramp, Maximum ramp value = +500 V di/dt ≤ +20 A/µs, Linear current ramp, Maximum ramp value = +10 A			+3.3		V
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, maximum ramp value < 0.85V_{DRM}		-5			kV/µs
C_O	Off-state capacitance	f = 1 MHz, V_d = 1 V rms	V_D = -2 V		60	65	pF
			V_D = -50 V		20	25	

Thermal Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	P_{tot} = 0.8 W 5 cm^2 FR4 PCB			160	°C/W

Parameter Measurement Information

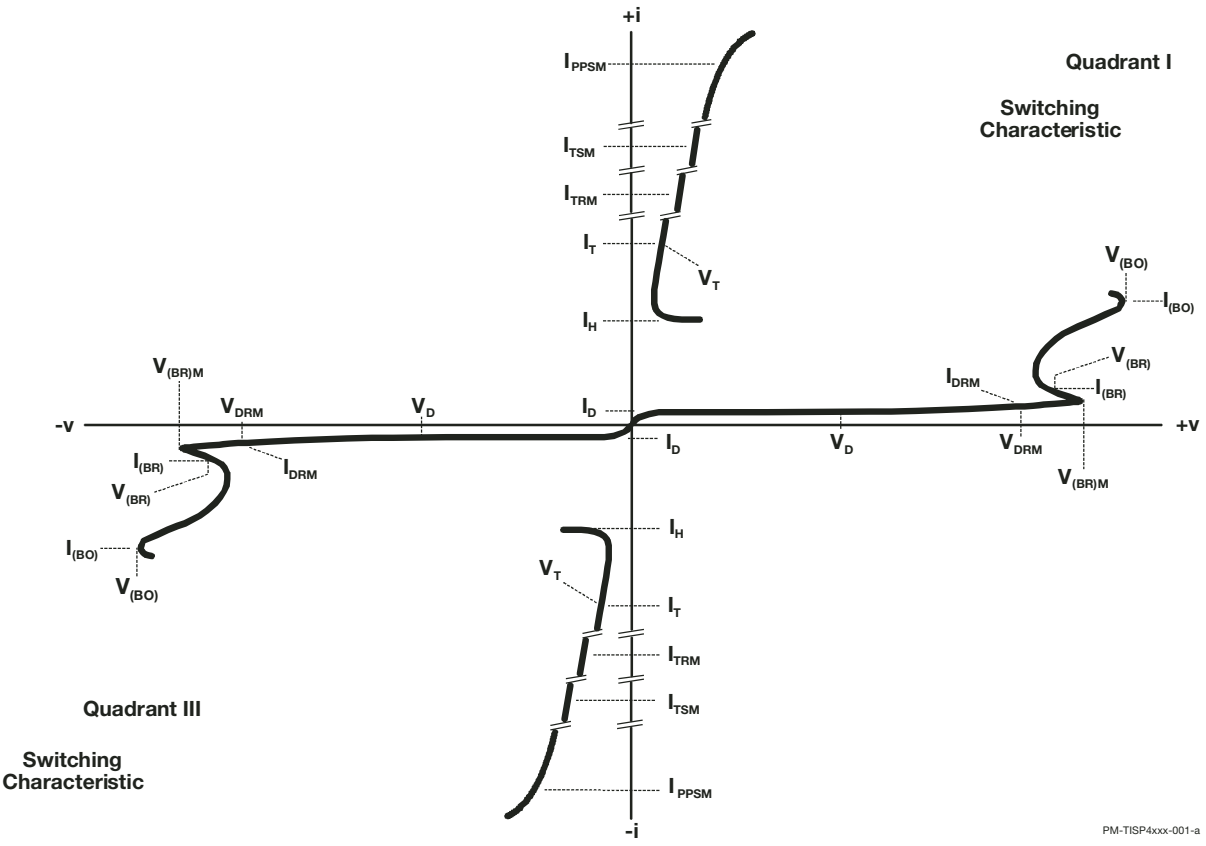


Figure 1. Voltage-Current Characteristic for the Terminals T and R
All Measurements are Referenced to Terminal R

Parameter Measurement Information (Continued)

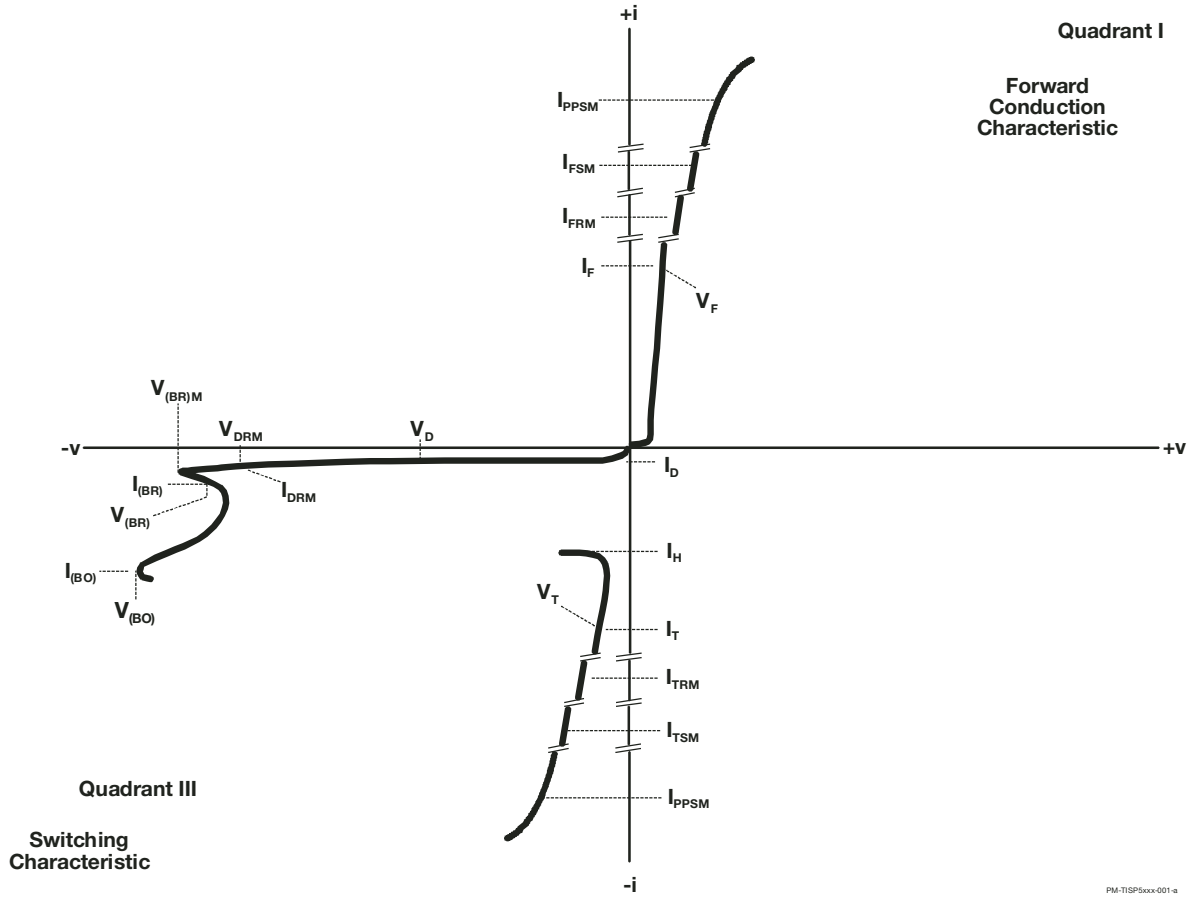


Figure 2. Voltage-Current Characteristic for Terminals T and G or R and G
All Measurements are Referenced to Terminal G

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