R2A20162NS/SA/SP

8-bit 2ch D/A Converter with Buffer

R03DS0016EJ0100
Rev.1.00
2011.09.05

Description

The R2A20162 is an integrated circuit semiconductor of CMOS structure with 2 channels of built in D/A converters with output buffer op-amps. It is the electrical characteristic improvement version of the M62342.

Serial data transfer type input can easily be used through a combination of three lines: DI, CLK, and LD.

Outputs incorporate buffer op-amps that have a drive capacity of 1 mA or above for both sink source, and can operate over the entire voltage range from almost ground to Vcc (0 to 5V), making peripheral elements unnecessary and enabling configuration of a system with few component parts.

Very small SON package is added to lineup. It is suitable for a small mounting and reduces the mounting area.

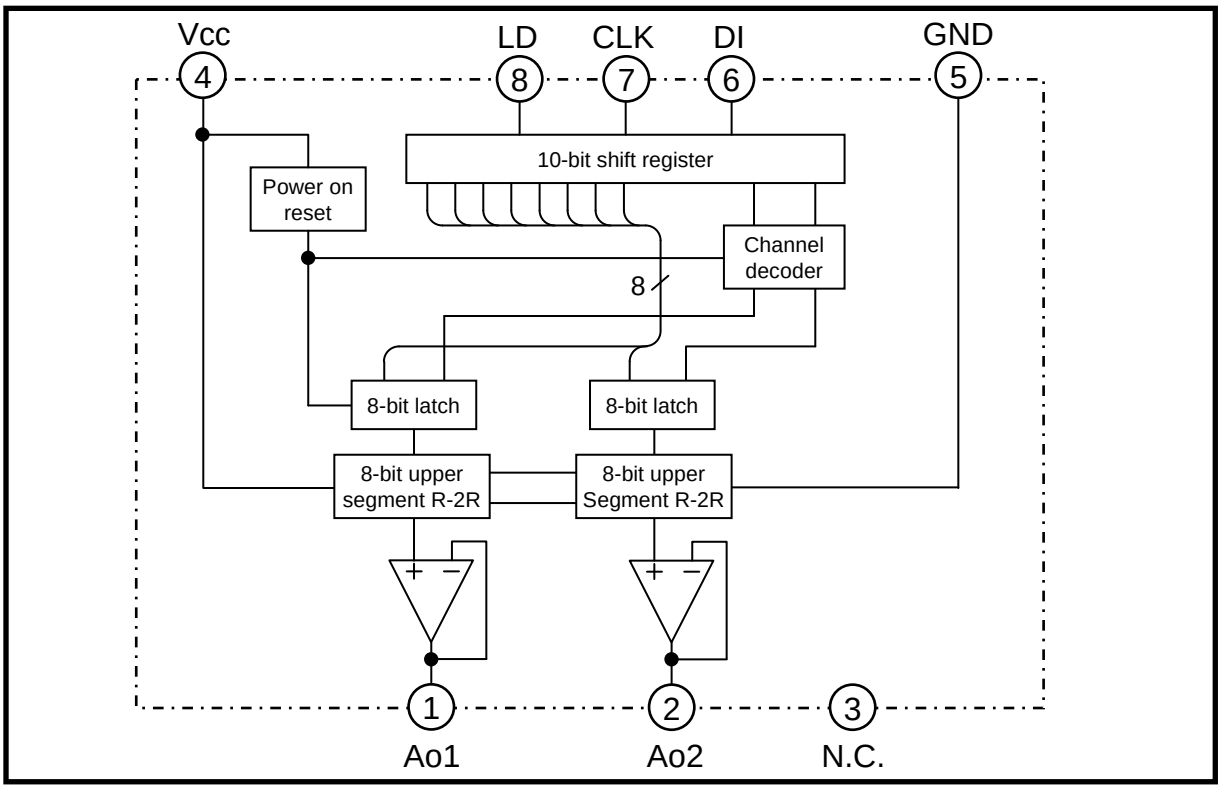
Features

- Guarantee Differential Nonlinearity error : +/- 0.7LSB, Nonlinearity error : +/- 1.0LSB,
- Data transfer format: 10-bit serial data input type by 3 wire (DI, SCK, LD)
- Output buffer op-amps: Operable over entire voltage range from almost ground to Vcc (0 to 5V)
- High output current capacity: +/- 1mA or Higher
- Very mall size package line-up: SON-8 (pin pitch: 0.5mm), TSSOP-8 (pin pitch 0.65mm)

Application

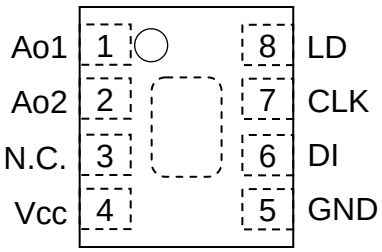
- Conversion from digital data to analog control data for home-use and industrial equipment.
- Signal gain control or automatic adjustment of LCD-TV, PDP-TV or LCD display-monitor.
- Blurring correction control or various control of the interchangeable lens of digital camera for self adjustment by combination with microcomputer and EEPROM. (substitution of half fixed resistance)

Block Diagram



Pin Arrangement

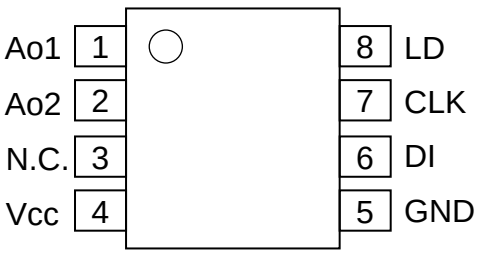
R2A20162NS (Top view)



N.C.: Not connected

Outline: PWSN0008KA-A [NS]

R2A20162SA/SP (Top view)



N.C.: Not connected

Outline: PRSP0008DE-C [SP]
PTSP-0008JC-B [SA]

Pin Description

Pin No.	Pin Name	Function
6	DI	Serial data input terminal. (Input serial data with a 10-bit data length.)
7	CLK	Serial clock input terminal (Input signal from DI terminal is input to 10-bit shift register at rise of serial clock.)
8	LD	Load terminal (When High level is input to LD terminal, value in 10-bit shift register is loaded into decoder and 8-bit latch.)
1	Ao1	8-bit resolution D/A converter output terminals (After power-on, all channels are reset and DAC data 00h is output.)
2	A02	
3	N.C.	Not connected
4	Vcc	Power supply terminal
5	GND	GND terminal

Absolute Maximum Ratings

(Ta= +25deg unless otherwise noted)

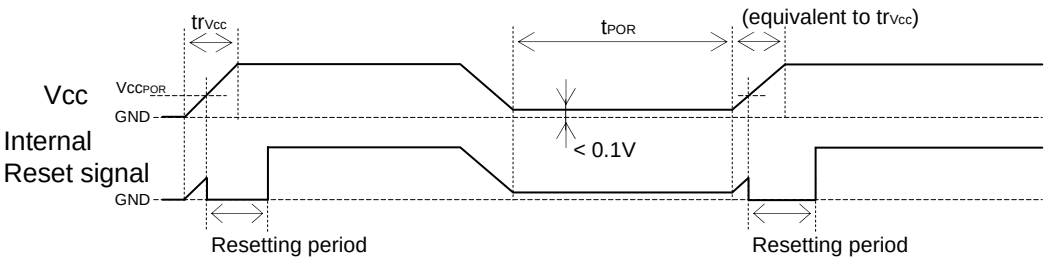
Item	Symbol	Conditions	Ratings	Unit
Supply voltage	Vcc		-0.3 to +6.5	V
Input voltage	Vin		-0.3 to Vcc+0.3 <6.5	V
Output voltage	Vo		-0.3 to Vcc+0.3 <6.5	V
Buffer amplifier output current	I_{AO}	Continuous	-2.0 to +2.0	mA
Power dissipation	Pd	Ta=85deg	270(NS) / 200(SA) / 272(SP)	mW
Thermal derating factor	K theta	Ta>25deg	6.75(NS) / 5.0(SA) / 6.8(SP)	mW/deg
Operating temperature	Topr		-30 to +85	deg
Storage temperature	Tstg		-40 to +125	deg

Electrical Characteristics

(Vcc= +5V +/-10%, GND=0V, Ta= -30 to +85deg unless otherwise noted)

Item	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Supply voltage	Vcc		2.7	5.0	5.5	V
Supply current	Icc	CLK = 1MHz operation, I_{AO}=0µA, DATA: 6Ah (at maximum current)	0	0.7	2.5	mA
		SDA = SCL = GND, I_{AO}=0µA	0	0.5	1.6	mA
Supply voltage rise-up time *1	tr_{Vcc}	Vcc=0 to 2.7V	100	—	—	µs
Operating voltage of Internal resetting *1	Vcc_{POR}	Vcc=0 to 2.7V	—	1.5	1.9	V
Time period of re-power on (Power supply OFF → ON) *1	t_{POR}	Vcc < 0.1V	1	—	—	ms
Input leak current	I_{ILK}	VIN= 0 to Vcc	-10	—	10	µA
Input low voltage	V_{IL}		0	—	0.2Vcc	V
Input high voltage	V_{IH}	4.0V < Vcc	0.5Vcc	—	Vcc	V
		Vcc < 4.0V	0.8Vcc	—	Vcc	V
Buffer amplifier output voltage range	V_{AO}	I_{AO}= +/-100µA	0.1	—	Vcc-0.1	V
		I_{AO}= +/-500µA	0.2	—	Vcc-0.2	
Buffer amplifier output drive range	I_{AO}	Upper side saturation voltage = 0.3V Lower side saturation voltage = 0.2V	-1.0	—	1.0	mA
Differential nonlinearity	S_{DL}	Vcc=5.12V (20mV/ LSB), without load (I_{AO}= 0µA)	-0.7	—	0.7	LSB
Nonlinearity	S_L		-1.0	—	1.0	LSB
Zero code error	S_{ZERO}		-2.0	—	2.0	LSB
Full scale error	S_{FULL}		-2.0	—	2.0	LSB
Output capacitate load	Co		—	—	0.1	µF
Buffer amplifier output impedance	Ro		—	5.0	—	ohm

*1 : When power supply is turned on, internal circuit is initialized by power on reset circuit. But, if re-powered on quickly, initialize is not operate. So, keep the time period of re-powered on (t_{POR}).

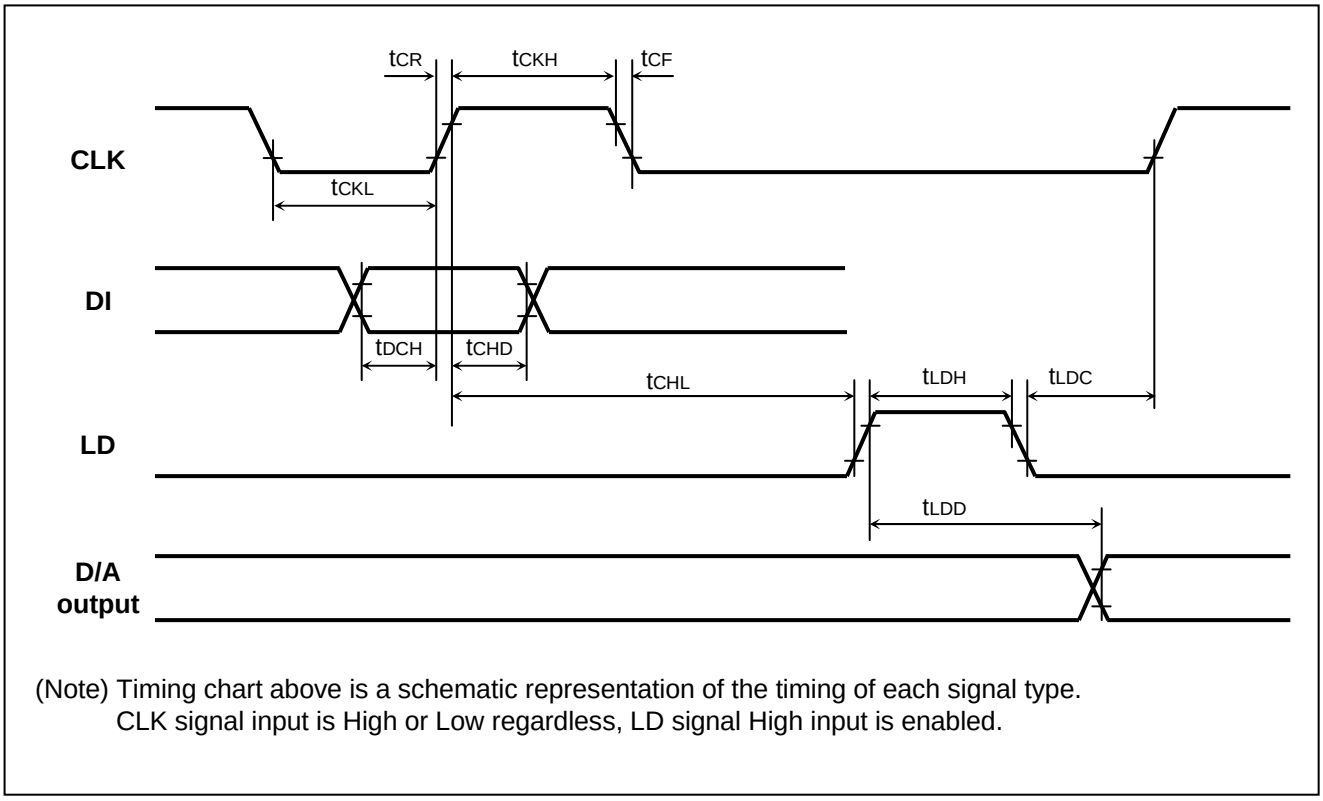


AC Characteristics

(Vcc = +5V +/-10deg, GND = 0V, Ta = -30 to +85deg unless otherwise noted)

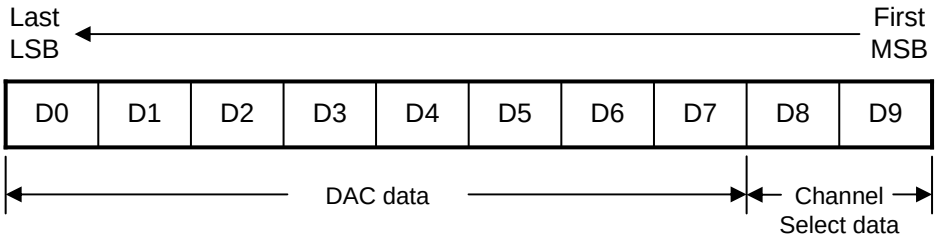
Item	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Clock frequency	f_{CLK}		-	1.0	10	MHz
Clock high pulse width	t_{CKH}		40	-	-	ns
Clock low pulse width	t_{CKL}		40	-	-	ns
Clock rise time	t_{CR}		-	-	200	ns
Clock fall time	t_{CF}		-	-	200	ns
Data setup time	t_{DCH}		5	-	-	ns
Data hold time	t_{CHD}		30	-	-	ns
Load setup time	t_{CHL}		40	-	-	ns
Load hold time	t_{LDC}		40	-	-	ns
Load high pulse width	t_{LDH}		40	-	-	ns
D/A output settling time	t_{LDD}	Ta=25deg, C_L<100pF, V_{AO}: 0.5←→4.5V, The time until the output becomes the final value of 1/2 LSB.	-	-	150	µs

Timing Chart



(Note) Timing chart above is a schematic representation of the timing of each signal type.
CLK signal input is High or Low regardless, LD signal High input is enabled.

Digital Data Format



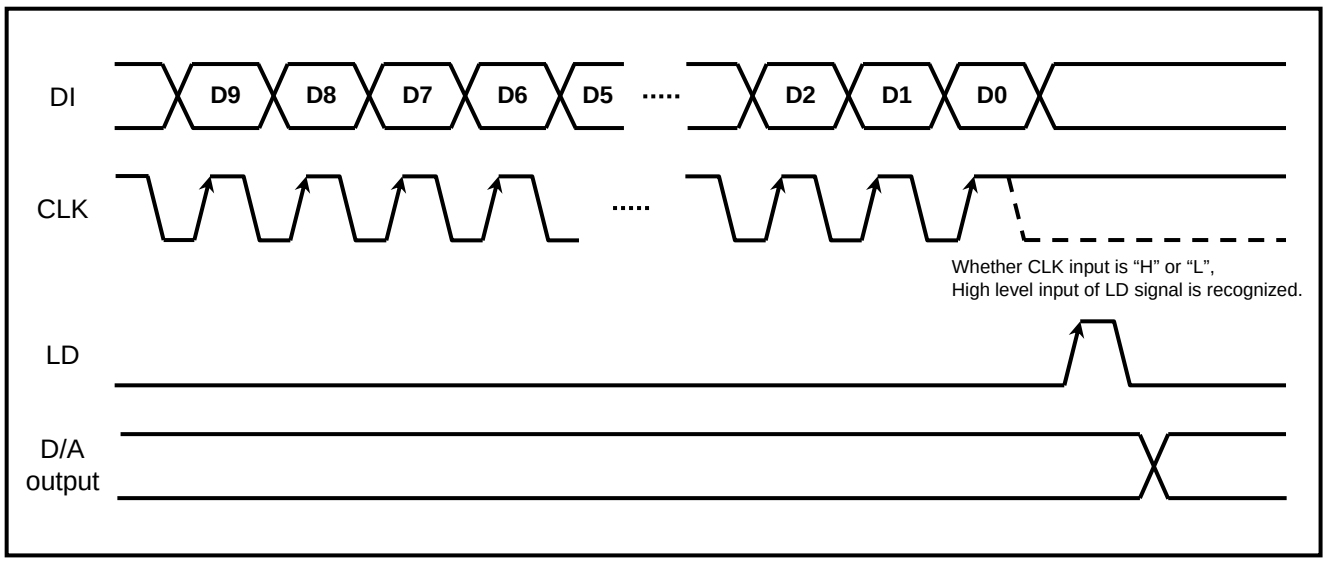
Channel select data

D8	D9	Channel selection
0	0	Ao1 selected
1	0	Ao2 selected
0	1	Don't care
1	1	Don't care

DAC data

D0	D1	D2	D3	D4	D5	D6	D7	DAC output
0	0	0	0	0	0	0	0	Vcc/256 x 1
1	0	0	0	0	0	0	0	Vcc/256 x 2
0	1	0	0	0	0	0	0	Vcc/256 x 3
1	1	0	0	0	0	0	0	Vcc/256 x 4
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	Vcc/256 x 255
1	1	1	1	1	1	1	1	Vcc

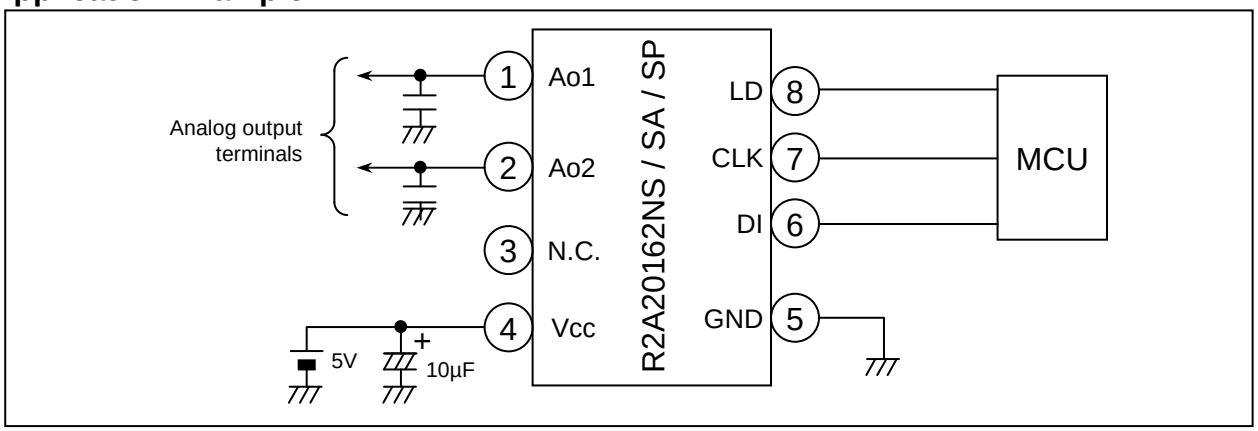
Data timing chart (Model)



Precaution For use

- Supply voltage terminal (Vcc) is also used for D/A converter upper reference voltage setting. If ripple or spike is input this terminal, accuracy of D/A converter is down, So, when use this device, please connect capacitor among Vcc to GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load, So, it's no problem at device action when connect capacitor (0.1 µF Max) among output to GND for every noise elimination.

Application Example



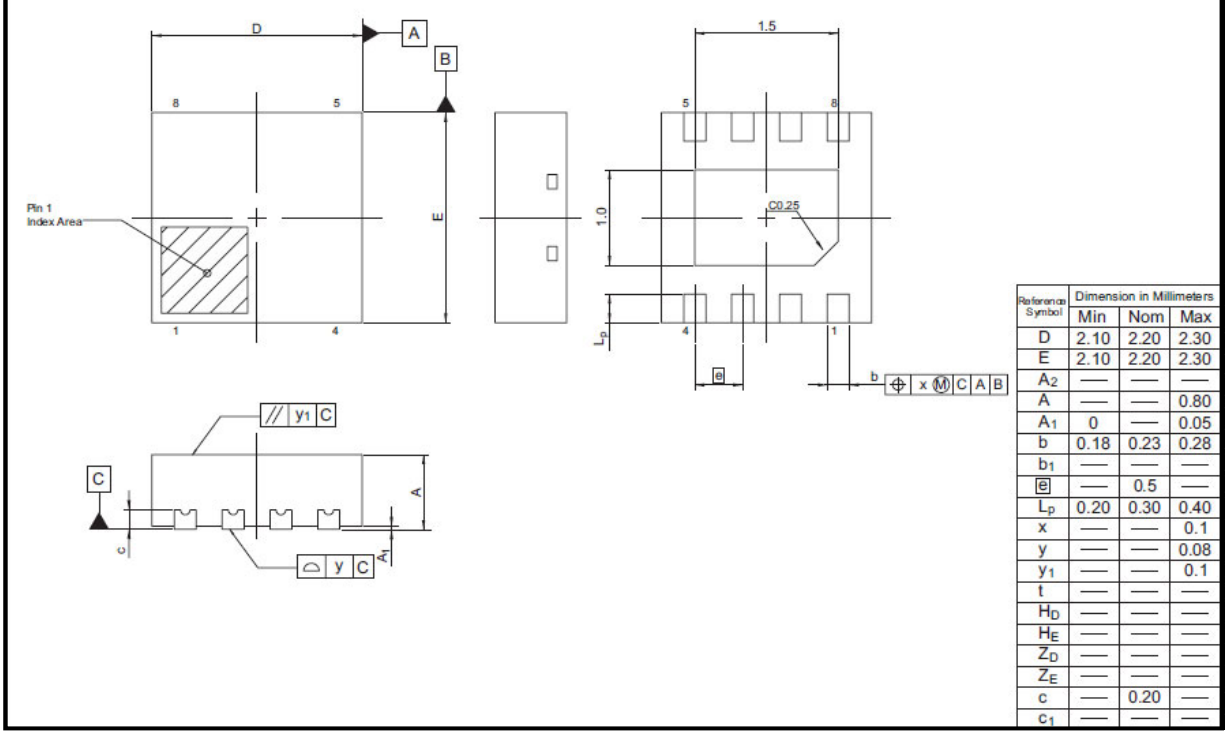
Ordering Information

Order part No.	Package Name	Package Code	Package type No.	Packing/Quantity
R2A20162SP	SOP-8	PRSP0008DE-C	SP	Embossed Taping/2,500 pcs.
R2A20162SA	TSSOP-8	RTSP0008JC-B	SA	Embossed Taping/3,000 pcs.
R2A20162NS	SON-8	PWSN0008KA-A	NS	Embossed Taping/5,000 pcs.

Package Dimensions

PWSN0008KA-A [NS]

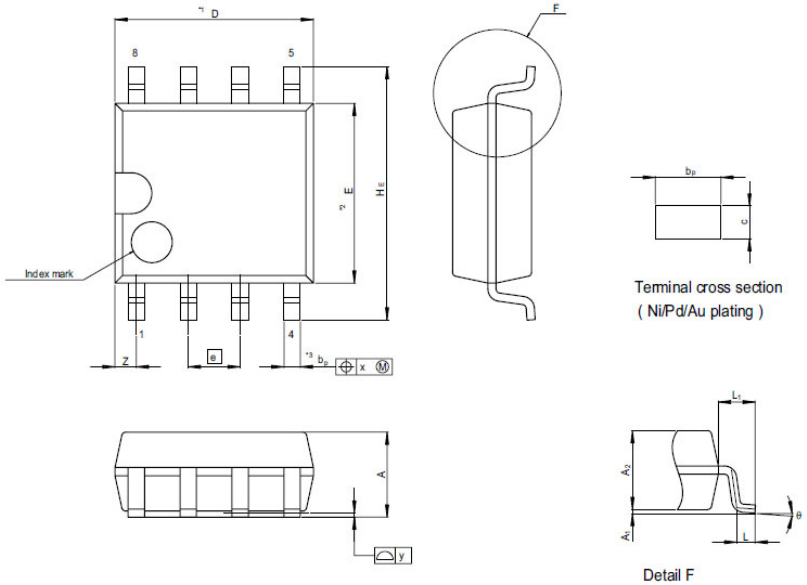
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWSON8-2.2x2.2-0.50	PWSN0008KA-A	—	0.011g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	2.10	2.20	2.30
E	2.10	2.20	2.30
A_2	—	—	—
A	—	—	0.80
A_1	0	—	0.05
b	0.18	0.23	0.28
b_1	—	—	—
e	—	0.5	—
L_p	0.20	0.30	0.40
x	—	—	0.1
y	—	—	0.08
y_1	—	—	0.1
t	—	—	—
H_D	—	—	—
H_E	—	—	—
Z_D	—	—	—
Z_E	—	—	—
c	—	0.20	—
c_1	—	—	—

PRSP0008DE-C [SP]

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g

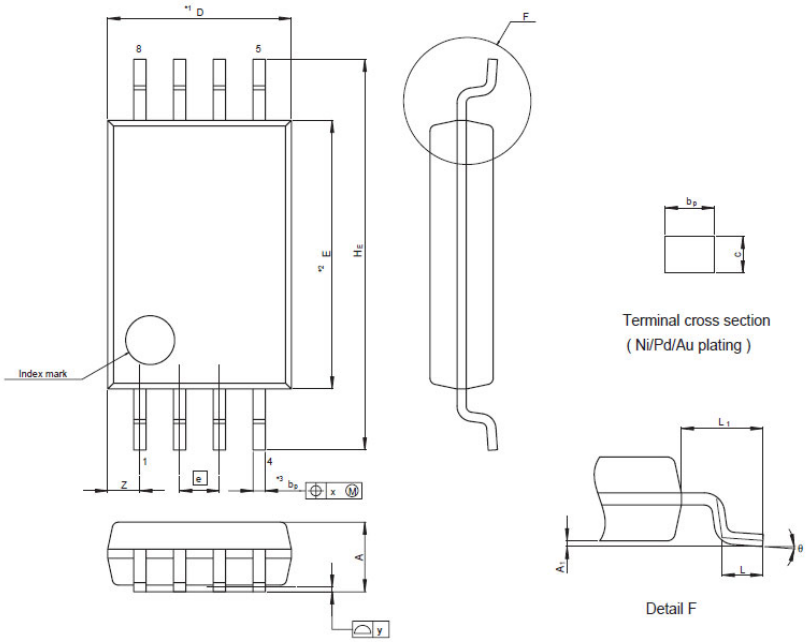


NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A_2	—	1.85	—
A_1	0.00	0.1	0.20
A	—	—	2.03
b_p	0.34	0.4	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	5.7	6.2	6.5
e	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L_1	—	0.90	—

PTSP0008JC-B [SA]

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP8-4.4x3-0.65	PTSP0008JC-B	TTP-8DAV	0.034g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	3.00	3.30
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.805
L	0.40	0.50	0.60
L_1	—	1.00	—

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