MC14022B

Octal Counter

The MC14022B is a four−stage Johnson octal counter with built−in code converter. High−speed operation and spike−free outputs are obtained by use of a Johnson octal counter design. The eight decoded outputs are normally low, and go high only at their appropriate octal time period. The output changes occur on the positive−going edge of the clock pulse. This part can be used in frequency division applications as well as octal counter or octal decode display applications.

ON Semiconductor®

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SOIC−16
D SUFFIX
CASE 751B

Features

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Pin−for−Pin Replacement for CD4022B
- Triple Diode Protection on All Inputs
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

PIN ASSIGNMENT

Q1	1●		16	V_{DD}
Q0	2		15	R
Q2	3		14	C
Q5	4		13	$\overline{CE}$
Q6	5		12	C_{out}
NC	6		11	Q4
Q3	7		10	Q7
V_{SS}	8		9	NC

NC = NO CONNECTION

MARKING DIAGRAM

16
14022BG
○ AWLYWW
1

A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Indicator

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MC14022B

BLOCK DIAGRAM

CLOCK	14		Q0	2	
			Q1	1	
			Q2	3	
$\overline{\text{CLOCK}}$ $\overline{\text{ENABLE}}$	13		Q3	7	
			Q4	11	
			Q5	4	
			Q6	5	
RESET	15		Q7	10	
			C_{out}	12	

V_{DD} = PIN 16
V_{SS} = PIN 8
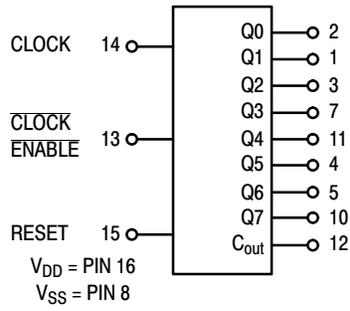
NC = PIN 6, 9

FUNCTIONAL TRUTH TABLE
(Positive Logic)

Clock	$\overline{\text{Clock}}$ $\overline{\text{Enable}}$	Reset	Output=n
0	X	0	n
X	1	0	n
⌐	0	0	n+1
⌐	X	0	n
1	⌐	0	n+1
X	⌐	0	n
X	X	1	Q0

X = Don't Care. If n < 4 Carry = 1,
Otherwise = 0.

LOGIC DIAGRAM
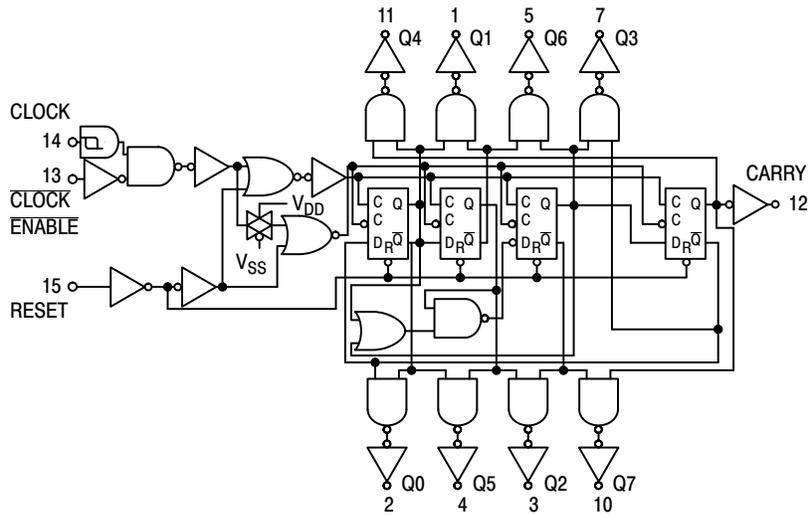
MC14022B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V$_{SS}$)

Characteristic		Symbol	V$_{DD}$ Vdc	−55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage "0" Level V$_{in}$ = V$_{DD}$ or 0		V$_{OL}$	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
"1" Level V$_{in}$ = 0 or V$_{DD}$		V$_{OH}$	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage "0" Level (V$_O$ = 4.5 or 0.5 Vdc) (V$_O$ = 9.0 or 1.0 Vdc) (V$_O$ = 13.5 or 1.5 Vdc)		V$_{IL}$	5.0 10 15	− − −	1.5 3.0 4.0	− − −	2.25 4.50 6.75	1.5 3.0 4.0	− − −	1.5 3.0 4.0	Vdc
"1" Level (V$_O$ = 0.5 or 4.5 Vdc) (V$_O$ = 1.0 or 9.0 Vdc) (V$_O$ = 1.5 or 13.5 Vdc)		V$_{IH}$	5.0 10 15	3.5 7.0 11	− − −	3.5 7.0 11	2.75 5.50 8.25	− − −	3.5 7.0 11	− − −	Vdc
Output Drive Current (V$_{OH}$ = 2.5 Vdc) (V$_{OH}$ = 4.6 Vdc) (V$_{OH}$ = 9.5 Vdc) (V$_{OH}$ = 13.5 Vdc)	Source	I$_{OH}$	5.0 5.0 10 15	−3.0 −0.64 −1.6 −4.2	− − − −	−2.4 −0.51 −1.3 −3.4	−4.2 −0.88 −2.25 −8.8	− − − −	−1.7 −0.36 −0.9 −2.4	− − − −	mAdc
(V$_{OL}$ = 0.4 Vdc) (V$_{OL}$ = 0.5 Vdc) (V$_{OL}$ = 1.5 Vdc)	Sink	I$_{OL}$	5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current		I$_{in}$	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance (V$_{in}$ = 0)		C$_{in}$	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)		I$_{DD}$	5.0 10 15	− − −	5.0 10 20	− − −	0.005 0.010 0.015	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C$_L$ = 50 pF on all outputs, all buffers switching)		I$_T$	5.0 10 15	I$_T$ = (0.28 μA/kHz)f + I$_{DD}$ I$_T$ = (0.56 μA/kHz)f + I$_{DD}$ I$_T$ = (0.85 μA/kHz)f + I$_{DD}$							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L − 50) \text{ Vfk}$$

where: I$_T$ is in μA (per package), C$_L$ in pF, V = (V$_{DD}$ − V$_{SS}$) in volts, f in kHz is input frequency, and k = 0.00125.

MC14022B

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Propagation Delay Time Reset to Decode Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 – – –	 500 230 175	 1000 460 350	ns
Propagation Delay Time Clock to C_{out} t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 315 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 142 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 100 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 – – –	 400 175 125	 800 350 250	ns
Propagation Delay Time Clock to Decode Output t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 197 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 150 ns	t_{PLH}, t_{PHL}	 5.0 10 15	 – – –	 275 125 95	 1000 460 350	ns
Turn–Off Delay Time Reset to C_{out} t_{PLH} = (1.7 ns/pF) C_L + 315 ns t_{PLH} = (0.66 ns/pF) C_L + 142 ns t_{PLH} = (0.5 ns/pF) C_L + 100 ns	t_{PLH}	 5.0 10 15	 – – –	 400 175 125	 800 350 250	ns
Clock Pulse Width	t_{WH}	5.0 10 15	250 100 75	125 50 35	– – –	ns
Clock Frequency	f_{cl}	5.0 10 15	– – –	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	t_{WH}	5.0 10 15	500 250 190	250 125 95	– – –	ns
Reset Removal Time	t_{rem}	5.0 10 15	750 275 210	375 135 105	– – –	ns
Clock Input Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	No Limit			–
Clock Enable Setup Time	t_{su}	5.0 10 15	350 150 115	175 75 52	– – –	ns
Clock Enable Removal Time	t_{rem}	5.0 10 15	420 200 140	260 100 70	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14022B

	Output Sink Drive	Output Source Drive
Outputs	**(S1 to A)**	**Clock to desired Output (S1 to B)**
Carry	Clock to Q5 thru Q7 (S1 to B)	S1 to A
$V_{GS} =$	V_{DD}	$- V_{DD}$
$V_{DS} =$	V_{out}	$V_{out} - V_{DD}$
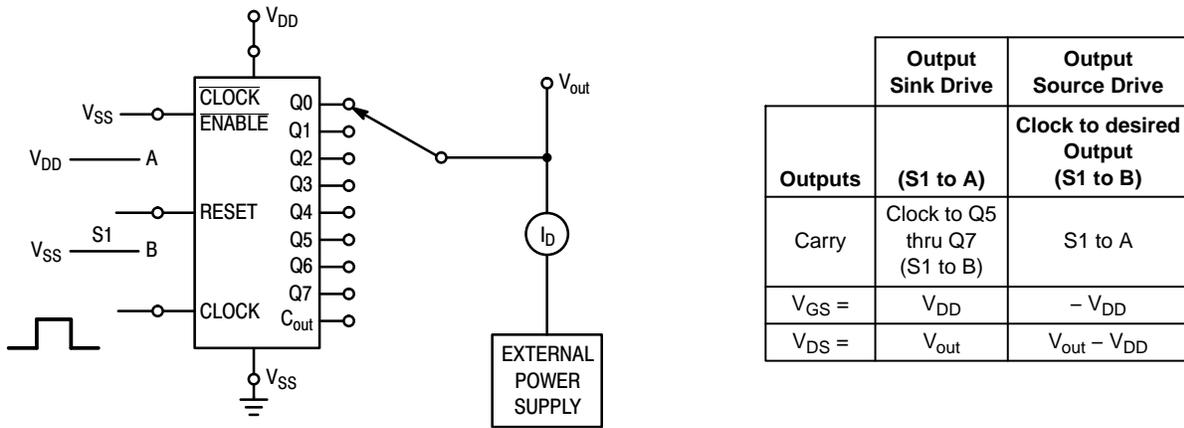
Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit
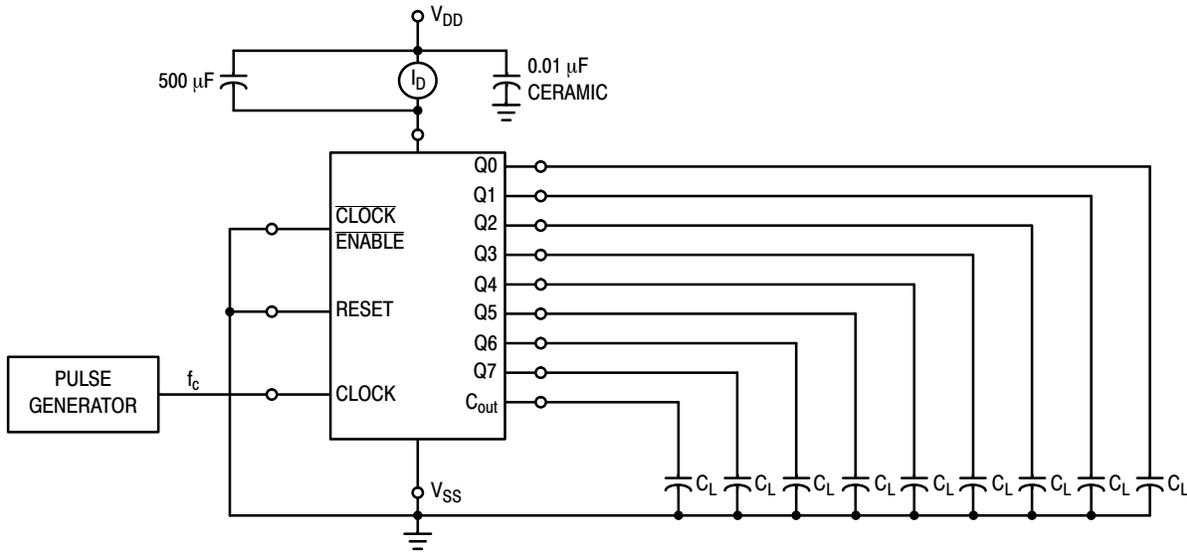
Figure 2. Typical Power Dissipation Test Circuit

APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14022B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).
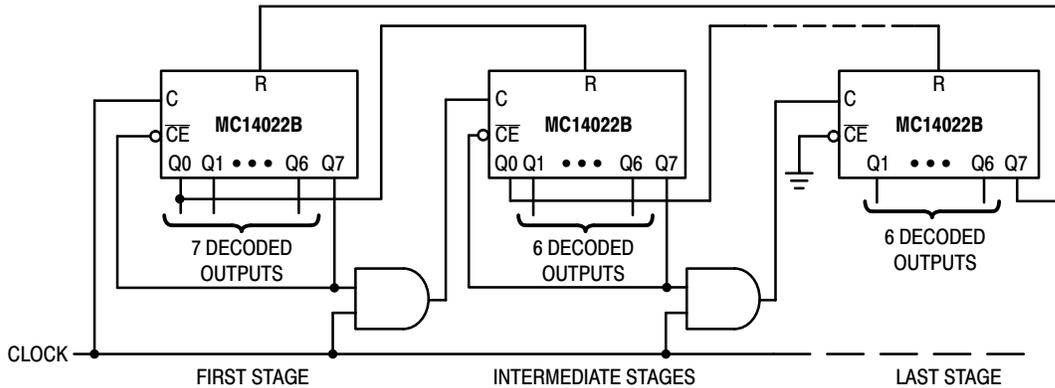
Figure 3. Counter Expansion

MC14022B
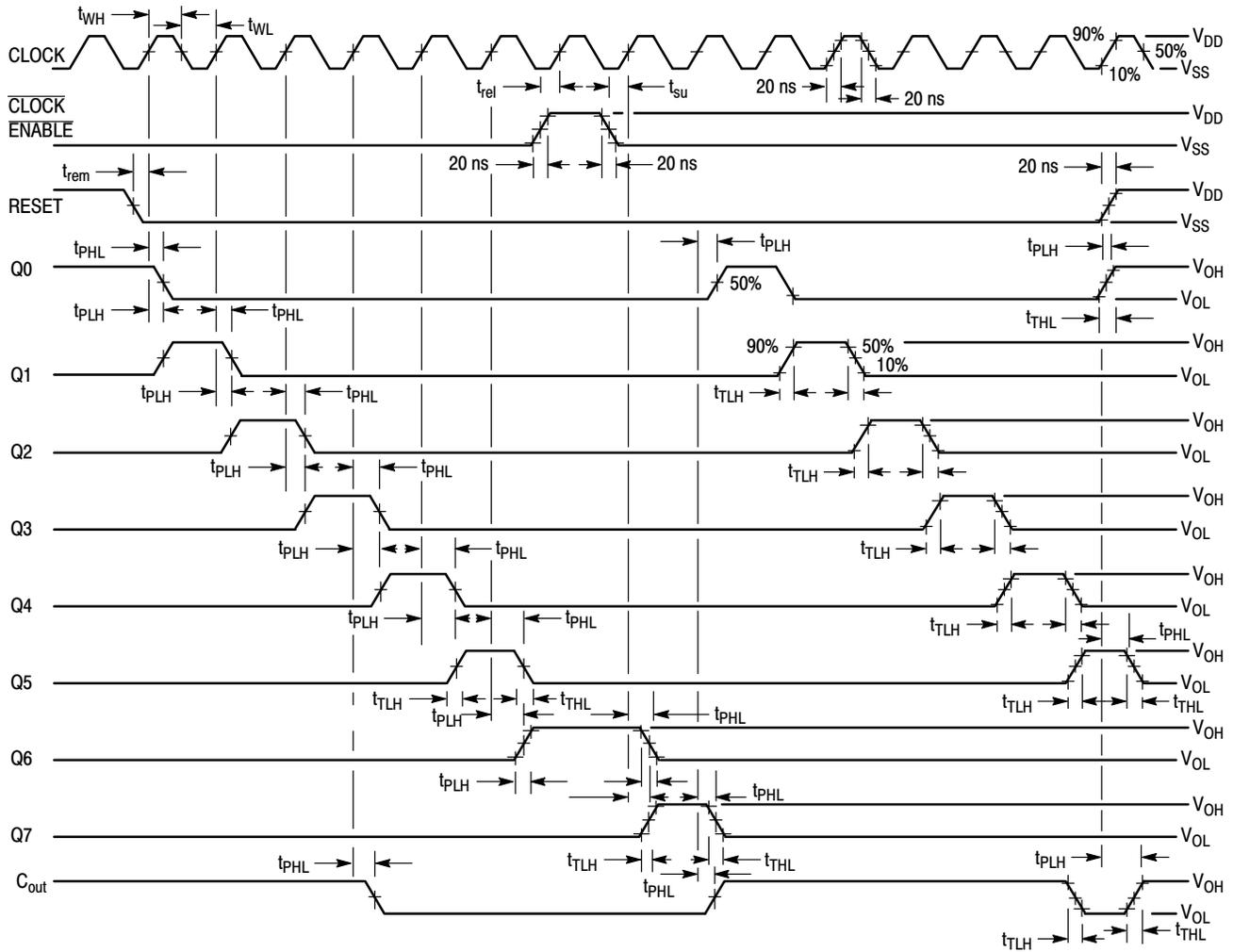
Figure 4. AC Measurement Definition and Functional Waveforms

ORDERING INFORMATION

Device	Package	Shipping†
MC14022BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14022BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14022BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

SOIC–16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE K
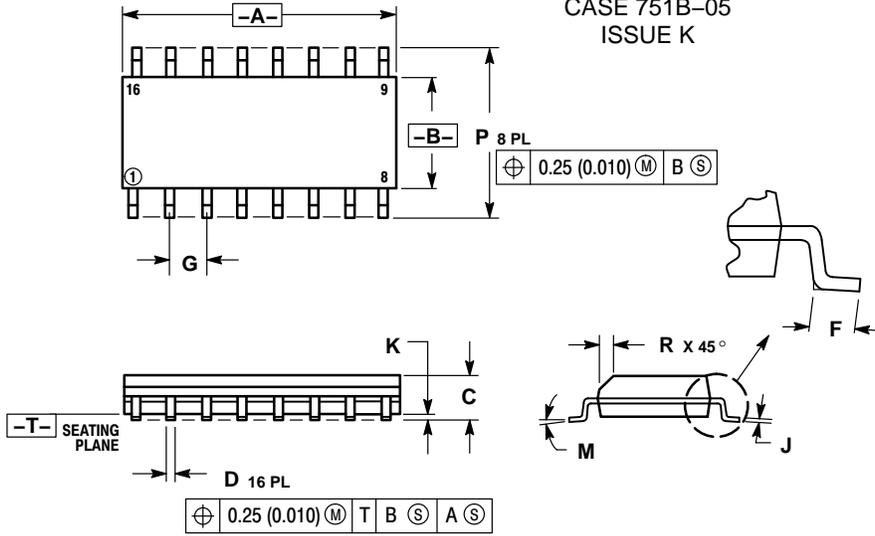
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS
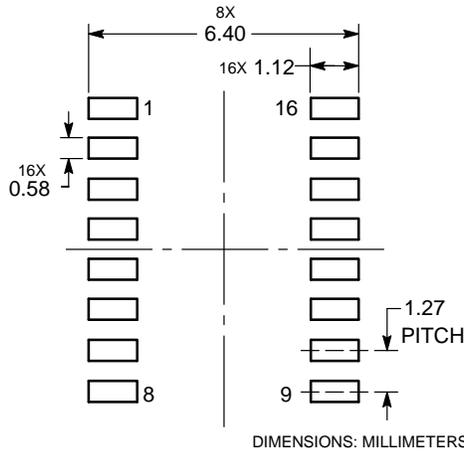
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.