Si53305

1:10 Low Jitter Universal Buffer/Level Translator with 2:1 Input Mux and Individual OE

Features

- 10 differential or 20 LVCMOS outputs
- Ultra-low additive jitter: 45 fs rms
- Wide frequency range: dc to 725 MHz
- Any-format input with pin selectable output formats: LVPECL, Low Power LVPECL, LVDS, CML, HCSL, LVCMOS
- 2:1 mux with hot-swappable inputs
- Glitchless input clock switching (1 MHz to 725 MHz)
- Individual output enable
- Synchronous output enable
- Low output-output skew: <70 ps
- Low propagation delay variation: <400 ps
- Independent V_{DD} and V_{DDO} : 1.8/2.5/3.3 V
- Excellent power supply noise rejection (PSRR)
- Selectable LVCMOS drive strength to tailor jitter and EMI performance
- Small size: 44-QFN (7 mm x 7 mm)
- RoHS compliant, Pb-free
- Industrial temperature range: –40 to +85 °C

Ordering Information:
See page 30.

Applications

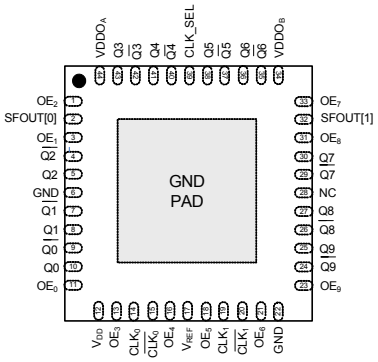
- High-speed clock distribution
- Ethernet switch/router
- Optical Transport Network (OTN)
- SONET/SDH
- PCI Express Gen 1/2/3
- Storage
- Telecom
- Industrial
- Servers
- Backplane clock distribution

Description

The Si53305 is an ultra low jitter ten output differential buffer with pin-selectable output clock signal format and individual OE. The Si53305 features a 2:1 mux with glitchless switching, making it ideal for redundant clocking applications. The Si53305 utilizes Silicon Laboratories' advanced CMOS technology to fanout clocks from dc to 725 MHz with guaranteed low additive jitter, low skew, and low propagation delay variability. The Si53305 features minimal cross-talk and provides superior supply noise rejection, simplifying low jitter clock distribution in noisy environments. Independent core and output bank supply pins provide integrated level translation without the need for external circuitry.

Pin Assignments

Si53305



Patents pending

Functional Block Diagram

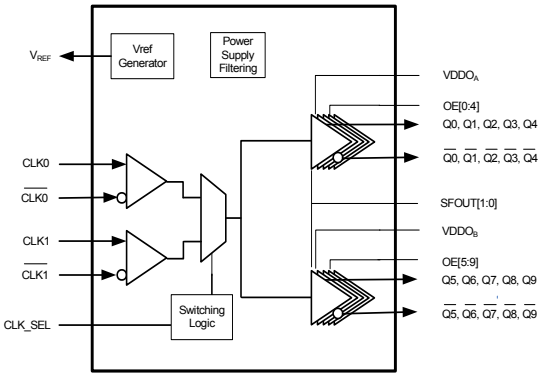


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature	T_A		–40	—	85	°C
Supply Voltage Range*	V_{DD}	LVDS, CML	1.71	1.8	1.89	V
			2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		LVPECL, low power LVPECL, LVCMOS	2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		HCSL	2.97	3.3	3.63	V
Output Buffer Supply Voltage*	V_{DDOX}	LVDS, CML, LVCMOS	1.71	1.8	1.89	V
			2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		LVPECL, low power LVPECL	2.38	2.5	2.63	V
			2.97	3.3	3.63	V
		HCSL	2.97	3.3	3.63	V

***Note:** Core supply V_{DD} and output buffer supplies V_{DDO} are independent. LVCMOS clock input is not supported for V_{DD} = 1.8V but is supported for LVCMOS clock output for V_{DDOX} = 1.8V. LVCMOS outputs at 1.5V and 1.2V can be supported via a simple resistor divider network. See “2.9.1. LVCMOS Output Termination To Support 1.5V and 1.2V”

Table 2. Input Clock Specifications

(V_{DD}=1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A=–40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential Input Common Mode Voltage	V_{CM}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	0.05	—	—	V
Differential Input Swing (peak-to-peak)	V_{IN}		0.2	—	2.2	V
LVCMOS Input High Voltage	V_{IH}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	V_{DD} x 0.7	—	—	V
LVCMOS Input Low Voltage	V_{IL}	V_{DD} = 2.5 V± 5%, 3.3 V± 10%	—	—	V_{DD} x 0.3	V
Input Capacitance	C_{IN}	CLK0 and CLK1 pins with respect to GND	—	5	—	pF

Table 3. DC Common Characteristics

(V_{DD} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_{DD}		—	65	100	mA
Output Buffer Supply Current (Per Clock Output) @100 MHz (diff) @200 MHz (CMOS)	I_{DDOX}	LVPECL (3.3 V)	—	35	—	mA
		Low Power LVPECL (3.3 V)*	—	35	—	mA
		LVDS (3.3 V)	—	20	—	mA
		CML (3.3 V)	—	30	—	mA
		HCSL, 100 MHz, 2 pF load (3.3 V)	—	35	—	mA
		CMOS (1.8 V, SFOUT = Open/0), per output, C_L = 5 pF, 200 MHz	—	5	—	mA
		CMOS (2.5 V, SFOUT = Open/0), per output, C_L = 5 pF, 200 MHz	—	8	—	mA
		CMOS (3.3 V, SFOUT = 0/1), per output, C_L = 5 pF, 200 MHz	—	15	—	mA
Input Clock Voltage Reference	V_{REF}	V_{REF} pin I_{REF} = +/-500 µA	—	V_{DD}/2	—	V
Input High Voltage	V_{IH}	SFOUT, CLK_SEL, OEx	0.8 x V_{DD}	—	—	V
Input Mid Voltage	V_{IM}	SFOUT, 3-level input pins	0.45 x V_{DD}	0.5 x V_{DD}	0.55 x V_{DD}	V
Input Low Voltage	V_{IL}	SFOUT, CLK_SEL, OEx	—	—	0.2 x V_{DD}	V
Internal Pull-down Resistor	R_{DOWN}	CLK_SEL, SFOUT	—	25	—	kΩ
Internal Pull-up Resistor	R_{UP}	OEx, SFOUT	—	25	—	kΩ

***Note:** Low-power LVPECL mode supports an output termination scheme that will reduce overall system power.

Table 4. Output Characteristics (LVPECL)

(V_{DDOX} = 2.5 V ± 5%, or 3.3 V ± 10%,TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	V_{COM}		V_{DDOX} – 1.595	—	V_{DDOX} – 1.245	V
Single-Ended Output Swing*	V_{SE}		0.55	0.80	1.050	V
***Note:** Unused outputs can be left floating. Do not short unused outputs to ground.						

Table 5. Output Characteristics (Low Power LVPECL)

(V_{DDOX} = 2.5 V ± 5%, or 3.3 V ± 10%,TA = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output DC Common Mode Voltage	V_{COM}	R_L = 100 Ω across Qn and $\overline{Qn}$	V_{DDOX} – 1.895		V_{DDOX} – 1.275	V
Single-Ended Output Swing	V_{SE}	R_L = 100 Ω across Qn and $\overline{Qn}$	0.25	0.60	0.85	V

Table 6. Output Characteristics—CML

(V_{DDOX} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	V_{SE}	Terminated as shown in Figure 9 (CML termination).	300	400	550	mV

Table 7. Output Characteristics—LVDS

(V_{DDOX} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single-Ended Output Swing	V_{SE}	R_L = 100 Ω across Q_N and $\overline{Q}_N$	247	—	490	mV
Output Common Mode Voltage (V_{DDO} = 2.5 V or 3.3V)	V_{COM1}	V_{DDOX} = 2.38 to 2.63 V, 2.97 to 3.63 V, R_L = 100 Ω across Q_N and $\overline{Q}_N$	1.10	1.25	1.35	V
Output Common Mode Voltage (V_{DDO} = 1.8 V)	V_{COM2}	V_{DDOX} = 1.71 to 1.89 V, R_L = 100 Ω across Q_N and $\overline{Q}_N$	0.85	0.97	1.25	V

Table 8. Output Characteristics—LVCMOS

(V_{DDOX} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High*	V_{OH}		0.75 x V_{DDOX}	—	—	V
Output Voltage Low*	V_{OL}		—	—	0.25 x V_{DDOX}	V
***Note:** I_{OH} and I_{OL} per the Output Signal Format Table for specific V_{DDOX} and SFOUT settings.						

Table 9. Output Characteristics—HCSL

(V_{DDOX} = 3.3 V ± 10%, T_A = –40 to 85 °C))

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage High	V_{OH}	R_L = 50 Ω to GND	550	700	900	mV
Output Voltage Low	V_{OL}	R_L = 50 Ω to GND	–150	0	150	mV
Single-Ended Output Swing	V_{SE}	R_L = 50 Ω to GND	550	700	850	mV
Crossing Voltage	V_C	R_L = 50 Ω to GND	250	350	550	mV

Table 10. AC Characteristics

(V_{DD} = V_{DDOX} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%, T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency	F	LVPECL, low power LVPECL, LVDS, CML, HCSL (Glitchless switching to a min of 1 MHz)	dc	—	725	MHz
		LVCMOS (Glitchless switching to a min of 1 MHz)	dc	—	200	MHz
Duty Cycle **Note:** 50% input duty cycle.	D_C	200 MHz, 20/80% T_R/T_F<10% of period (LVCMOS) (12 mA drive)	40	50	60	%
		20/80% T_R/T_F<10% of period (Differential)	48	50	52	%
Minimum Input Clock Slew Rate[1]	SR	Required to meet prop delay and additive jitter specifications (20–80%)	0.75	—	—	V/ns
Output Rise/Fall Time	T_R/T_F	LVDS, 20/80%	—	—	325	ps
		LVPECL, 20/80%	—	—	350	ps
		HCSL[1], 20/80%	—	—	280	ps
		CML, 20/80%	—	—	350	ps
		Low-Power LVPECL, 20/80%	—	—	325	ps
		LVCMOS 200 MHz, 20/80%, 2 pF load	—	—	750	ps
Minimum Input Pulse Width	T_W		500	—	—	ps
Propagation Delay	T_{PLH}, T_{PHL}	LVCMOS (12mA drive with no load)	1250	2000	2750	ps
		LVPECL	600	800	1000	ps
		LVDS	600	800	1000	ps
Output Enable Time	T_{EN}	F = 1 MHz	—	2500	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	5	—	ns

Notes:

1. HCSL measurements were made with receiver termination. See Figure 9 on page 19.
2. Output to Output skew specified for outputs with an identical configuration.
3. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (3.3 V = 100 mV_{PP}) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

Table 10. AC Characteristics (Continued)

(V_{DD} = V_{DDOX} = 1.8 V ± 5%, 2.5 V ± 5%, or 3.3 V ± 10%,T_A = –40 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Disable Time	T_{DIS}	F = 1 MHz	—	2000	—	ns
		F = 100 MHz	—	30	—	ns
		F = 725 MHz	—	5	—	ns
Output to Output Skew[2]	T_{SK}	LVCMOS (12 mA drive to no load)	—	50	120	ps
		LVPECL	—	35	70	ps
		LVDS	—	35	70	ps
Part to Part Skew[3]	T_{PS}	Differential	—	—	150	ps
Power Supply Noise Rejection[4]	PSRR	10 kHz sinusoidal noise	—	–63	—	dBc
		100 kHz sinusoidal noise	—	–62	—	dBc
		500 kHz sinusoidal noise	—	–58	—	dBc
		1 MHz sinusoidal noise	—	–55	—	dBc

Notes:

1. HCSL measurements were made with receiver termination. See Figure 9 on page 19.
2. Output to Output skew specified for outputs with an identical configuration.
3. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (3.3 V = 100 mV_{PP}) and noise spur amplitude measured. See “AN491: Power Supply Rejection for Low-Jitter Clocks” for further details.

Table 11. Additive Jitter, Differential Clock Input

V_{DD}	Input[1,2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (Single-Ended, Peak-to-Peak)	Differential 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	725	Differential	0.15	0.637	LVPECL	45	65
3.3	725	Differential	0.15	0.637	LVDS	50	65
3.3	156.25	Differential	0.5	0.458	LVPECL	160	185
3.3	156.25	Differential	0.5	0.458	LVDS	150	200
2.5	725	Differential	0.15	0.637	LVPECL	45	65
2.5	725	Differential	0.15	0.637	LVDS	50	65
2.5	156.25	Differential	0.5	0.458	LVPECL	145	185
2.5	156.25	Differential	0.5	0.458	LVDS	145	195

Notes:
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. AC-coupled differential inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.

Table 12. Additive Jitter, Single-Ended Clock Input

V_{DD}	Input[1,2]				Output	Additive Jitter (fs rms, 12 kHz to 20 MHz)[3]	
	Freq (MHz)	Clock Format	Amplitude V_{IN} (single-ended, peak to peak)	SE 20%-80% Slew Rate (V/ns)	Clock Format	Typ	Max
3.3	200	Single-ended	1.70	1	LVCMOS[4]	120	160
3.3	156.25	Single-ended	2.18	1	LVPECL	160	185
3.3	156.25	Single-ended	2.18	1	LVDS	150	200
3.3	156.25	Single-ended	2.18	1	LVCMOS[4]	130	180
2.5	200	Single-ended	1.70	1	LVCMOS[5]	120	160
2.5	156.25	Single-ended	2.18	1	LVPECL	145	185
2.5	156.25	Single-ended	2.18	1	LVDS	145	195
2.5	156.25	Single-ended	2.18	1	LVCMOS[5]	140	180

Notes:
1. For best additive jitter results, use the fastest slew rate possible. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.
2. DC-coupled single-ended inputs.
3. Measured differentially using a balun at the phase noise analyzer input. See Figure 1.
4. Drive Strength: 12 mA, 3.3 V (SFOUT = 11). LVCMOS jitter is measured single-ended.
5. Drive Strength: 9 mA, 2.5 V (SFOUT = 11). LVCMOS jitter is measured single-ended.

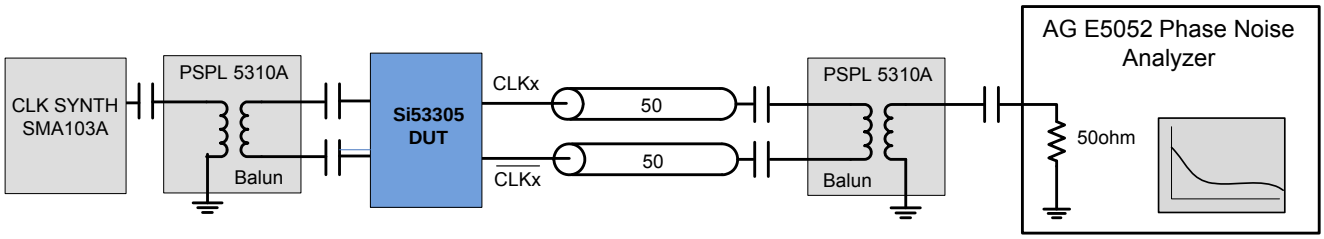


Figure 1. Differential Measurement Method Using a Balun

Table 13. Thermal Conditions

Parameter	Symbol	Test Condition	Value	Unit
Thermal Resistance, Junction to Ambient	θ_{JA}	Still air	49.6	°C/W
Thermal Resistance, Junction to Case	θ_{JC}	Still air	32.3	°C/W

Table 14. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage Temperature	T_S		–55	—	150	°C
Supply Voltage	V_{DD}		–0.5	—	3.8	V
Input Voltage	V_{IN}		–0.5	—	V_{DD}+ 0.3	V
Output Voltage	V_{OUT}		—	—	V_{DD}+ 0.3	V
ESD Sensitivity	HBM	HBM, 100 pF, 1.5 kΩ	—	—	2000	V
ESD Sensitivity	CDM		—	—	500	V
Peak Soldering Reflow Temperature	T_{PEAK}	Pb-Free; Solder reflow profile per JEDEC J-STD-020	—	—	260	°C
Maximum Junction Temperature	T_J		—	—	125	°C

Note: Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

2. Functional Description

The Si53305 is a low jitter, low skew 1:10 differential buffer with an integrated 2:1 input mux and individual OE control. The device has a universal input that accepts most common differential or LVCMOS input signals. A clock select pin is used to select the active input clock. The Si53305 features two control pins to select the signal format and LVCMOS drive strength settings. In addition, each clock output has an independent OE pin for individual clock enable/disable.

2.1. Universal, Any-Format Input

The universal input stage enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. Tables 15 and 16 summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended as low slew rates can increased the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See “AN766: Understanding and Optimizing Clock Buffer’s Additive Jitter Performance” for more information.

Table 15. LVPECL, LVCMOS, and LVDS Input Clock Options

	LVPECL		LVCMOS		LVDS	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	N/A	N/A	No	No	Yes	No
2.5/3.3 V	Yes	Yes	No	Yes	Yes	Yes

Table 16. HCSL and CML Input Clock Options

	HCSL		CML	
	AC-Couple	DC-Couple	AC-Couple	DC-Couple
1.8 V	No	No	Yes	No
2.5/3.3 V	Yes (3.3 V)	Yes (3.3 V)	Yes	No

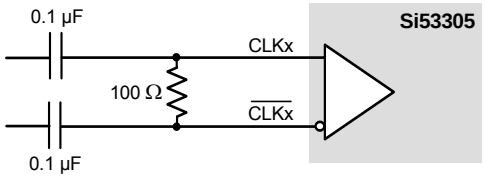


Figure 2. Differential HCSL, LVPECL, Low-Power LVPECL, LVDS, CML AC-Coupled Input Termination

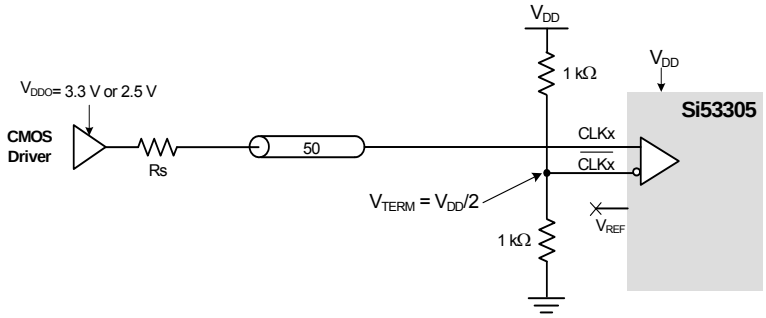
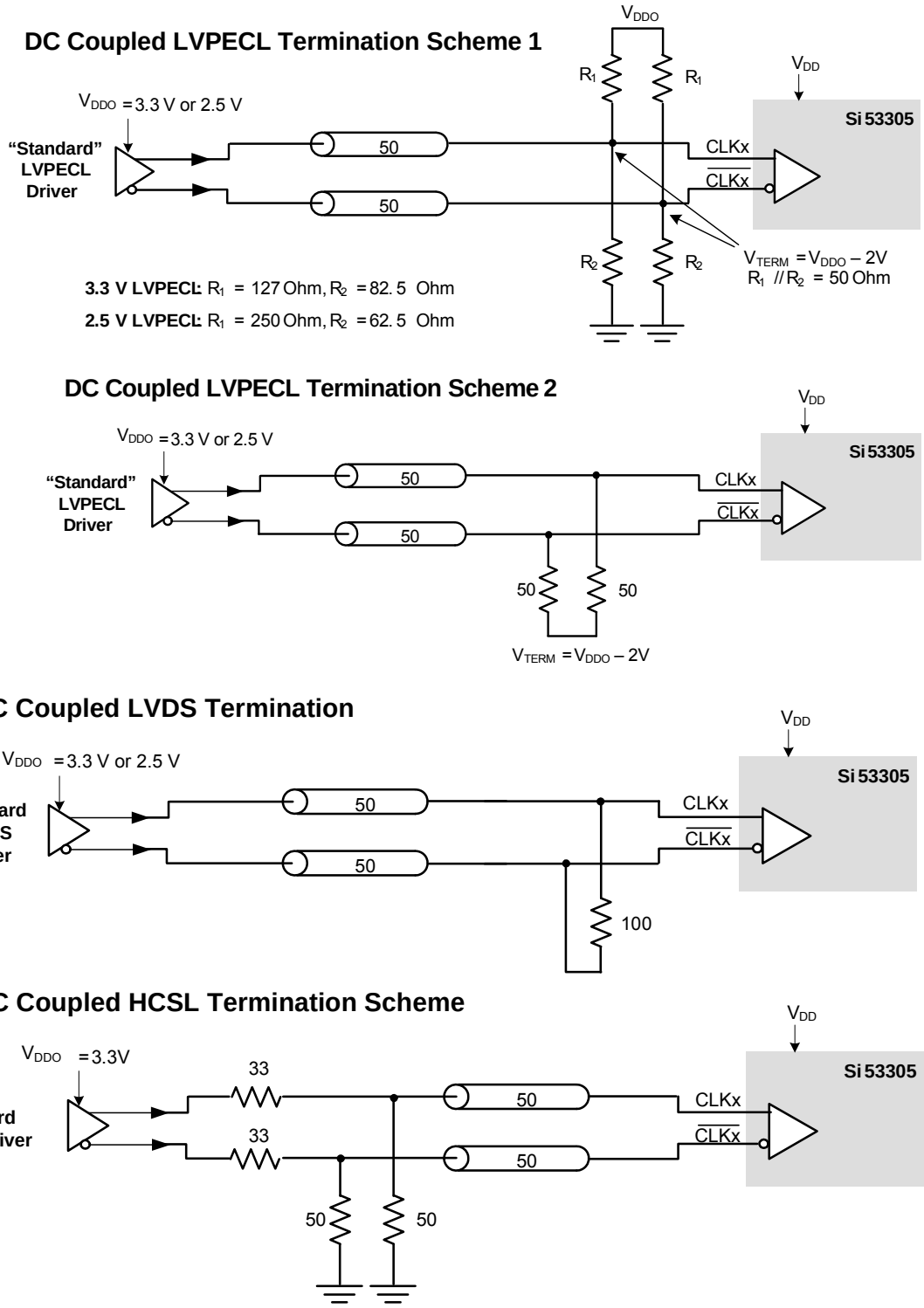


Figure 3. LVCMOS DC-Coupled Input Termination



Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 4. Differential DC-Coupled Input Terminations

2.2. Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The noninverting input is biased with a 18.75 kΩ pulldown to GND and a 75 kΩ pullup to V_{DD}. The inverting input is biased with a 75 kΩ pullup to V_{DD}.

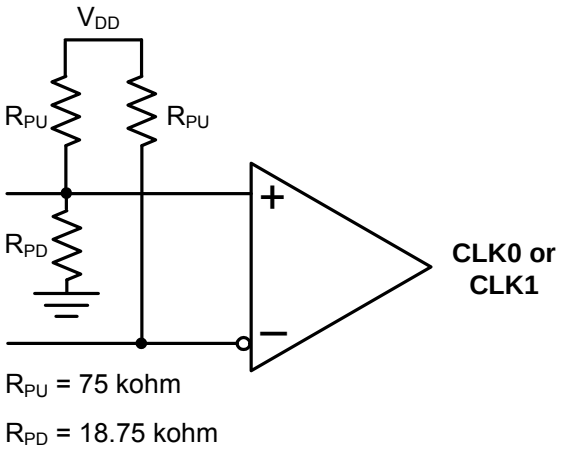


Figure 5. Input Bias Resistors

2.3. Voltage Reference (V_{REF})

The V_{REF} pin is used to bias the input receiver as shown in Figure 6 when a single-ended input clock (such as LVCMOS) is used. Note that $V_{REF}=V_{DD}/2$ and should be compatible with the VCM rating of the single-ended input clock driving the CLK0 or CLK1 inputs. To optimize jitter and duty cycle performance, use the circuit in Figure 3. V_{REF} pin should be left floating when differential clocks are used.

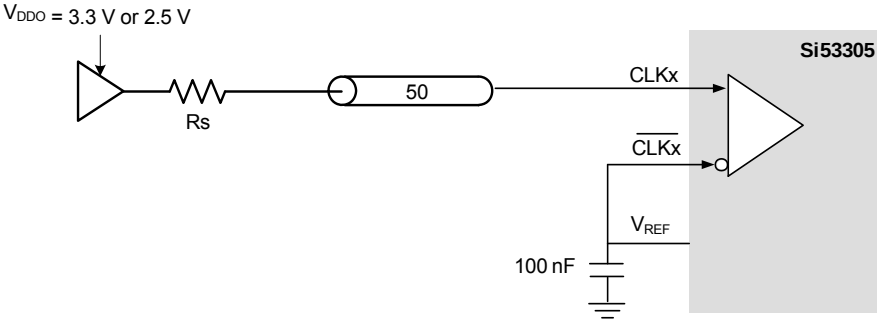


Figure 6. Using Voltage Reference with Single-Ended Input Clock

2.4. Universal, Any-Format Output Buffer

The highly flexible output drivers support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUT[1] and SFOUT[0] are 3-level inputs that can be pin-strapped to select the Bank A and Bank B clock signal formats. This feature enables the device to be used for format translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each V_{DDO} setting.

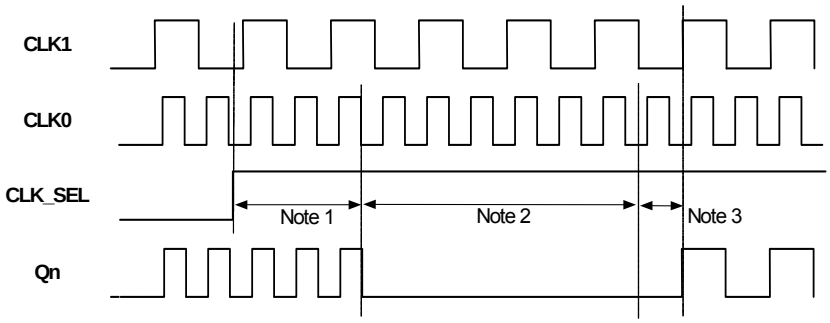
Table 17. Output Signal Format Selection

SFOUT[1]	SFOUT[0]	V_{DDOX} = 3.3 V	V_{DDOX} = 2.5 V	V_{DDOX} = 1.8 V
Open*	Open*	LVPECL	LVPECL	N/A
0	0	LVDS	LVDS	LVDS
0	1	LVCMOS, 24 mA drive	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive
1	0	LVCMOS, 18 mA drive	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive
1	1	LVCMOS, 12 mA drive	LVCMOS, 9 mA drive	LVCMOS, 6 mA drive
Open*	0	LVCMOS, 6 mA drive	LVCMOS, 4 mA drive	LVCMOS, 2 mA drive
Open*	1	LVPECL low power	LVPECL low power	N/A
0	Open*	CML	CML	CML
1	Open*	HCSL	N/A	N/A

***Note:** SFOUT[1] and SFOUT[0] are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin floats to $V_{DD}/2$.

2.5. Glitchless Clock Input Switching

The input clock mux features glitchless switching between two valid input clocks. Figure 7 illustrates that switching between input clocks does not generate runt pulses or glitches at the output.



Notes:

1. Q_n continues with CLK0 for 2-3 falling edges of CLK0.
2. Q_n is disabled low for 2-3 falling edges of CLK1 .
3. Q_n starts on the first rising edge after 1 + 2.

Figure 7. Glitchless Input Clock Switch

Glitchless switching between 2 input clocks that are up to 10x different in frequency and between 1 MHz and 725 MHz is supported. When a switchover to a new clock is made, the output will disable low after two or three clock cycles of the previously-selected input clock. The outputs will remain low for up to three clock cycles of the newly-selected clock, after which the outputs will start from the newly-selected input. In the case a switchover to an absent clock is made, the output will glitchlessly stop low and wait for edges of the newly selected clock. A switchover from an absent clock to a live clock will also be glitchless. Note that the CLK_SEL input should not be toggled faster than 1/250th the frequency of the slower input clock.

2.6. Synchronous Output Enable

This buffer features a synchronous output enable (disable) feature. Output enable is sampled and synchronized on the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.

When OE is low, Q is held low and $\overline{Q}$ is held high for differential output formats. For LVCMOS output format options, both Q and $\overline{Q}$ are held low when OE is set low. The device outputs are enabled when the output enable pin is unconnected. See Table 10, “AC Characteristics,” on page 7 for output enable and output disable times.

2.7. Input Mux and Output Enable Logic

Two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input. The table below summarizes the input and output clock based on the input mux and output enable pin settings.

Table 18. Input Mux and Output Enable Logic

CLK_SEL	CLK0	CLK1	OE[1]	Q[2]
L	L	X	H	L
L	H	X	H	H
H	X	L	H	L
H	X	H	H	H
X	X	X	L	L[3]

Notes:
1. Output enable active high
2. On the next negative transition of CLK0 or CLK1.
3. Single-end: Q = low, $\overline{Q}$ = low
   Differential: Q = low, $\overline{Q}$ = high

2.8. Power Supply (V_{DD} and V_{DDOX})

The device includes separate core (V_{DD}) and output driver supplies (V_{DDOX}). This feature allows the core to operate at a lower voltage than V_{DDO}, reducing current consumption in mixed supply applications. The core V_{DD} supports 3.3 V, 2.5 V, or 1.8 V. Each output bank has its own V_{DDOX} supply, supporting 3.3 V, 2.5 V, or 1.8 V.

2.9. Output Clock Termination Options

The recommended output clock termination options are shown below.

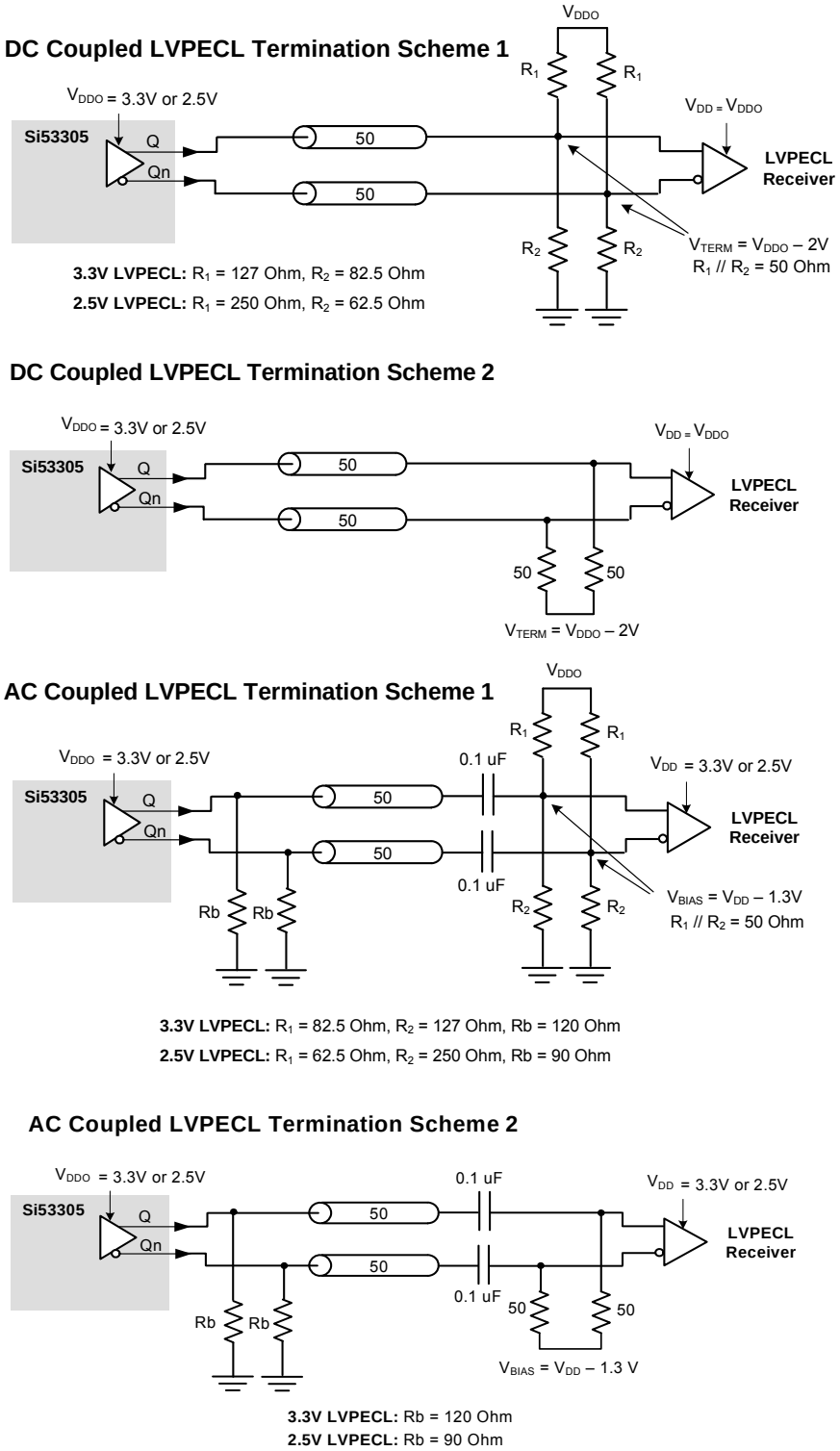
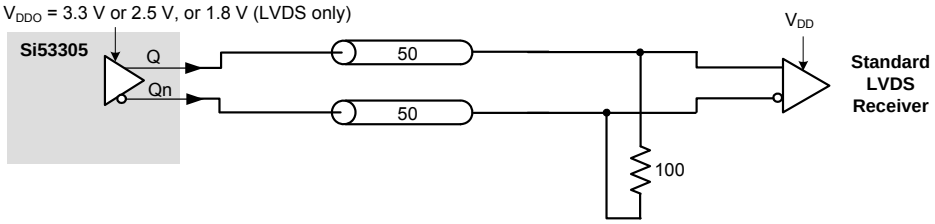
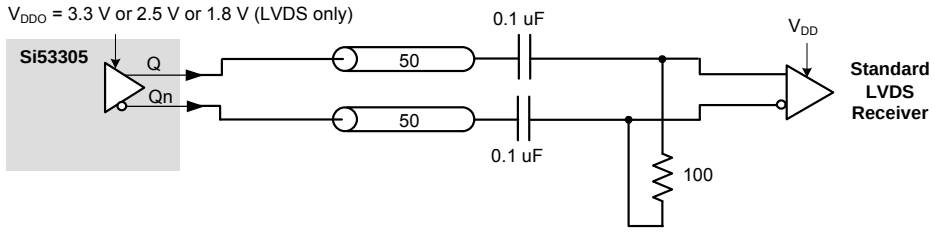


Figure 8. LVPECL Output Termination

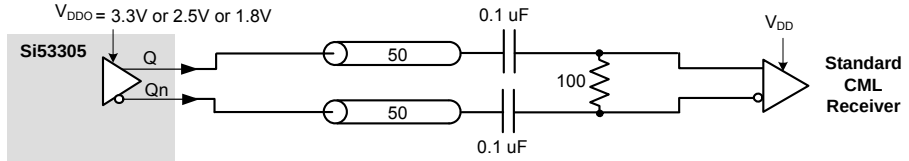
DC Coupled LVDS and Low-Power LVPECL Termination



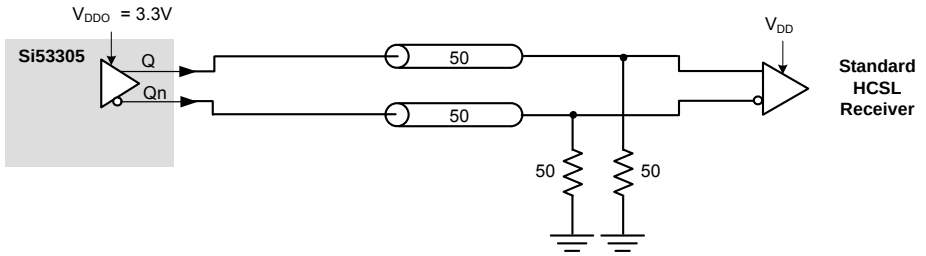
AC Coupled LVDS and Low-Power LVPECL Termination



AC Coupled CML Termination



DC Coupled HCSL Receiver Termination



DC Coupled HCSL Source Termination

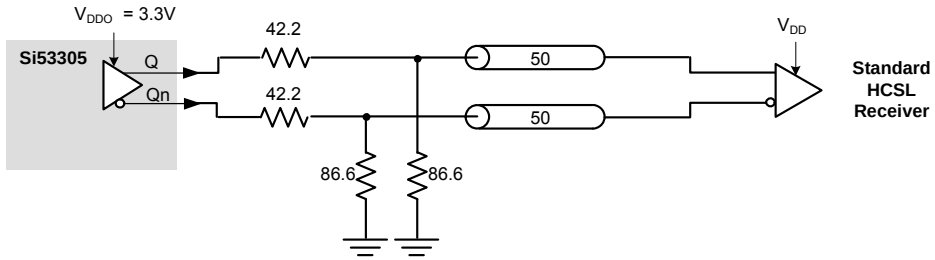


Figure 9. LVDS, CML, HCSL, and Low-Power LVPECL Output Termination

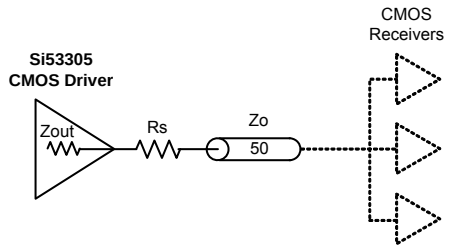


Figure 10. LVCMOS Output Termination

Table 19. Recommended LVCMOS R_S Series Termination

SFOUT[1]	SFOUT[0]	R_S (ohms)		
		3.3 V	2.5 V	1.8 V
0	1	33	33	33
1	0	33	33	33
1	1	33	33	0
Open	0	0	0	0

2.9.1. LVCMOS Output Termination To Support 1.5V and 1.2V

LVCMOS clock outputs are natively supported at 1.8V, 2.5V, and 3.3V. However, 1.2V and 1.5V LVCMOS clock outputs can be supported via a simple resistor divider network that will translate the buffer's 1.8V output to a lower voltage as shown in Figure 11 below.

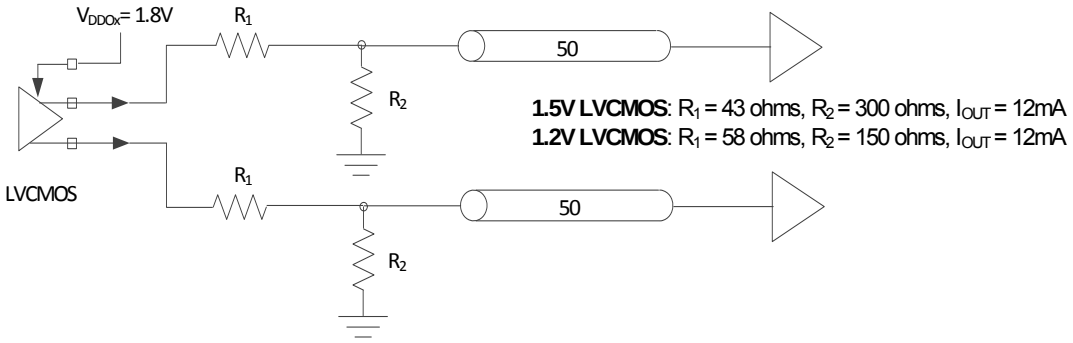


Figure 11. 1.5V and 1.2V LVCMOS Low-Voltage Output Termination

2.10. AC Timing Waveforms

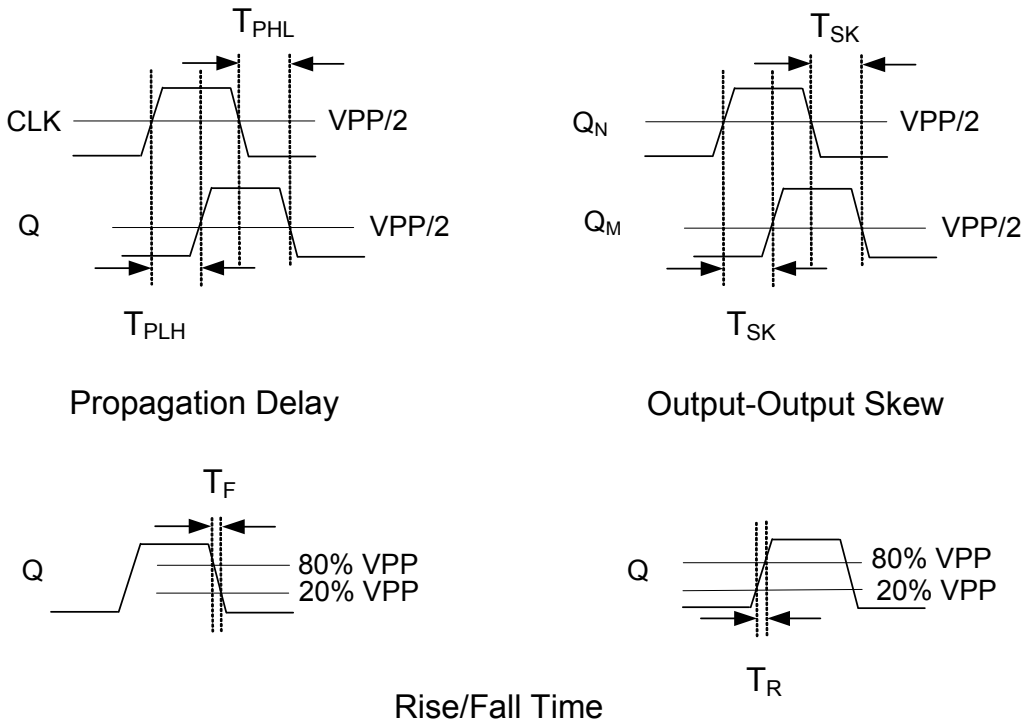


Figure 12. AC Waveforms

2.11. Typical Phase Noise Performance

Each of the following three figures shows three phase noise plots superimposed on the same diagram.

Source Jitter: Reference clock phase noise.

Total Jitter (SE): Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.

Total Jitter (Diff): Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. See Figure 1 on page 10.

Note: To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

The total jitter is a measure of the source plus the buffer's additive phase jitter. The additive jitter (rms) of the buffer can then be calculated (via root-sum-square addition).

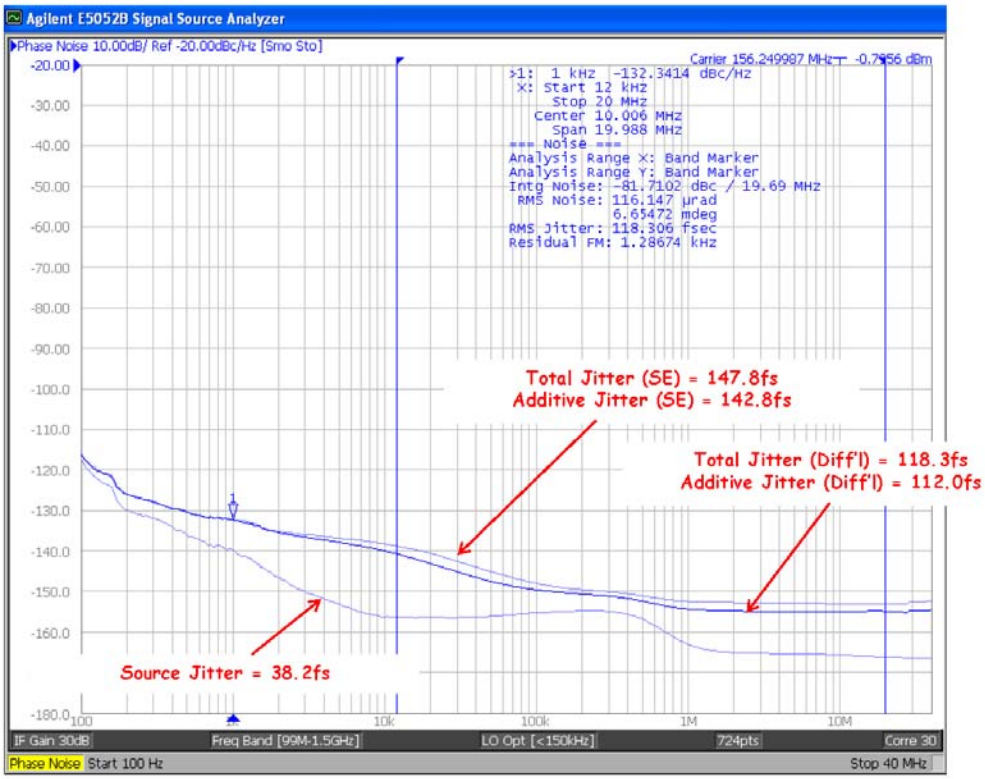


Figure 13. Source, Additive, and Total Jitter (156.25 MHz)

Table 20. Source, Additive, and Total Jitter (156.25 MHz)

Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
156.25	1.0	38.2	147.8	142.8	118.3	112.0

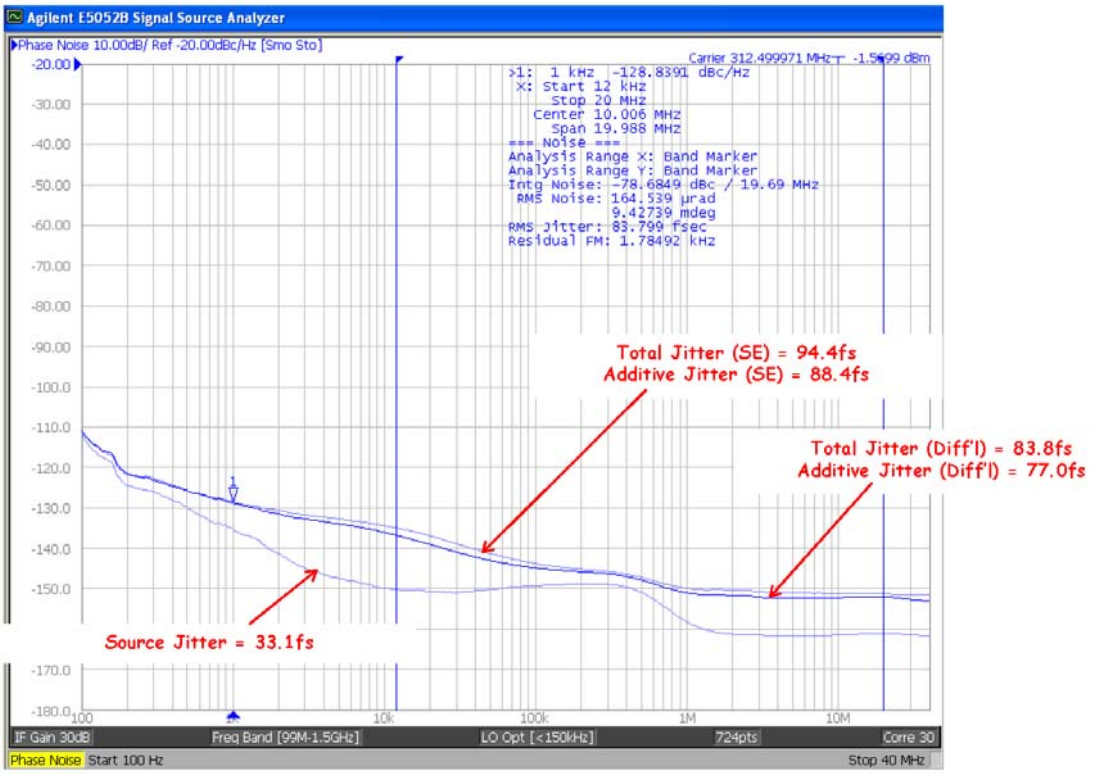


Figure 14. Source, Additive, and Total Jitter (312.5 MHz)

Table 21. Source, Additive, and Total Jitter (312.5 MHz)

Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
312.5	1.0	33.10	94.39	88.39	83.80	76.99

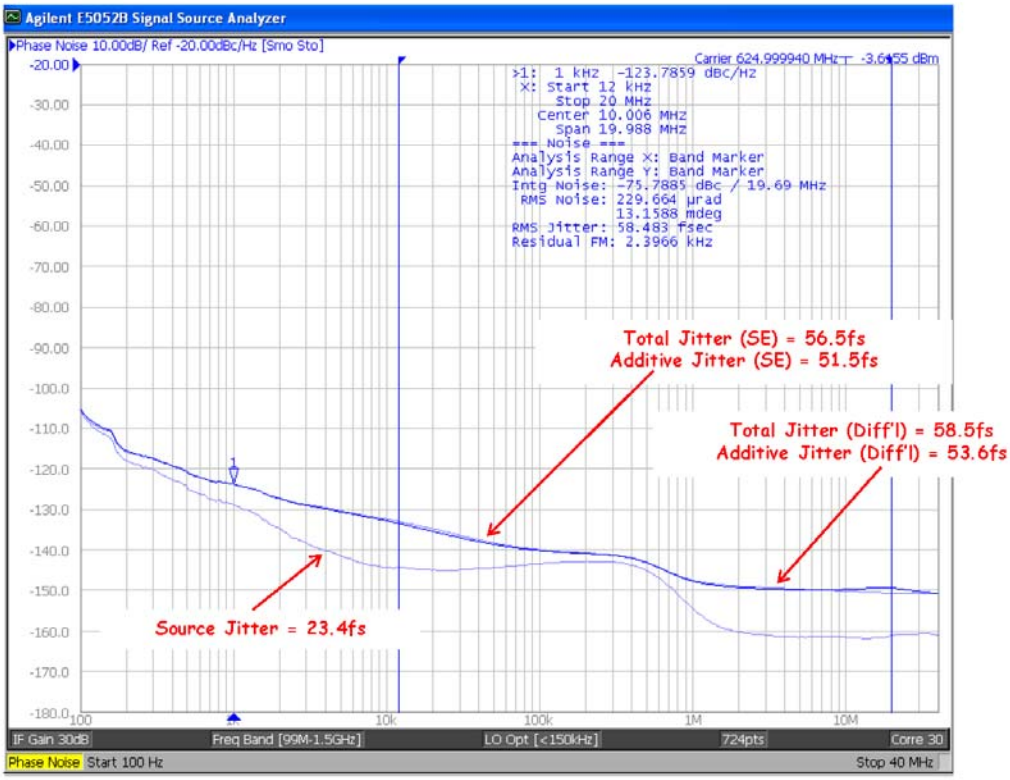


Figure 15. Source, Additive, and Total Jitter (625 MHz)

Table 22. Source, Additive, and Total Jitter (625 MHz)

Frequency (MHz)	Diff'l Input Slew Rate (V/ns)	Source Jitter (fs)	Total Jitter (SE) (fs)	Additive Jitter (SE) (fs)	Total Jitter (Diff'l) (fs)	Additive Jitter (Diff'l) (fs)
625	1.0	23.4	56.5	51.5	58.5	53.6

2.12. Input Mux Noise Isolation

The buffer's input clock mux is designed to minimize crosstalk between the CLK0 and CLK1. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. Figure 16 below is a measurement the input mux's noise isolation.

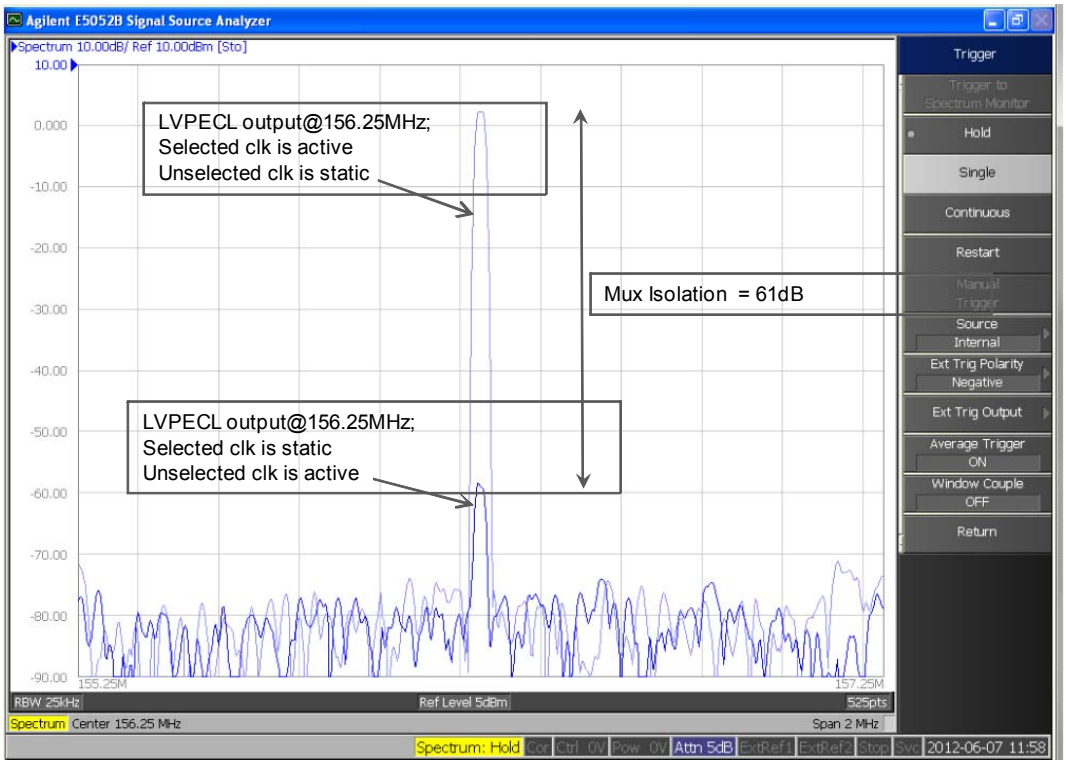


Figure 16. Input Mux Noise Isolation

2.13. Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject noise present on the power supply, simplifying low jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. For more information, see "AN491: Power Supply Rejection for Low Jitter Clocks".

3. Pin Description: 44-Pin QFN

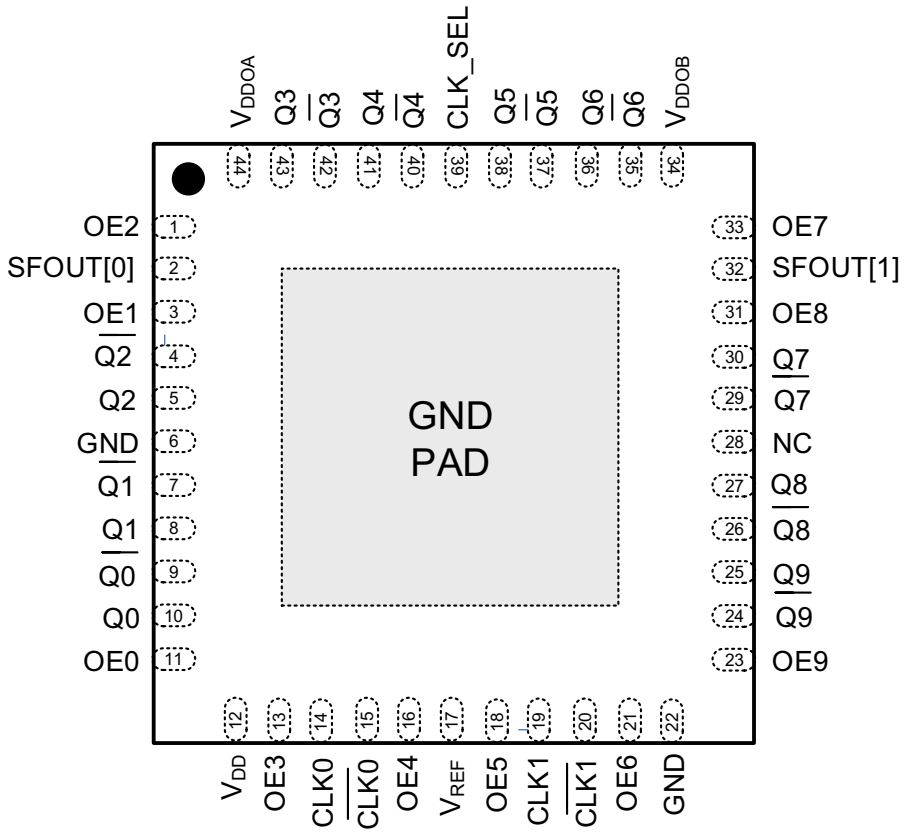


Table 23. Pin Description

Pin #	Name	Description
1	OE2	Output enable-Output 2. When OE2 = high, the Q2 is enabled. When OE2 = low, Q2 is held low, and $\overline{Q2}$ is held high for differential formats. For LVCMOS, both Q2 and $\overline{Q2}$ are held low when OE2 is set low. OE2 contains an internal pull-up resistor.
2	SFOUT[0]	Output signal format control pin [0]. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD}.
3	OE1	Output enable-Output 1. When OE1 = high, the Q1 is enabled. When OE1 = low, Q1 is held low, and $\overline{Q1}$ is held high for differential formats. For LVCMOS, both Q1 and $\overline{Q1}$ are held low when OE1 is set low. OE1 contains an internal pull-up resistor.
4	$\overline{Q2}$	Output clock 2 (complement).
5	Q2	Output clock 2.
6	GND	Ground.

Table 23. Pin Description (Continued)

Pin #	Name	Description
7	$\overline{Q1}$	Output clock 1 (complement).
8	Q1	Output clock 1.
9	$\overline{Q0}$	Output clock 0 (complement).
10	Q0	Output clock 0.
11	OE0	Output enable-Output 0. When OE0 = high, Q0 and $\overline{Q0}$ outputs are enabled. When OE0 = low, Q0 is held low, and $\overline{Q0}$ is held high for differential formats. For LVCMOS, both Q0 and $\overline{Q0}$ are held low when OE0 is set low. OE0 contains an internal pull-up resistor.
12	V_{DD}	Core voltage supply. Bypass with 1 µF capacitor placed as close to the V_{DD} pin as possible.
13	OE3	Output Enable 3. When OE3 = high, Q3 and $\overline{Q3}$ outputs are enabled. When OE3 = low, Q3 is held low, and $\overline{Q3}$ is held high for differential formats. For LVCMOS, both Q3 and $\overline{Q3}$ are held low when OE3 is set low. OE3 contains an internal pull-up resistor.
14	CLK0	Input clock 0.
15	$\overline{CLK0}$	Input clock 0 (complement). When CLK0 is driven by a single-ended LVCMOS input, connect $\overline{CLK0}$ to $V_{DD}/2$.
16	OE4	Output Enable 4. When OE4 = high, Q4 and $\overline{Q4}$ outputs are enabled. When OE4 = low, Q4 is held low, and $\overline{Q4}$ is held high for differential formats. For LVCMOS, both Q4 and $\overline{Q4}$ are held low when OE4 is set low. OE4 contains an internal pull-up resistor.
17	V_{REF}	Reference voltage for single-ended CMOS clocks. V_{REF} is an output voltage and is equal to $V_{DD}/2$. See “2.3. Voltage Reference (VREF)” for more details.
18	OE5	Output Enable 5. When OE5 = high, Q5 and $\overline{Q5}$ outputs are enabled. When OE5 = low, Q5 is held low, and $\overline{Q5}$ is held high for differential formats. For LVCMOS, both Q5 and $\overline{Q5}$ are held low when OE5 is set low. OE5 contains an internal pull-up resistor.
19	CLK1	Input clock 1.
20	$\overline{CLK1}$	Input clock 1 (complement). When CLK1 is driven by a single-ended LVCMOS input, connect $\overline{CLK1}$ to $V_{DD}/2$.

Table 23. Pin Description (Continued)

Pin #	Name	Description
21	OE6	Output Enable 6. When OE6 = high, Q6 and $\overline{Q6}$ outputs are enabled. When OE6 = low, Q6 is held low, and $\overline{Q6}$ is held high for differential formats. For LVCMOS, both Q6 and $\overline{Q6}$ are held low when OE6 is set low. OE6 contains an internal pull-up resistor.
22	GND	Ground.
23	OE9	Output Enable 9. When OE9 = high, Q9 and $\overline{Q9}$ outputs are enabled. When OE9 = low, Q9 is held low, and $\overline{Q9}$ is held high for differential formats. For LVCMOS, both Q9 and $\overline{Q9}$ are held low when OE9 is set low. OE9 contains an internal pull-up resistor.
24	$\overline{Q9}$	Output clock 9 (complement).
25	Q9	Output clock 9.
26	$\overline{Q8}$	Output clock 8 (complement).
27	Q8	Output clock 8.
28	NC	No connect.
29	$\overline{Q7}$	Output clock 7 (complement).
30	Q7	Output clock 7.
31	OE8	Output Enable 8. When OE8 = high, Q8 and $\overline{Q8}$ outputs are enabled. When OE8 = low, Q8 is held low, and $\overline{Q8}$ is held high for differential formats. For LVCMOS, both Q8 and $\overline{Q8}$ are held low when OE8 is set low. OE8 contains an internal pull-up resistor.
32	SFOUT[1]	Output signal format control pin [1]. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD}.
33	OE7	Output Enable 7. When OE7 = high, Q7 and $\overline{Q7}$ outputs are enabled. When OE7 = low, Q7 is held low, and $\overline{Q7}$ is held high for differential formats. For LVCMOS, both Q7 and $\overline{Q7}$ are held low when OE7 is set low. OE7 contains an internal pull-up resistor.
34	V_{DDOB}	Output Clock Voltage Supply—Bank B (Outputs: Q5 to Q9). Bypass with a 1µF capacitor placed as close to the pin as possible.
35	$\overline{Q6}$	Output clock 6 (complement).
36	Q6	Output clock 6.
37	$\overline{Q5}$	Output clock 5 (complement).
38	Q5	Output clock 5.

Table 23. Pin Description (Continued)

Pin #	Name	Description
39	CLK_SEL	MUX input select pin (LVCMOS). Clock inputs are switched without the introduction of glitches. When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor.
40	$\overline{Q4}$	Output clock 4 (complement).
41	Q4	Output clock 4.
42	$\overline{Q3}$	Output clock 3 (complement).
43	Q3	Output clock 3.
44	V_{DDOA}	Output Voltage Supply—Bank A (Outputs: Q0 to Q4). Bypass with a 1µF capacitor placed as close to the pin as possible.
GND Pad	GND	Ground Pad Power supply ground and thermal relief.

4. Ordering Guide

Part Number	Package	PB-Free, ROHS-6	Temperature
Si53305-B-GM	44-QFN	Yes	–40 to 85 °C

5. Package Outline

5.1. 7x7 mm 44-QFN Package Diagram

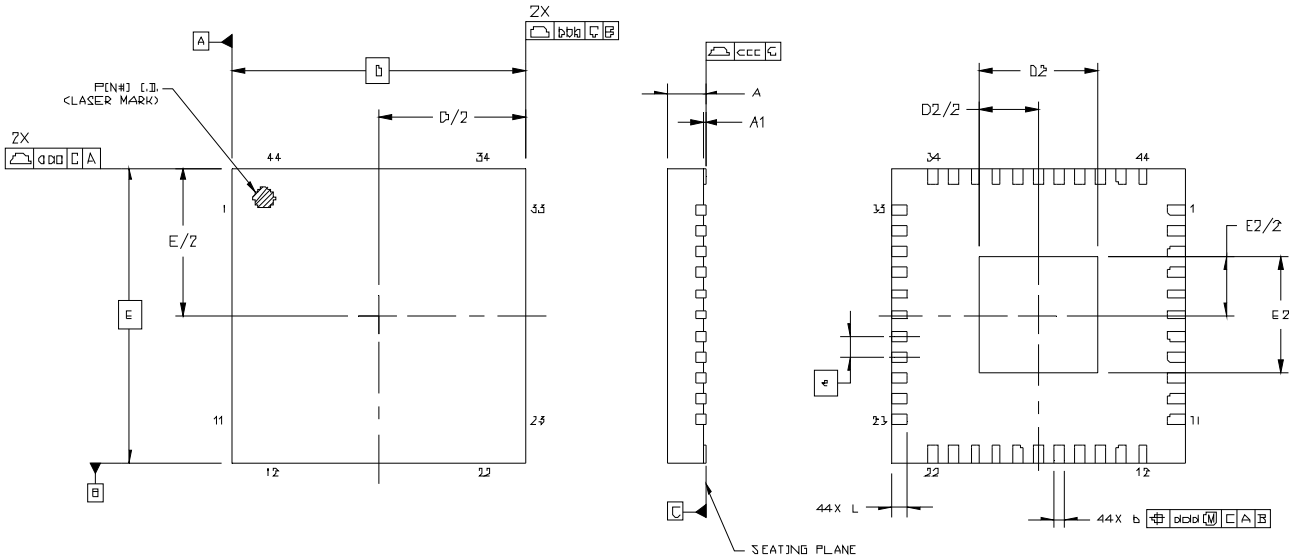


Figure 17. Si53305 7x7 mm 44-QFN Package Diagram

Table 24. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		7.00 BSC	
D2	2.65	2.80	2.95
e		0.50 BSC	
E		7.00 BSC	
E2	2.65	2.80	2.95
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6. PCB Land Pattern

6.1. 7x7 mm 44-QFN Package Land Pattern

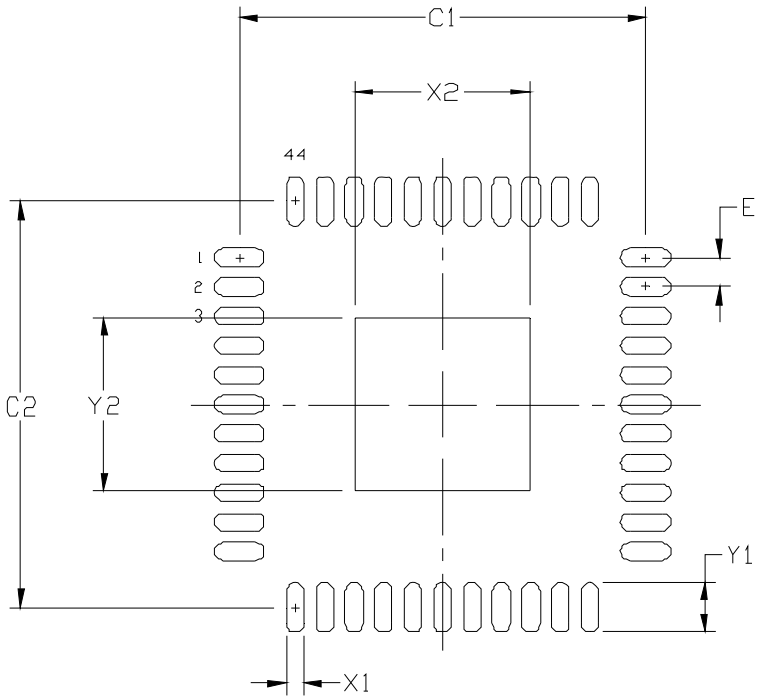


Figure 18. Si53305 7x7 mm 44-QFN Package Land Pattern

Table 25. PCB Land Pattern

Dimension	Min	Max	Dimension	Min	Max
C1	6.80	6.90	X2	2.85	2.95
C2	6.80	6.90	Y1	0.75	0.85
E	0.50 BSC		Y2	2.85	2.95
X1	0.20	0.30			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 1.0 mm square openings on 1.45 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Top Marking

7.1. Si53305 Top Marking

7.2. Top Marking Explanation

Mark Method:	Laser	
Font Size:	1.9 Point (26 mils) Right-Justified	
Line 1 Marking:	Device Part Number	**53305-B-GM**
Line 2 Marking:	YY = Year WW = Work Week	Assigned by Assembly Supplier. Corresponds to the year and work week of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	Circle = 1.3 mm Diameter Center-Justified	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	**TW**
Line 4 Marking	Circle = 0.75 mm Diameter Filled	Pin 1 Identification

Document Change List

Revision 0.4 to 1.0

- Updated frequency spec from 1MHz to dc.
- Updated operating conditions, including LVCMOS and HCSL voltage support.
- Updated tables 1-11.
- Updated section 2.1-2.12 text descriptions and diagrams.
- Improved data for additive jitter specifications.
- Improved typical phase noise plots.
- Improved performance specifications with more detail.

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