19-5722; Rev 0; 12/10

MAX2982

Industrial Broadband Power-Line Modem

General Description

The MAX2982 power-line transceiver utilizes state-of-the-art CMOS design techniques to deliver the highest level of performance, flexibility, and operational temperature range at reduced cost. This highly integrated design combines the Media Access Control (MAC) and the Physical (PHY) layers in a single device. The MAX2982 digital baseband and its companion device, the MAX2981 analog front-end (AFE) with integrated line driver, offer a complete high-speed power-line communication solution fully compliant with HomePlug® 1.0 Powerline Alliance Specification.

The MAX2982 offers reliable broadband communication for industrial environments. The PHY layer is comprised of 84-carrier OFDM modulation engine and Forward Error Correcting (FEC) blocks. The OFDM engine can modulate the signals in one of four modes of operation, namely DBPSK, DQPSK (1/2 rate FEC), DQPSK (3/4 rate FEC) and the ROBO mode. The MAX2982 offers -1dB SNR performance in ROBO mode, a robust mode of operation, to maintain communication over harsh industrial line conditions. Additionally, advanced narrow-band interference rejection circuitry provides immunity from jammer signals.

The MAX2982 offers extensive flexibility by integrating an ARM946E-S™ microprocessor allowing feature enhancement, worldwide regulatory compliance, and improved testability. Optional spectral shaping and notching profiles provide an unparalleled level of flexibility in system design. Additionally, the automatic channel adaptation and interference rejection features of the MAX2982 guarantee outstanding performance. Privacy is provided by a hard-macro DES encryption with key management.

The MAX2982 supports an IEEE® 802.3 standard *Media Independent Interface* (MII), *Reduced Media Independent Interface* (RMII), synchronous FIFO supporting a glue-free interface to microcontrollers, and 10/100 Ethernet MAC. These interfaces and standards compliance simplify configuration of monitoring and control networks. Fast response time and an integrated temperature sensor make the MAX2982 an excellent solution for real-time control over power lines. The MAX2982 operates over the -40°C to +105°C temperature range and is available in a 128-pin, lead-free, LQFP package.

Features

- **Single-Chip Power-Line Networking Transceiver**
- **Integrated Temperature Sensor**
- **Up to 14Mbps Data Rate**
- **Low-Rate Adaptation (LORA) Operation Option Provides -2dB SNR Performance at 1Mbps**
- **4.49MHz to 20.7MHz Frequency Band**
- **Flexible MAC/PHY**
  - **Field Upgradable Firmware using TFTP**
  - **Spectral Shaping Including Bandwidth and Notching Capability**
  - **Programmable Preamble**
  - **128kB Internal SRAM**
- **Advanced Narrowband Interference Rejection Circuitry**
- **84-Carrier, OFDM-Based PHY**
  - **Automatic Channel Adaptation**
  - **FEC (Forward Error Correction)**
  - **DQPSK, DBPSK Modulation**
  - **Enhanced ROBO Mode with -1dB SNR**
- **Large Bridge Table: Up to 512 Addresses**
- **56-Bit DES Encryption with Key Management for Secure Communication**
- **On-Chip Communication Interfaces**
  - **UART**
  - **10/100 Ethernet**
  - **MII/RMII**
  - **High-Speed Synchronous FIFO**
- **HomePlug 1.0 Compliant**
- **AEC-Q100-REV-G Automotive Grade Qualification**

Applications

Industrial Automation

Motor Control

Remote Monitoring and Control

Building Automation

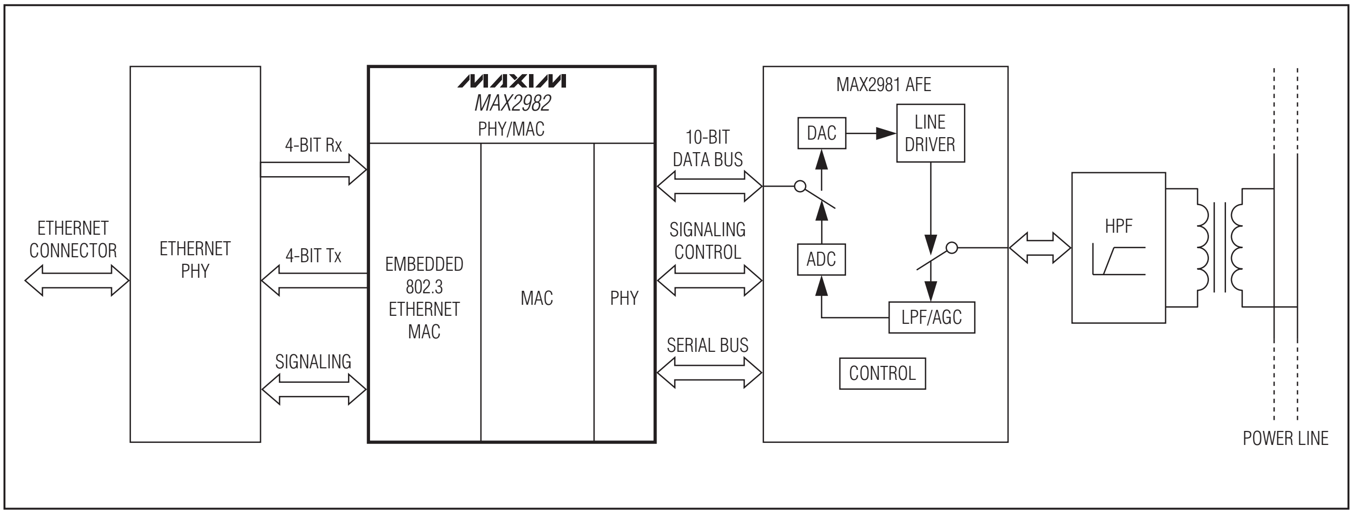
Broadband Over Shared Coax/Copper Line

***Ordering Information** appears at end of data sheet.*

Typical Application Circuit appears at end of data sheet.

*For related parts and recommended products to use with this part, refer to **www.maxim-ic.com/MAX2982.related**.*

Typical Application Circuit



ABSOLUTE MAXIMUM RATINGS

V_{DD33} to DGND ....-0.3V to +4V
V_{DD12} to DGND, DVDD to DVSS.........................-0.3V to +1.5V
AVDD to AVSS...-0.5V to +1.5V
All Other Input Pins ....-0.5V to +5.5V
All Other Output Pins ....-0.5V to +4.6V
Continuous Power Dissipation (T_A = +105°C)
LQFP (derate 25.6mW/°C above +105°C) 2045mW

Operating Temperature Range........................ -40°C to +105°C
Junction Temperature ....+125°C
Storage Temperature Range............................ -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) ....30°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....................8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS*

(V_{DD33} = +3.3V, V_{DD12} = V_{DVDD} = V_{AVDD} = +1.2V, V_{AVSS} = V_{DVSS} = V_{DGND} = 0V, T_A = -40 to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER-SUPPLY CHARACTERISTICS						
Digital Supply Voltage Range	V_{DD33}		3.0	3.3	3.6	V
Core Supply Voltage Range	V_{DD12}		1.14	1.2	1.26	V
Digital Supply Current	I_{DD33}			30		mA
Core Supply Current	I_{DD12}			365		mA
PLL Supply Current	I_{PLL}			9.5		mA
Output Voltage High	V_{OH}	UARTTXD, ETHMDC, ETHTXD[0], ETHTXD[1], ETHTXD[2], ETHTXD[3], ETHTXEN, ETHTXER, JRTCK, MIICRS, MIIRXDV, MIIRXER, I_{OH} = 4mA	2.4			V
		AFECLK, AFEFRZ, AFEPDRX, AFEREN, AFERESET, AFETXEN, I_{OH} = 8mA				
		JTDO (three-state port), I_{OH} = 4mA				
		GPIO[23:21],GPIO[18:0], I_{OH} = 5mA				
Output Voltage Low	V_{OL}	UARTTXD, ETHMDC, ETHTXD[0], ETHTXD[1], ETHTXD[2], ETHTXD[3], ETHTXEN, ETHTXER, JRTCK, MIICRS, MIIRXDV, MIIRXER, I_{OI} = 4mA			0.4	V
		AFECLK, AFEFRZ, AFEPDRX, AFEREN, AFERESET, AFETXEN, I_{OI} = 8mA				
		JTDO (three-state port), I_{OI} = 4mA				
		GPIO[23:21],GPIO[18:0], I_{OI} = 5mA				

The parametic values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

ELECTRICAL CHARACTERISTICS* (continued)

(V_{DD33} = +3.3V, V_{DD12} = V_{DVDD} = V_{AVDD} = +1.2V, V_{AVSS} = V_{DVSS} = V_{DGND} = 0V, T_A = -40 to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC-INPUT CHARACTERISTICS						
Input High Voltage	V_{IH}		2.0		5.5	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Current	I_{IH}	ETHCOL, ETHCRS, ETHRXDV, ETHRXD[0], ETHRXD[1], ETHRXD[2], ETHRXD[3], ETHRXER, JTCK, JTDI, JTMS, JTRSTN, MIIMDC, MIITXEN	-10		+10	µA
		ETHRXCLK, ETHTXCLK, MIICLK	-10		+10	
		UARTRXD, $\overline{BUFCS}$, $\overline{BUFRD}$, $\overline{BUFWR}$, $\overline{RESET}$	-10		+10	
		GPIO[23:21],GPIO[18:0]	-10		+10	
TEMPERATURE SENSOR						
Nominal Voltage				465		mV
Transfer Function				7		mV/°C
Sensor Accuracy				5		°C
Output Impedance				185		kΩ

AC TIMING CHARACTERISTICS*

(V_{DD33} = +3.3V, V_{DD12} = V_{DVDD} = V_{AVDD} = +1.2V, V_{AVSS} = V_{DVSS} = V_{DGND} = 0V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MII TIMING (See Figures 4, 5)						
MIICLK Input Clock Frequency			2.5		25	MHz
RMIICLK Input Clock Frequency			5		50	MHz
Interframe Gap	IFG	10M-bit mode			0.96	µs
		100M-bit mode			9.6	
Setup Prior to Positive Edge of MIICLK	t_{IS}		5			ns
Hold After Positive Edge of MIICLK	t_{IH}		5			ns
Data Valid After Positive Edge of MIICLK	t_{OV}				15	ns
Data Hold Time	t_{OH}		One MIICLK			period

The parametric values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.

AC TIMING CHARACTERISTICS* (continued)

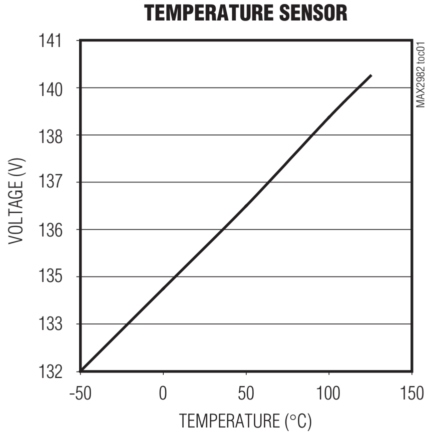
(V_{DD33} = +3.3V, V_{DD12} = V_{DVDD} = V_{AVDD} = +1.2V, V_{AVSS} = V_{DVSS} = V_{DGND} = 0V, T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.)

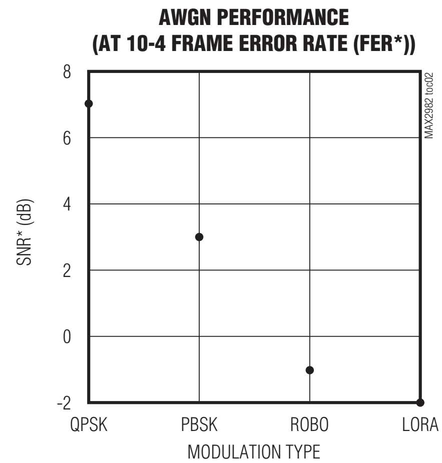
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FIFO INTERFACE TIMING (See Figures 10, 12, 13, 14)						
Input Clock Frequency			2.5	12.5	66	MHz
Setup Prior to Positive Edge of $\overline{BUFWR}$	t_{IS}	See timing diagram sync configuration	3			ns
Hold After Positive Edge of MIICLK $\overline{BUFWR}$	t_{IH}	See timing diagram sync configuration	2			ns
Data Valid After Negative Edge of $\overline{BUFRD}$	t_{OV}	See timing diagram sync configuration	10			ns
Data Valid After Positive Edge of $\overline{BUFRD}$	t_{OH}	See timing diagram sync configuration	5		10	ns
ETHERNET INTERFACE TIMING (See Figures 18, 19)						
Time Data Must be Valid	t_{TXDV}				25	ns
Time Data Must be Held	t_{TXDH}		5			ns
Setup Time Prior to the Positive Edge of ETHRXCLK	t_{RXS}		5			ns
Data Hold Time After the Positive Edge	t_{RXH}				5	ns
AFE TX TIMING (See Figure 23)						
Warm Out AFE TX Path	t_{XMT_PDRX}		1900	2300	2500	ns
Transmit Bus Switched to TX Mode and RX Path Shut Down	t_{PDRX_REN}		30	60	100	ns
Data Available on TX	t_{REN_d}		70	130	180	ns
RX Path On	t_{PDRX_XMT}		10000	12000	15000	ns
TX Data Not Valid	t_{d_REN}		5	20	50	ns
AFE RX TIMING (See Figure 24)						
Warm Out AFE RX Path	t_{PDRX_REN}		10000	12000	15000	ns
Transmit Bus Switched to TX Mode and RX Path Shut Down	t_{REN_XMT}		50	100	200	ns

**The parametic values (min, typ, max limits) shown in the Electrical Characteristics table supersede values quoted elsewhere in this data sheet.*

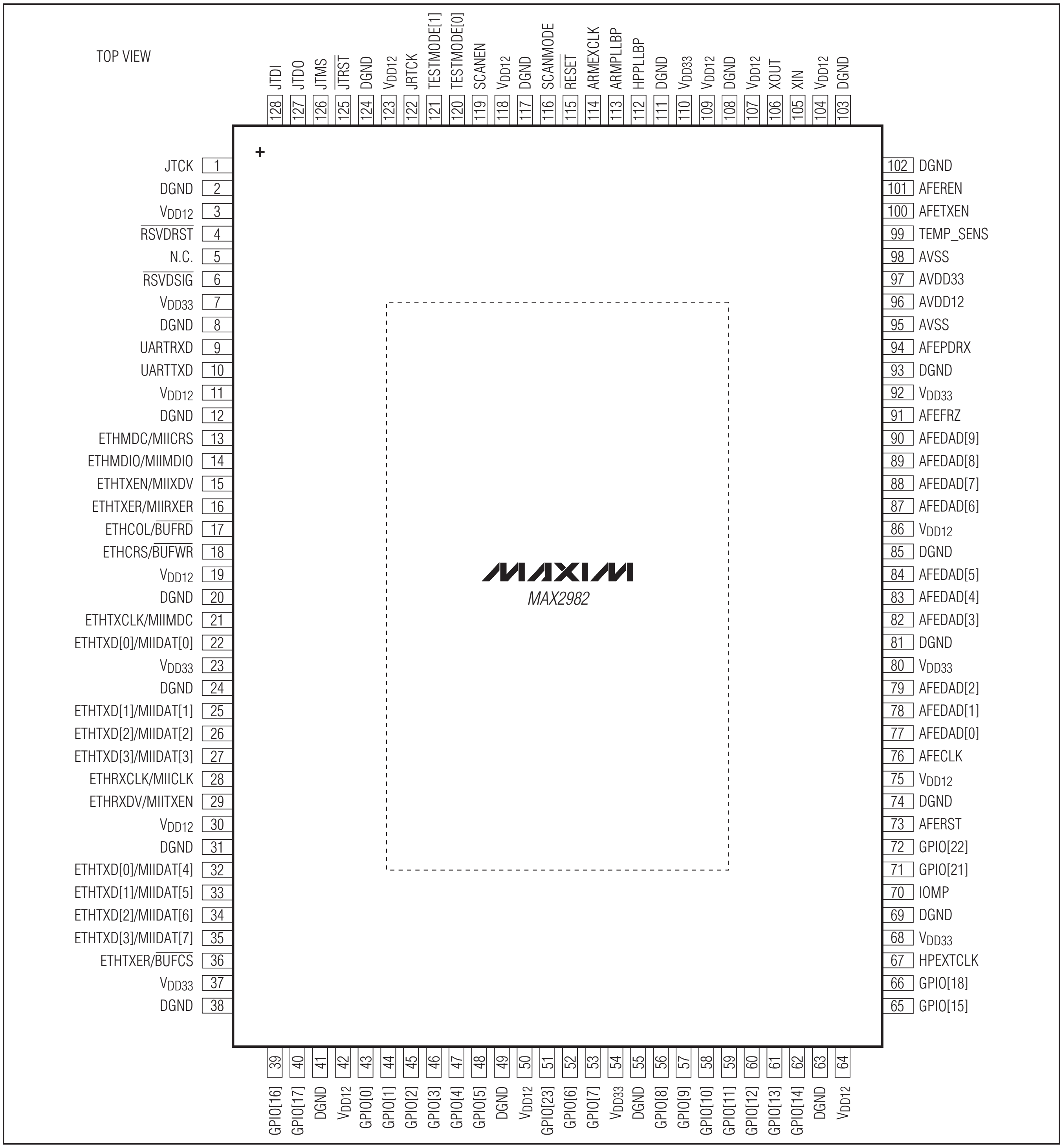
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)





Pin Configuration



Pin Description

PIN	NAME	TYPE	FUNCTION
1	JTCK	I	JTAG Clock. Connect a 10kΩ pullup resistor to V_{DD33}.
2, 8, 12, 20, 24, 31, 38, 41, 49, 55, 63, 69, 74, 81, 85, 93, 102, 103, 108, 111, 117, 124	DGND	P	Digital Ground
3, 11, 19, 30, 42, 50, 64, 75, 86, 104, 107, 109, 118	V_{DD12}	P	+1.2V Digital Power Supply. Bypass V_{DD12} to DGND with a 100nF capacitor as close as possible to device.
4	$\overline{\text{RSVDRST}}$	I	Connect to $\overline{\text{RESET}}$
5	N.C.	IPD/O	Reserved
6	$\overline{\text{RSVDSIG}}$	IPD/O	Connect to DGND
7, 23, 37, 54, 68, 80, 92, 110, 123	V_{DD33}	P	+3.3V Digital Power Supply. Bypass V_{DD33} to DGND with a 100nF capacitor as close to device as possible.
9	UARTRXD	I	UART Receive
10	UARTTXD	O	UART Transmit
13	ETHMDC/ MIICRS	O	Ethernet Management Data Interface Clock/MII/FIFO Mode MII Carrier Sense
14	ETHMDIO/ MIIMDIO	I/O	Ethernet Management Data Input/Output/MII/FIFO Mode MII Management Data
15	ETHTXEN/ MIIRXDV	O	Ethernet MII Transmit Enable/MII/FIFO Mode MII Receive Data Valid
16	ETHTXER/ MIIRXER	O	Ethernet MII Transmit Error/MII/FIFO Mode MII Receive Error Indicator
17	ETHCOL/ $\overline{\text{BUFRD}}$	I	Ethernet MII Collision/MII/FIFO Mode Active-Low FIFO Read Enable
18	ETHCRS/ $\overline{\text{BUFWR}}$	I	Ethernet MII Carrier Sense/MII/FIFO Mode Active-Low FIFO Write Enable
21	ETHTXCLK/ MIIMDC	I	Ethernet MII Transmit Clock/MII/FIFO Mode MII Management Data Clock
22	ETHTXD[0]/ MIIDAT[0]	I/O	Ethernet MII Transmit Data Bit 0/MII/FIFO Mode MII/FIFO Transmit/ Receive Data [0]
25	ETHTXD[1]/ MIIDAT[1]	I/O	Ethernet MII Transmit Data Bit 1/MII/FIFO Mode MII/FIFO Transmit/ Receive Data [1]
26	ETHTXD[2]/ MIIDAT[2]	I/O	Ethernet MII Transmit Data Bit 2/MII/FIFO Mode MII/FIFO Transmit/ Receive Data [2]
27	ETHTXD[3]/ MIIDAT[3]	I/O	Ethernet MII Transmit Data Bit 3/MII/FIFO Mode MII/FIFO Transmit/ Receive Data [3]
28	ETHRXCLK/ MIICLK	I	Ethernet MII Receive Clock/MII/FIFO Mode MIICLK
29	ETHRXDV/ MIITXEN	I	Ethernet MII Receive Data Valid/MII/FIFO Mode MII Transmit Enable.
32	ETHRXD[0]/ MIIDAT[4]	I/O	Ethernet MII Receive Data Bit 0/MII/FIFO Mode MII Transmit/Receive Data [4]

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
33	ETHRXD[1]/ MIIDAT[5]	I/O	Ethernet MII Receive Data Bit 1/MII/FIFO Mode MII/FIFO Transmit/ Receive Data [5]
34	ETHRXD[2]/ MIIDAT[6]	I/O	Ethernet MII Receive Data Bit 2/MII/FIFO Mode MII/FIFO Transmit/ Receive Data [6]
35	ETHRXD[3]/ MIIDAT[7]	I/O	Ethernet MII Receive Data Bit 3/MII/FIFO Mode MII/FIFO Transmit/ Receive Data [7]
36	ETHRXER/ $\overline{\text{BUFCS}}$	I	Ethernet MII Receive Error/MII/FIFO Mode Active-Low FIFO Chip Select
39	GPIO[16]	I/O	General-Purpose Input/Output 16. GPIO[16] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[16] if not used.
40	GPIO[17]	I/O	General-Purpose Input/Output 17. GPIO[17] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[17] if not used.
43	GPIO[0]	I/O	General-Purpose Input/Output 0. GPIO[0] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[0] if not used.
44	GPIO[1]	I/O	General-Purpose Input/Output 1. GPIO[1] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[1] if not used.
45	GPIO[2]	I/O	Reserved
46	GPIO[3]	I/O	General-Purpose Input/Output 3. GPIO[3] is used for upper layer interface bit 2 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 2kΩ pulldown resistor according to Table 14.
47	GPIO[4]	I/O	General-Purpose Input/Output 4. GPIO[4] is used for AFE interface serial clock signal (output) and upper layer interface bit 0 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 2kΩ pulldown resistor according to Table 14.
48	GPIO[5]	I/O	General-Purpose Input/Output 5. GPIO[5] is used for AFE interface serial data signal (input/output). Connect a 100kΩ pullup resistor.
51	GPIO[23]	I/O	General-Purpose Input/Output 23. GPIO[23] is used for the boot pin bit 2 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 1kΩ pulldown resistor according to Table 11.
52	GPIO [6]	I/O	General-Purpose Input/Output 6. GPIO[6] is used for AFE interface serial write signal (output) and upper layer interface bit 1 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 2kΩ pulldown resistor according to Table 14.
53	GPIO[7]	I/O	General-Purpose Input/Output 7. GPIO[7] is used for AFE interface power-down signal. Connect a 2kΩ pullup resistor.
56	GPIO[8]	I/O	General-Purpose Input/Output 8. GPIO[8] is used for nonvolatile memory serial clock signal (output). Connect a 10kΩ pullup resistor to V_{DD33}.
57	GPIO[9]	I/O	General-Purpose Input/Output 9. GPIO[9] is used for serial data in nonvolatile memory interface.

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
58	GPIO[10]	I/O	General-Purpose Input/Output 10. GPIO[10] is used for nonvolatile memory chip select signal (output). Connect a 10kΩ pullup resistor.
59	GPIO[11]	I/O	General-Purpose Input/Output 11. GPIO[11] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[11] .
60	GPIO[12]	I/O	General-Purpose Input/Output 12. GPIO[12] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[12].
61	GPIO[13]	I/O	General-Purpose Input/Output 13. GPIO[13] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[13].
62	GPIO[14]	I/O	General-Purpose Input/Output 14. GPIO[14] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[14].
65	GPIO[15]	I/O	General-Purpose Input/Output 15. GPIO[15] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[15].
66	GPIO[18]	I/O	General-Purpose Input/Output 18. GPIO[18] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[18].
67	HPEXTCLK	I	HP External Clock. Connect to DGND.
70	IOMAP	I	Connect IOMAP to DGND
71	GPIO[21]	I/O	General-Purpose Input/Output 21. GPIO[21] is used for AFE interface collision LED (output) and boot pin bit 0 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 1kΩ pulldown resistor according to Table 11.
72	GPIO[22]	I/O	General-Purpose Input/Output 22. GPIO[22] is used for AFE interface link status activity LED (output) and boot pin bit 1 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 1kΩ pulldown resistor according to Table 11.
73	AFERESET	O	AFE Reset. Connect a 10kΩ pulldown resistor.
76	AFECLK	O	50MHz AFE Clock
77	AFEDAD[0]	I/O	Analog Front-End DAC/ADC Input/Output 0 Interface
78	AFEDAD[1]	I/O	Analog Front-End DAC/ADC Input/Output 1 Interface
79	AFEDAD[2]	I/O	Analog Front-End DAC/ADC Input/Output 2 Interface
82	AFEDAD[3]	I/O	Analog Front-End DAC/ADC Input/Output 3 Interface
83	AFEDAD[4]	I/O	Analog Front-End DAC/ADC Input/Output 4 Interface
84	AFEDAD[5]	I/O	Analog Front-End DAC/ADC Input/Output 5 Interface
87	AFEDAD[6]	I/O	Analog Front-End DAC/ADC Input/Output 6 Interface
88	AFEDAD[7]	I/O	Analog Front-End DAC/ADC Input/Output 7 Interface
89	AFEDAD[8]	I/O	Analog Front-End DAC/ADC Input/Output 8 Interface
90	AFEDAD[9]	I/O	Analog Front-End DAC/ADC Input/Output 9 Interface
91	AFEFRZ	O	Analog Front-End Carrier Sense Indicator. Connect a 10kΩ pulldown resistor.
94	AFEPDRX	O	AFE Receiver Power-Down. Connect a 100kΩ pulldown resistor.

Pin Description (continued)

PIN	NAME	TYPE	FUNCTION
95, 98	AVSS	P	Analog Ground
96	AVDD12		+1.2V Analog Power Supply
97	AVDD33	P	+3.3V Analog Power Supply
99	TEMP_SENS	OA	Analog Temperature Output
100	AFETXEN	O	Analog Front-End Transmitter Enable Output
101	AFEREN	O	Analog Front-End Read Enable Output
105	XIN	I	Crystal Input (30MHz)
106	XOUT	O	Crystal Output
112	HPPLLBP	I	DSP PLL Bypass. Connect HPPLLBP to DGND.
113	ARMPLLBP	I	ARM PLL Bypass. Connect ARMPLLBP to DGND.
114	ARMEXCLK	I	ARM External Clock. Connect ARMEXCLK to DGND.
115	$\overline{\text{RESET}}$	I	Asynchronous Active-Low Reset Input. $\overline{\text{RESET}}$ pulse is at least 1µs long during power-on reset.
116	SCANMODE	I	Scan Mode. Connect SCANMODE to DGND.
119	SCANEN	I	Scan Enable. Connect SCANEN to DGND.
120	TESTMODE[0]	I	Test Mode 0. Connect TESTMODE[0] to DGND.
121	TESTMODE[1]	I	Test Mode 1. Connect TESTMODE[1] to DGND.
122	JRTCK	O	JTAG Return Clock
125	$\overline{\text{JTRST}}$	IPU	Active-Low JTAG Reset. Internal pullup resistance 83kΩ. On power-on, pin must be asserted for 1µs with chip reset ($\overline{\text{RESET}}$).
126	JTMS	IPU	JTAG Mode Select. Internal pullup resistance 83kΩ.
127	JTDO	O	JTAG Data Output
128	JTDI	IPU	JTAG Test Data Input. Internal pullup resistance 83kΩ.

Pin Description by Function

CONTACT	NAME	TYPE	FUNCTION
POWER SUPPLY			
7, 23, 37, 54, 68, 80, 92, 110, 123	V_{DD33}	P	+3.3V Digital Power Supply. Bypass V_{DD33} to DGND with a 100nF capacitor as close to device as possible.
3, 11, 19, 30, 42, 50, 64, 75, 86, 104, 107, 109, 118	V_{DD12}	P	+1.2V Digital Power Supply. Bypass V_{DD12} to DGND with a 100nF capacitor as close to device as possible.
2, 8, 12, 20, 24, 31, 38, 41, 49, 55, 63, 69, 74, 81, 85, 93, 102, 103, 108, 111, 117, 124	DGND	P	Digital Ground
95, 98	AVSS	P	Analog Ground
97	AVDD33	P	+3.3V Analog Power Supply
96	AVDD12		+1.2V Analog Power Supply

Pin Description by Function (continued)

CONTACT	NAME	TYPE	FUNCTION
ANALOG FRONT-END INTERFACE			
76	AFECLK	O	50MHz AFE Clock
91	AFEFRZ	O	Analog Front-End Carrier Sense Indicator. Connect a 10kΩ pulldown resistor.
94	AFEPDRX	O	AFE Receiver Power-Down. Connect a 100kΩ pulldown resistor.
101	AFEREN	O	Analog Front-End Read Enable Output
73	AFERESET	O	AFE Reset. Connect a 10kΩ pulldown resistor.
100	AFETXEN	O	Analog Front-End Transmitter Enable Output
77	AFEDAD[0]	I/O	Analog Front-End DAC/ADC Input/Output 0 Interface
78	AFEDAD[1]	I/O	Analog Front-End DAC/ADC Input/Output 1 Interface
79	AFEDAD[2]	I/O	Analog Front-End DAC/ADC Input/Output 2 Interface
82	AFEDAD[3]	I/O	Analog Front-End DAC/ADC Input/Output 3 Interface
83	AFEDAD[4]	I/O	Analog Front-End DAC/ADC Input/Output 4 Interface
84	AFEDAD[5]	I/O	Analog Front-End DAC/ADC Input/Output 5 Interface
87	AFEDAD[6]	I/O	Analog Front-End DAC/ADC Input/Output 6 Interface
88	AFEDAD[7]	I/O	Analog Front-End DAC/ADC Input/Output 7 Interface
89	AFEDAD[8]	I/O	Analog Front-End DAC/ADC Input/Output 8 Interface
90	AFEDAD[9]	I/O	Analog Front-End DAC/ADC Input/Output 9 Interface
GENERAL-PURPOSE I/O			
43	GPIO[0]	I/O	General-Purpose Input/Output 0. GPIO[0] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[0] if not used.
44	GPIO[1]	I/O	General-Purpose Input/Output 1. GPIO[1] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[1] if not used.
45	GPIO[2]	I/O	General-Purpose Input/Output 2. Reserved.
46	GPIO[3]	I/O	General-Purpose Input/Output 3. GPIO[3] is used for upper layer interface bit 2 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 2kΩ pulldown resistor according to Table 14.
47	GPIO[4]	I/O	General-Purpose Input/Output 4. GPIO[4] is used for AFE interface serial clock signal (output) and upper layer interface bit 0 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 2kΩ pulldown resistor according to Table 14.
48	GPIO[5]	I/O	General-Purpose Input/Output 5. GPIO[5] is used for AFE interface serial data signal (input/output). Connect a 100kΩ pulldown resistor.
52	GPIO [6]	I/O	General-Purpose Input/Output 6 GPIO[6] is used for AFE interface serial write signal (output) and upper layer interface bit 1 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 2kΩ pulldown resistor according to Table 14.
53	GPIO[7]	I/O	General-Purpose Input/Output 7. GPIO[7] is used for AFE interface power-down signal. Connect a 2kΩ pulldown resistor.
56	GPIO[8]	I/O	General-Purpose Input/Output 8. GPIO[8] is used for nonvolatile memory serial clock signal (output). Connect a 10kΩ pulldown resistor to V_{DD33}.
57	GPIO[9]	I/O	General-Purpose Input/Output 9. GPIO[9] is used for serial data in nonvolatile memory interface.

Pin Description by Function (continued)

CONTACT	NAME	TYPE	FUNCTION
58	GPIO[10]	I/O	General-Purpose Input/Output 10. GPIO[10] is used for nonvolatile memory chip select signal (output). Connect a 10kΩ pullup resistor.
59	GPIO[11]	I/O	General-Purpose Input/Output 11. GPIO[11] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[11].
60	GPIO[12]	I/O	General-Purpose Input/Output 12. GPIO[12] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[12].
61	GPIO[13]	I/O	General-Purpose Input/Output 13. GPIO[13] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[13].
62	GPIO[14]	I/O	General-Purpose Input/Output 14. GPIO[14] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[14].
65	GPIO[15]	I/O	General-Purpose Input/Output 15. GPIO[15] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[15].
39	GPIO[16]	I/O	General-Purpose Input/Output 16. GPIO[16] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[16] if not used.
40	GPIO[17]	I/O	General-Purpose Input/Output 17. GPIO[17] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[17] if not used.
66	GPIO[18]	I/O	General-Purpose Input/Output 18. GPIO[18] is in three-state during boot-up. Connect a 100kΩ pullup or pulldown resistor to GPIO[18].
71	GPIO[21]	I/O	General-Purpose Input/Output 21. GPIO[21] is used for AFE interface collision LED (output) and boot pin bit 0 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 1kΩ pulldown resistor according to Table 11.
72	GPIO[22]	I/O	General-Purpose Input/Output 22. GPIO[22] is used for AFE interface link status activity LED (output) and boot pin bit 1 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 1kΩ pulldown resistor according to Table 11.
51	GPIO[23]	I/O	General-Purpose Input/Output 23. GPIO[23] is used for the boot pin bit 2 (input). Connect a 10kΩ pullup resistor to V_{DD33} or a 1kΩ pulldown resistor according to Table 11.
SHARED UPPER-LAYER INTERFACE			
22	ETHTXD[0]/ MIIDAT[0]	I/O	Ethernet MII Transmit Data Bit 0/MII/FIFO Mode MII/FIFO Transmit/Receive Data [0]
25	ETHTXD[1]/ MIIDAT[1]	I/O	Ethernet MII Transmit Data Bit 1/MII/FIFO Mode MII/FIFO Transmit/Receive Data [1]
26	ETHTXD[2]/ MIIDAT[2]	I/O	Ethernet MII Transmit Data Bit 2/MII/FIFO Mode MII/FIFO Transmit/Receive Data [2]
27	ETHTXD[3]/ MIIDAT[3]	I/O	Ethernet MII Transmit Data Bit 3/MII/FIFO Mode MII/FIFO Transmit/Receive Data [3]
32	ETHRXD[0]/ MIIDAT[4]	I/O	Ethernet MII Receive Data Bit 0/MII/FIFO Mode MII Transmit/Receive Data [4]
33	ETHRXD[1]/ MIIDAT[5]	I/O	Ethernet MII Receive Data Bit 1/MII/FIFO Mode MII/FIFO Transmit/Receive Data [5]
34	ETHRXD[2]/ MIIDAT[6]	I/O	Ethernet MII Receive Data Bit 2/MII/FIFO Mode MII/FIFO Transmit/Receive Data [6]

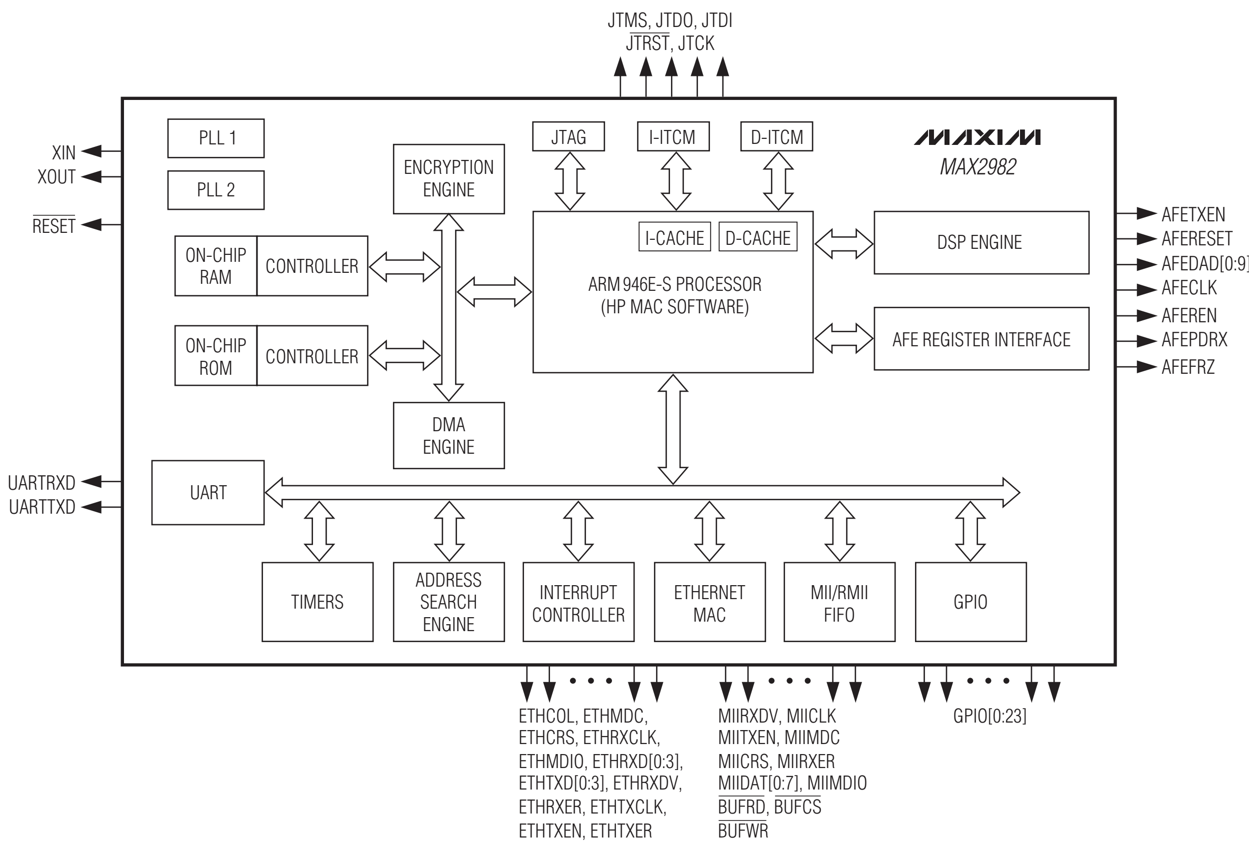
Pin Description by Function (continued)

CONTACT	NAME	TYPE	FUNCTION
35	ETHRXD[3]/ MIIDAT[7]	I/O	Ethernet MII Receive Data Bit 3 / MII/FIFO Mode MII/FIFO Transmit/Receive Data [7]
21	ETHTXCLK/ MIIMDC	I	Ethernet MII Transmit Clock or MII Management Data Clock in MII/FIFO Mode
13	ETHMDC/ MIICRS	O	Ethernet Management Data Interface Clock/MII/FIFO Mode MII Carrier Sense
28	ETHRXCLK/ MIICLK	I	Ethernet MII Receive Clock/MII/FIFO Mode MIICLK
29	ETHRXDV/ MIITXEN	I	Ethernet MII Receive Data Valid/MII/FIFO Mode MII Transmit Enable
15	ETHTXEN/ MIIRXDV	O	Ethernet MII Transmit Enable/MII/FIFO Mode MII Receive Data Valid
17	ETHCOL/ $\overline{\text{BUFRD}}$	I	Ethernet MII Collision/MII/FIFO Mode Active-Low FIFO Read Enable
18	ETHCRS/ $\overline{\text{BUFWR}}$	I	Ethernet MII Carrier Sense/MII/FIFO Mode Active-Low FIFO Write Enable
14	ETHMDIO/ MIIMDIO	I/O	Ethernet Management Data Input/Output/MII/FIFO Mode MII Management Data
36	ETHRXER/ $\overline{\text{BUFCS}}$	I	Ethernet MII Receive Error/MII/FIFO Mode Active-Low FIFO Chip Select
16	ETHTXER/ MIIRXER	O	Ethernet MII Transmit Error/MII/FIFO Mode MII Receive Error Indicator
UART INTERFACE			
10	UARTTXD	O	UART Transmit
9	UARTRXD	I	UART Receive
CRYSTAL OSCILLATOR			
105	XIN	I	Crystal Input (30MHz)
106	XOUT	O	Crystal Output
TEST PINS			
115	$\overline{\text{RESET}}$	I	Asynchronous Active-Low Reset Input. $\overline{\text{RESET}}$ pulse is at least 1µs long during power-on reset. On power-on, pin must be asserted for 1µs with chip reset ($\overline{\text{RESET}}$).
126	JTMS	IPU	JTAG Mode Select. Internal pullup resistance 83kΩ.
128	JTDI	IPU	JTAG Test Data Input. Internal pullup resistance 83kΩ.
122	JRTCK	O	JTAG Return Test Clock
127	JTDO	O	JTAG Data Output
125	$\overline{\text{JTRST}}$	IPU	Active-Low JTAG Reset. Internal pullup resistance 83kΩ.

Pin Description by Function (continued)

CONTACT	NAME	TYPE	FUNCTION
1	JTCK	I	JTAG Clock. Connect a 10kΩ pullup resistor to V_{DD33}.
70	IOMAP	I	Connect IOMAP to DGND
99	TEMP_SENS	OA	Analog Temperature Output
67	HPEXTCLK	I	HP External Clock. Connect to DGND.
112	HPPLLBP	I	DSP PLL Bypass. Connect HPPLLBP to DGND.
114	ARMEXCLK	I	ARM External Clock. Connect ARMEXCLK to DGND.
113	ARMPLLBP	I	ARM PLL Bypass. Connect ARMPLLBP to DGND.
116	SCANMODE	I	Scan Mode. Connect SCANMODE to DGND.
119	SCANEN	I	Scan Enable. Connect SCANEN to DGND.
120	TESTMODE[0]	I	Test Mode 0. Connect TESTMODE[0] to DGND.
121	TESTMODE[1]	I	Test Mode 1. Connect TESTMODE[1] to DGND.

Functional Diagram



Detailed Description

The MAX2982 power-line transceiver device is a state-of-the-art CMOS device with high performance and extended operating temperature range to deliver reliable communications in industrial applications. This highly integrated design combines the MAC with the PHY layer in a single device. The MAX2982, with the MAX2981 analog front-end, forms a complete HomePlug 1.0-compliant solution with a substantially reduced system bill of materials.

MII/RMII/FIFO Interface

The MII/RMII/FIFO block is the data and control interface layer of the MAX2982 transceiver. This layer is designed to operate with IEEE 802.3 standard MII/RMII or other devices using the FIFO interface. Refer to the MAX2982 programming reference manual for information on initialization and control of the HomePlug 1.0 MAC through the MII/RMII/FIFO interface. The interface signals connecting to the external host are shown in Figure 1.

The interface is a data channel that transfers data in packets whose flow is controlled by the carrier-sense (MIICRS) signal. The MIICRS signal controls the half-duplex transmission between the external host and the HomePlug MAC. While a frame reception is in progress (MIICRS and MIIRXDV are high), the external host must wait until the completion of reception and the deassertion of MIICRS before starting a transmission. When sending two consecutive frames, the minimum time the external host needs to wait is the one-frame transfer time plus an interframe gap (IFG).

The MII signals MIICOL and MIITXER are not used, as the power-line networking device is able to detect and manage all transmission failures. The signals MIITXCLK and MIIRXCLK have the same source and are referred to as MIICLK in this data sheet.

In MII mode, the data is transferred synchronously with a 2.5MHz/25MHz clock. Data transmission in MII is in nibble format so the data transmission rate is 10Mbps/100Mbps.

In RMII mode, the data is transferred synchronously with a 5/50MHz clock. Data transmission in RMII is in di-bit (two-bit) format so the data transmission rate is 10Mbps/100Mbps.

In FIFO mode, data is read and written in byte format on each positive edge of BUFRDN and BUFWRN. The only limitation in this mode is that BUFRDN and BUFWRN must be low for at least three pulses of MIICLK to be considered a valid signal.

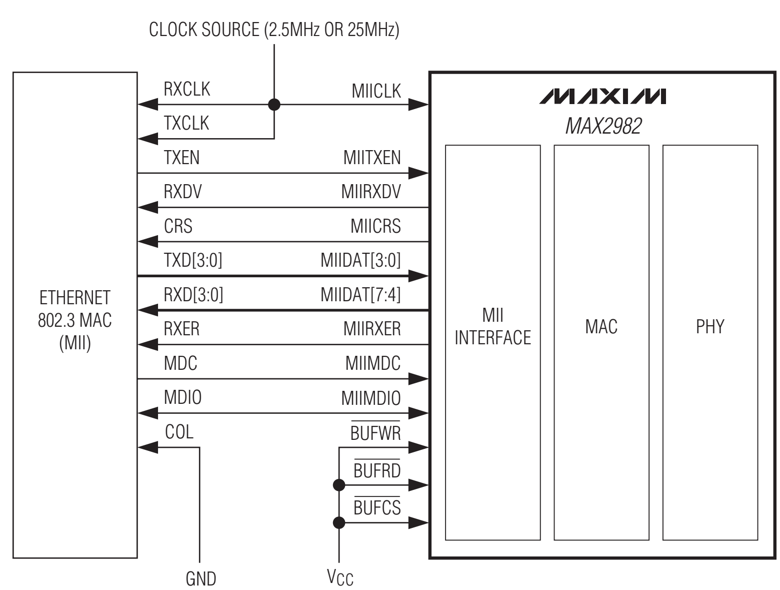


Figure 1. Ethernet MAC and MAX2982 Connection in MII Mode

The upper layer interface can be selected according to the settings shown in Table 1.

MII Interface Signals

Table 2 describes the signals that provide data, status, and control to and from the MAX2982 in MII mode.

MII MAC and PHY Connections

Figure 1 illustrates the connections between Ethernet/MAC and MAX2982 in MII mode. Although the TX and RX data paths are full duplex, the MII interface operates in half-duplex mode. MIIRXDV is never asserted at the same time as MIITXEN.

On transmit, the MAX2982 asserts MIICRS some time after MIITXEN is asserted, and drops MIICRS after MIITXEN is deasserted and the MAX2982 is ready to receive another packet. When MIICRS falls, the MAC times out an interframe gap (IFG) and asserts MIITXEN again when there is another packet to send. This differs from nominal behavior of MIICRS in that MIICRS can extend past the end of the packet by an arbitrary amount of time, while the MAX2982 is gaining access to the channel and transmitting the packet.

MACs in 10Mbps mode do not use a jabber timeout, so there is no timing restriction on how long MIICRS can assert other than timeouts (IFG) the MAX2982 implements.

Table 1. Upper Layer Interface Selection GPIO Settings

INTERFACE	GPIO[3] (UL2)	GPIO[6] (AWR_UL1)	GPIO[4] ASCL_UL0
MII	0	0	1
RMII	0	1	0
FIFO	0	1	1

Table 2. MII Signal Description

NAME	LINES	I/O	DESCRIPTION
MIIDAT[3:0]	4	I	**Transmit Data.** Data are transferred to MAX2982 from the external MAC across these four lines, one nibble at a time, synchronous to MIICLK.
MIITXEN	1	I	**Transmit Enable.** Provides the framing for the Ethernet packet from the Ethernet MAC. This signal indicates to the MAX2982 that valid data is present on MIIDAT[3:0] and must be sampled using MIICLK.
MIICRS	1	O	**Carrier Sense.** Logic-high indicates to the external host that traffic is present on the power line and the host must wait until the signal goes invalid before sending additional data. When a packet is being transmitted, MIICRS is held high.
MIIDAT[7:4]	4	O	**Receive Data.** Data are transferred from MAX2982 to the external MAC across these four lines, one nibble at a time, synchronous to MIICLK. The MAX2982 properly formats the frame such that the Ethernet MAC is presented with expected preamble plus Start Frame Delimiter (SFD).
MIIRXDV	1	O	**Receive Data Valid.** Logic-high indicates that the incoming data on the MIIDAT inputs are valid.
MIIRXER	1	O	**Receive Error.** Logic-high indicates to the external MAC that the MAX2982 detected a decoding error in the receive stream.
MIICLK	1	I	**Reference Clock.** A 2.5MHz clock in 10Mbps as a reference clock. A 25MHz clock in 100Mbps as a reference clock.
MANAGEMENT DATA UNIT			
MIIMDC	1	I	**Management Data Clock.** A 2.5MHz noncontinuous clock reference for the MIIMDIO signal.
MIIMDIO	1	I/O	**Management Data Input/Output.** A bidirectional signal that carries the data for the management data Interface.

Transmissions can "cut through" or begin to be modulated onto the wire as soon as the transfer begins when the MII fills the MAX2982 buffer faster than data needs to be made available to the modulator. When a packet arrives at MAX2982, the device attempts to gain access to the channel. This may not happen before the entire packet is transferred across the MII interface, so the MAX2982 buffers at least one Ethernet packet to perform this rate adaptation.

On receive, when the MAX2982 anticipates a packet to be demodulated, the device raises MIICRS to seize the half-duplex MII channel, waits one interframe gap time (IFG), then defers to MIITXEN when MIITXEN has been asserted plus an IFG. The device raises MIIRXDV to transfer the packet. At the end of the transfer, the MAX2982 drops MIICRS unless the transmit buffer is full or there is another receive packet ready to transfer. Figure 2 illustrates how one receive transfer is followed by a second, when the device defers to MIITXEN. Data reception maintains priority over transmission to ensure that the buffer empties faster than packets arrive off the wire. The longest that the receiver needs to wait is the time to transfer one TX frame plus an IFG or approximately 134µs. However, minimum size frames can arrive at a peak rate of one every 65µs, so the receive side buffer must accommodate multiple frames (but only a little more than one Ethernet packet of data).

Transmitting

When a frame in the external host is ready to transmit and MIICRS is not high (the previous transmission has finished), the external host asserts MIITXEN, while data is ready on MIIDAT[3:0]. In response, the MAX2982 asserts MIICRS.While the external host keeps MIITXEN high, data is sampled synchronously with respect to MIICLK into the MAX2982 through MIIDAT. After transmission of the last byte of data and before the next positive edge of the MIICLK, MIITXEN is reset by the external host.

The transmission timing of the MII interface is illustrated in Figure 3, with details in Figure 4 and Table 3.

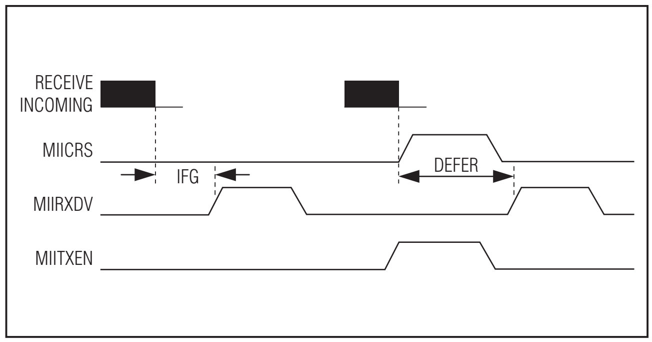


Figure 2. Receive Defer in MII Mode

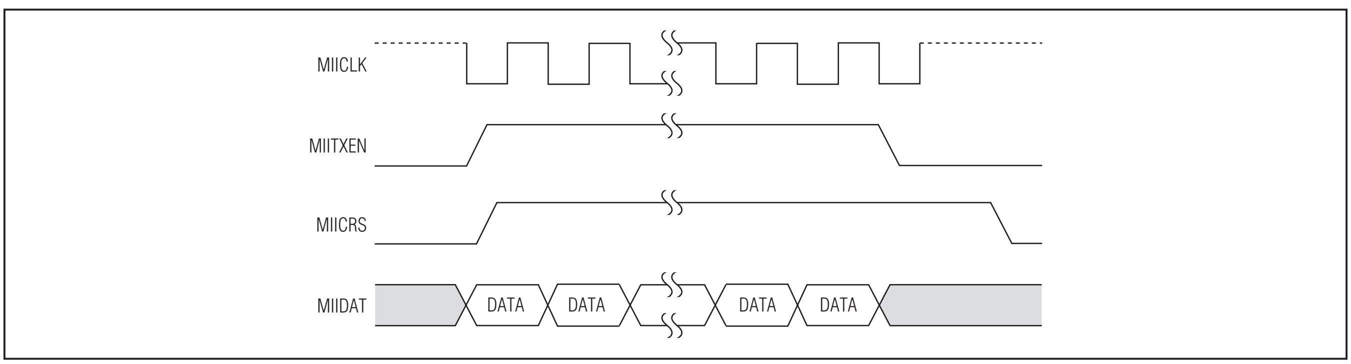


Figure 3. Transmission Behavior of the MII Interface

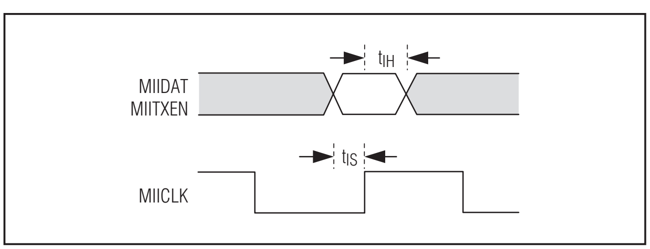


Figure 4. MII Interface Detailed Transmit Timing

Table 3. MII Interface Detailed Transmit Timing

PARAMETER	DESCRIPTION	MIN	UNITS
t_{IS}	Setup prior to positive edge of MIICLK	2.5	ns
t_{IH}	Hold after positive edge of MIICLK	2.5	ns

Receiving

When a frame is ready to send from the MAX2982 to the external host, the MAX2982 asserts MIIRXDV after IFG, while there is no transmission session in progress with respect to MIICRS.

Note: The receive process cannot start while a transmission is in progress.

While the MAX2982 keeps MIIRXDV high, data is sampled synchronously with respect to MIICLK from MAX2982 through MIIDAT. After the last byte of data is received, the MAX2982 resets MIIRXDV.

Receive timing of the MII interface is illustrated in Figure 5, with details in Figure 6 and Table 4.

Reduced Media Independent Interface (RMII)

Table 5 describes the signals that provide data, status, and control to the MAX2982 in RMII mode. In this mode, data is transmitted and received in bit pairs. The RMII mode connections are shown in Figure 7.

In case of an error in the received data, to eliminate the requirement for MIIRXER and still meet the requirement for undetected error rate, MIIDAT[5:4] replaces the decoded data in the receive stream with "10" until the end of carrier activity. By this replacement, the CRC check is guaranteed to reject the packet as being in error.

RMII Signal Timing

RMII transmit and receive timing are the same as for MII, except that the data are sent and received in di-bit format and MIICRS is removed.

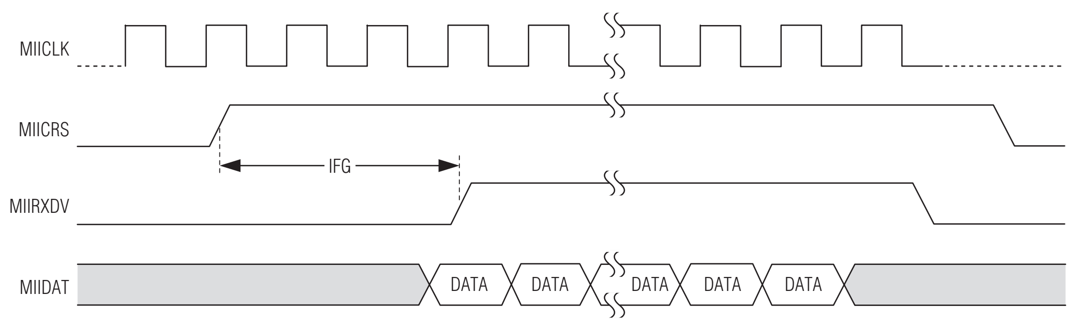


Figure 5. Receive Behavior of the MII Interface

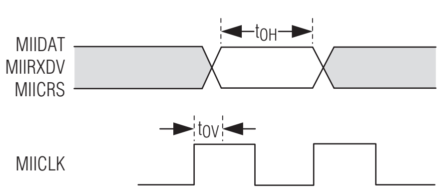


Figure 6. MII Interface Detailed Receive Timing

Table 4. MII Interface Detailed Receive Timing

PARAMETER	DESCRIPTION	MAX	UNITS
t_{OV}	Data valid after positive edge of MIICLK	2.5	ns
t_{OH}	Nominal data hold time	One MIICLK period	ns

Table 5. RMII Signal Description

NAME	DATA LINES	I/O	DESCRIPTION
MIIDAT[1:0]	2	I	**Transmit Data.** Data are transferred to the interface from the external MAC across these two lines, one di-bit at a time. MIIDAT[1:0] shall be "00" to indicate idle when MIITXEN is deasserted.

Table 5. RMII Signal Description (continued)

NAME	DATA LINES	I/O	DESCRIPTION
MIITXEN	1	I	**Transmit Enable.** This signal indicates to the MAX2982 that valid data is present on the MIIDAT I/Os. MIITXEN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented to the RMII.
MIIDAT[5:4]	2	O	**MII Receive Data.** Data is transferred from the MAX2982 to the external MAC across these two lines, one di-bit at a time. Upon assertion of MIIRXDV, the MAX2982 ensures that MIIDAT[5:4] = 00 until proper receive decoding takes place.
MIIRXDV	1	O	**Receive Data Valid (CRS_DV).** When asserted high, indicates that the incoming data on the MIIDAT inputs are valid.
MIICLK	1	I	**RMII Reference Clock.** A continuous clock that provides the timing reference for MIIRXDV, MIIDAT, MIITXEN, and MIIRXER. MIICLK is sourced by the Ethernet MAC or an external source and its frequency is 5MHz in 10Mbps data rate and 50MHz in 100Mbps data rate.
MANAGEMENT DATA UNIT			
MIIMDC	1	I	**MII Management Data Clock.** A 2.5MHz noncontinuous clock reference for the MIIMDIO signal.
MIIMDIO	1	I/O	**MII Management Data Input/Output.** It is a bidirectional signal that carries the data for the management data interface.

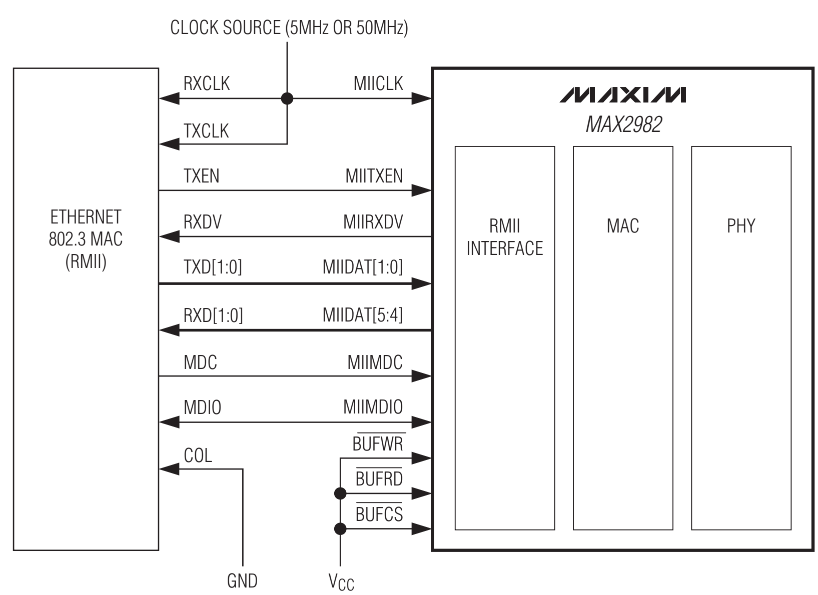


Figure 7. MAC-PHY Connection in RMII Mode

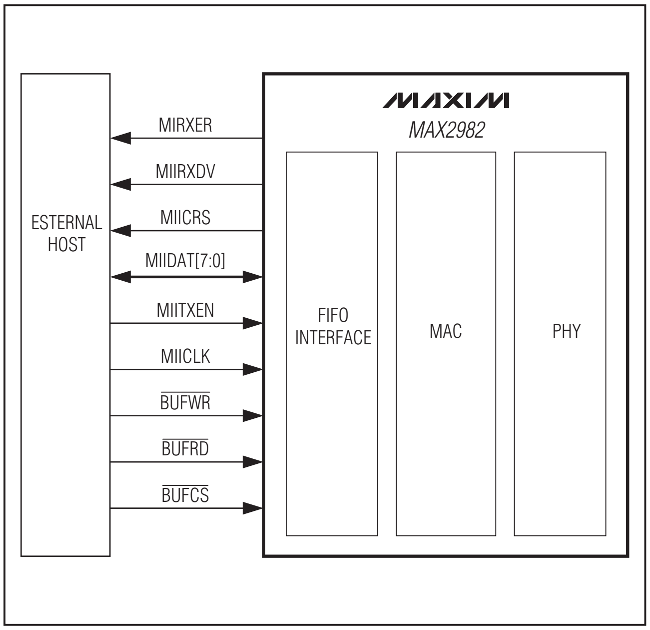


Figure 8. External Host and MAX2982 Connection in FIFO mode

FIFO Interface Signals

The buffering FIFO interface supports synchronous operation and can be interfaced gluelessly to an external microprocessor memory bus. The interface is clocked by the external processor on the MIICLK pin.

The read and write pulse width is three MIICLK cycles.

The signals that provide data, status, and control to and from the MAX2982 are shown in Table 6. MIIRXDV should never be asserted at the same time as MIITXEN`, but the device is able to start transmission while receive is in progress. The MAX2982 gives higher priority to TX packets from the external host to avoid data loss.

On transmit, the MAX2982 asserts MIICRS after MIITXEN is asserted by the host. The host should not assert MIITXEN if MIICRS is already high. After MIITXEN is deasserted by the host, which means that the host has completed data transmission, MIICRS goes low when the MAX2982 is ready to receive another packet. When MIICRS falls, MIITXEN can be held low if there is another packet to send.

Table 6. FIFO Signal Description

NAME	DATA LINES	I/O	DESCRIPTION
MIIDAT_IN/OUT[7:0]	8	I/O	**Transmit/Receive Data.** Data are transferred to/from the MAX2982 from/to the external MAC across this bidirectional port, one byte at a time.
MIITXEN	1	I	**Transmit Enable [Active-High].** This signal indicates to the MAX2982 that the transmission has started, and that data on MIIDAT should be sampled using BUFWRN. MIITXEN remains high to the end of the session.
MIICRS	1	O	**Transmit In Progress [Active-High].** When asserted high, indicates to the external host that outgoing traffic is present on the power line and the host should wait until the signal goes low before sending additional data.
$\overline{\text{BUFWR}}$	1	I	**Write [Active-Low].** Inputs a write signal to the MAX2982 from the external MAC, writing the present data on MIIDAT I/Os into the interface buffer on each positive edge.
MIIRXDV	1	O	**Receive Data Valid [Active-High].** When asserted high, indicates that the incoming data on the MIIDAT I/Os are valid.
MIIRXER	1	O	**Receive Error [Active High].** When asserted high, indicates to the external MAC that an error has occurred during the frame reception.
$\overline{\text{BUFRD}}$	1	I	**Read [Active-Low].** Inputs a read signal to the MAX2982 from the external MAC, reading the data from the MIIDAT I/Os of the MAX2982 on each positive edge.
$\overline{\text{BUFCS}}$	1	I	**Chip Select [Active-Low].** When asserted low, it enables the device. When it is high, all inputs/outputs are in high-Z including MIIData 0.7
MIICLK	1	I	**Reference Clock.** Used for sampling $\overline{\text{BUFWR}}$ and $\overline{\text{BUFRDN}}$. MIICLK speed must allow 100Mbps data rate. MIICLK is either 25MHz or 66MHz.

Transmissions can "cut through" or begin to be modulated onto the wire as soon as the transfer begins, as the interface fills the MAX2982 buffer faster than data needs to be made available to the modulator. When a packet arrives at the MAX2982, the device attempts to gain access to the channel. Since this may not happen before the entire packet is transferred across the interface, the MAX2982 FIFO features a 2Kbyte TX buffer to hold packets to perform this rate adaptation.

On receive, when the MAX2982 anticipates a packet to be demodulated, the device raises MIIRXDV to identify the upper layer that a packet is ready to transmit. MIIRXDV drops when the last byte is transmitted. Receive direction transfers maintain priority over the transmit direction to ensure that the buffer empties faster than packets arrive off the wire. The longest that the receiver needs to wait is the time to transfer one TX frame plus an IFG.

Transmitting

When the external host is ready to transmit a frame and MIICRS is not high (the previous transmission is finished), it asserts MIITXEN. The external host must assert MIITXEN if MIIRXDV is not high to avoid data loss. In response, the MAX2982 asserts MIICRS. While the external host keeps MIITXEN high, one byte of data is transmitted into the MAX2982 through MIIDAT_IN for each positive edge of $\overline{\text{BUFWR}}$. After transmission of the last byte of data, the external host resets MIITXEN. Figure 9 shows the interactions between the external host and the MAX2982. There are two GPIOs indicating packet loss and completion of a packet transmission controlled by software. The host can use these signals to determine packet retransmission much faster than through TCP or a packet-based scheme. The $\overline{\text{BUFWR}}$ clock rate is 16MHz maximum at MIICLK of 66MHz.

Figure 10 shows the overall transmission timing of the FIFO interface.

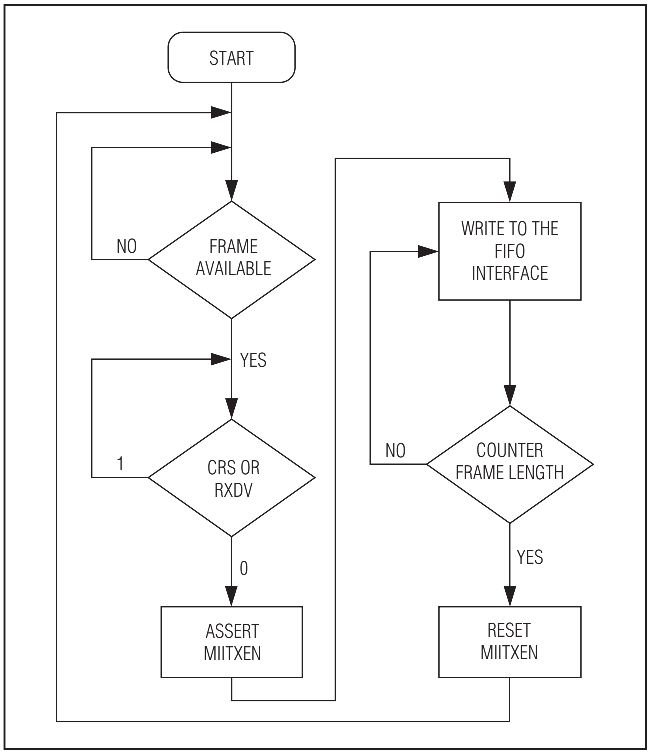


Figure 9. Buffering FIFO Transmission Process from External Host

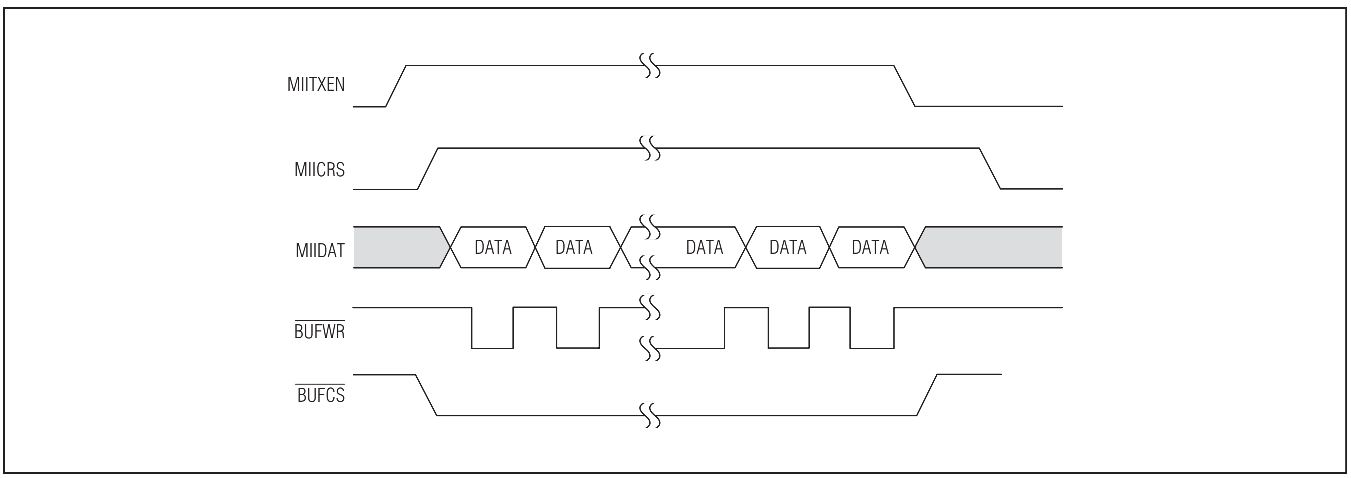


Figure 10. Transmission Timing of the Buffering (FIFO) Interface

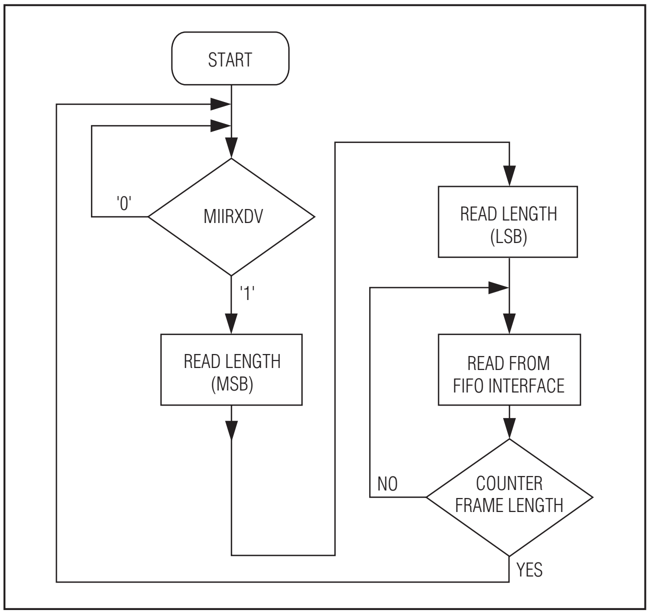


Figure 11. Buffering FIFO Interface Receive Process from the External Host View

Receiving

When the MAX2982 is ready to send a frame to the external host, the MAX2982 asserts MIIRXDV after an IFG when there is no transmission session in progress with respect to MIICRS. A receive process cannot start while a transmission is under progress. The FIFO features a 2Kb RX buffer to store received packets.

While the MAX2982 keeps MIIRXDV high, the device sends one byte of data on MIIDAT_OUT for each positive edge on $\overline{BUFRD}$. The first two bytes represent the frame length in MSB first format. After the last byte of data is received, the MAX2982 resets MIIRXDV. The direction of bidirectional data I/Os is controlled through $\overline{BUFCS}$ and $\overline{BUFRD}$. The MAX2982 enables data output drivers when BUFCSN = 0 and BUFRDN = 0. Figure 11 shows the interactions between the external host and the MAX2982.

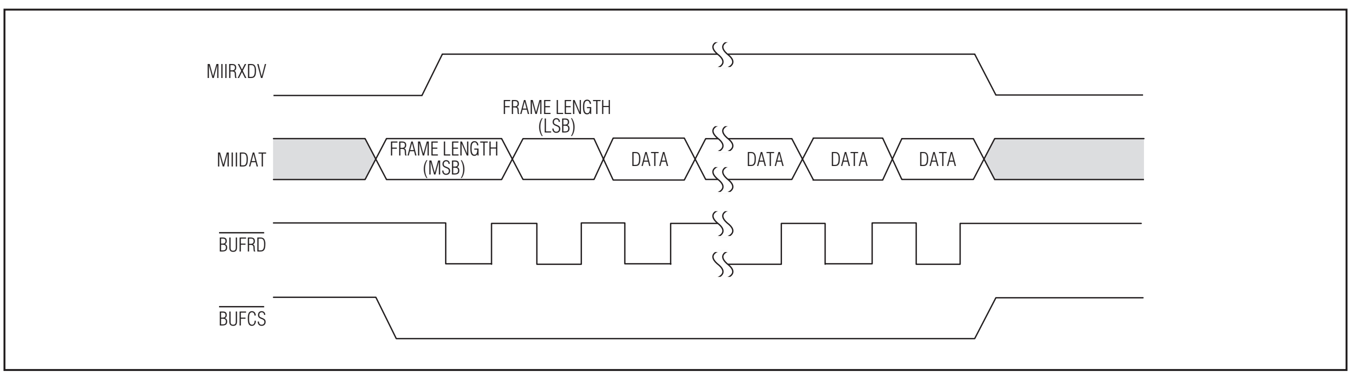


Figure 12. Receive Timing of Buffering (FIFO) Interface

FIFO Read/Write Timing

The FIFO interface is connected to an external data bus in half-duplex mode with independent buffers for TX and RX and MIICLK provided with external processor controls $\overline{BUFRD}$ and $\overline{BUFWR}$ timing as shown in Figures 13 and 14.

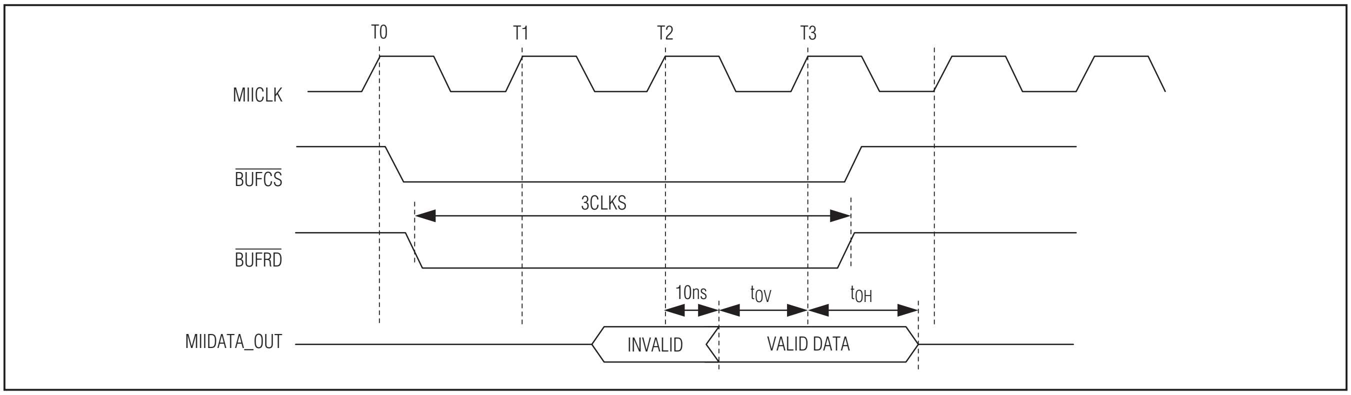


Figure 13. MAX2982 FIFO Read Timing Diagram

1) Minimum CLK frequency is 2.5MHz and maximum is 66MHz.
2) MIIDATA_OUT is valid maximum 10ns after the positive edge of T1. This means that worst case for
 t_{OV} = clock period - 10ns for pulse width of 2ns.
 t_{OV} = 2 x Clock Period -10ns for pulse width of 3ns.
3) MIIDATA_OUT is three-stated maximum 12ns and minimum 5ns after the positive edge of $\overline{BUFRD}$ or $\overline{BUFCS}$ whichever is earlier, which is tOH.
4) MIIDATA_OUT is driven low-Z minimum 0ns after the negative edge of $\overline{BUFRD}$.
5) CLK duty cycle is 40% to 60%.

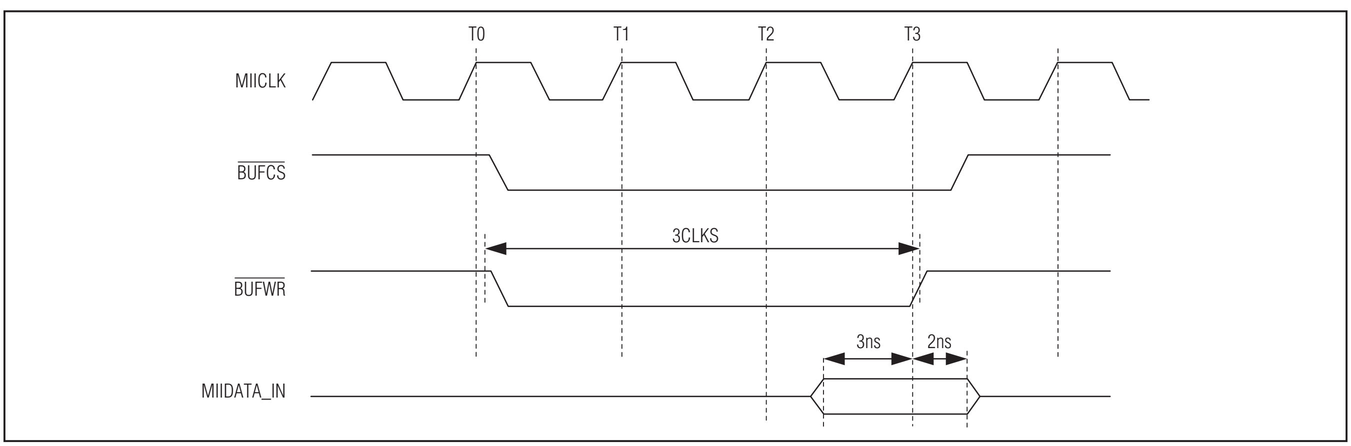


Figure 14. MAX2982 FIFO Write Timing Diagram

1) MIIDATA_IN minimum setup time is 3ns at the positive edge of T2.
2) $\overline{BUFWR}$ and MIIDAT minimum hold time is 2ns at the positive edge of T2.
3) $\overline{BUFWR}$ pulse width is 3 clock cycles long.
4) Minimum CLK frequency is 2.5MHz and maximum is 66MHz.
5) CLK duty cycle is 40% to 60%.

A typical interface between the MAX2982 and a microcontroller at a 66MHz clock rate is shown in Figure 15 with the following setting. $\overline{WR}$ and $\overline{RD}$ signals manage data transfer to/from the FIFO port through $\overline{BUFWR}$ and $\overline{BUFRD}$. $\overline{WR}$ and $\overline{RD}$ are asserted low for three clock cycles and data is valid for at least 3ns.

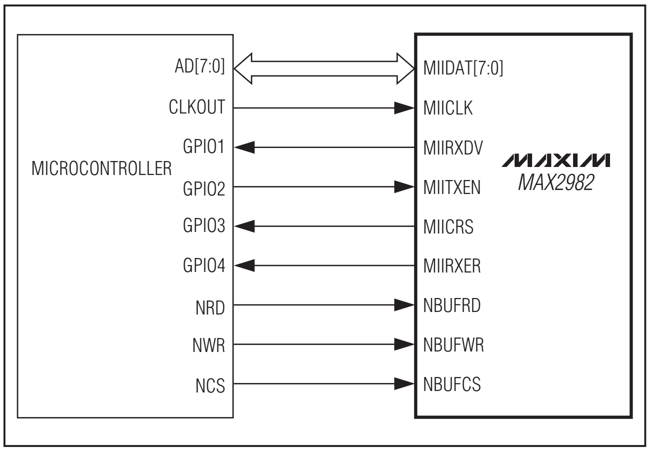


Figure 15. Typical Interface Between a Microcontroller and MAX2982

Microcontroller settings:

CLKOUT Max 66MHz.

$\overline{RD}$ and $\overline{WR}$ access phase set to 3 CLKOUT cycles.

GPIO[1]: When the MAX2982 is ready to send a frame to the microcontroller, the MAX2982 asserts MIIRXDV.

GPIO[2]: When the external host is ready to transmit a frame and MIICRS is not high (the previous transmission is finished), the microcontroller asserts MIITXEN. The external host must assert MIITXEN if MIIRXDV is not high to avoid data loss.

GPIO[3]: Upon assertion of MIITXEN, the MAX2982 asserts MIICRS.

GPIO[4]: When MIIRXER is asserted high, indicates to the microcontroller that an error has occurred during the frame reception.

Management Data Unit (MDU)

The MIIMDIO is a bidirectional data in/output for the Management Data Interface. The MIIMDC signal is a clock reference for the MIIMDIO signal. Figure 16 illustrates the write behavior of the MDU. Figure 17 illustrates the read behavior of the MDU.

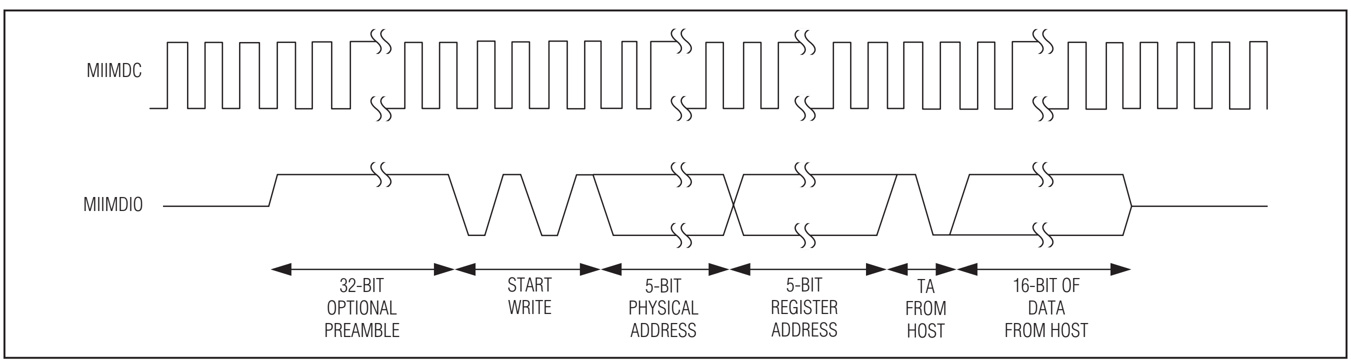


Figure 16. Write Behavior of the Management Data Unit

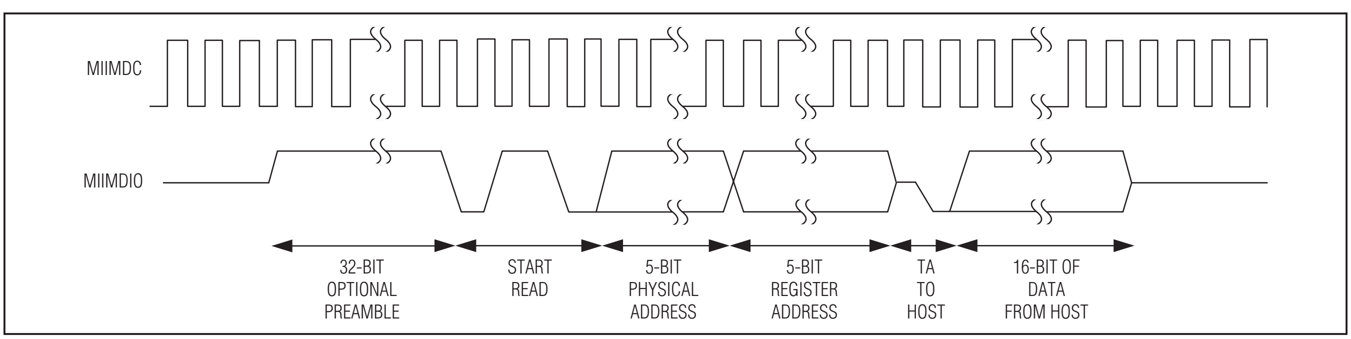


Figure 17. Read Behavior of Management Data Unit

Ethernet Interface

Table 7 shows the upper-layer interface selection. Figure 18 shows the transmit timing. t_{TXDV} is the time that data must be valid for after a low-to-high transition on ETHTXCLK. t_{TXDH} is the time that data must be held after a low-to-high transition on ETHTXCLK. Figure 19 shows the receive timing. t_{RXS} is the setup time prior to the positive edge of ETHRXCLK. t_{RXH} is the hold time after the positive edge of ETHRXCLK. Refer to IEEE 802.3 specification for further information on the Ethernet MAC interface.

Table 7. Upper-Layer Interface Selection GPIO Settings

INTERFACE	GPIO[3] UL2	GPIO[6] AWR_UL1	GPIO[4] ASCL_UL0
MII	1	0	0
RMII	1	0	1

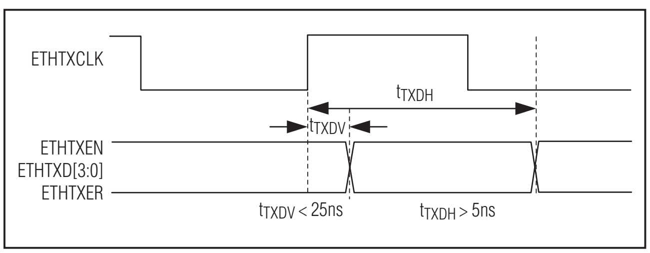


Figure 18. Transmit Timing for Ethernet MAC Interface

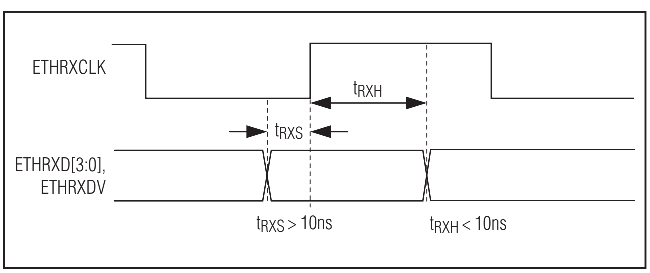


Figure 19. Receive Timing for Ethernet MAC Interface

UART Interface

A serial asynchronous communication protocol using UART standard interface is implemented in the MAX2982 to download MAC firmware. Configure the UART interface as shown in Table 8 to communicate with the current MAC software, unless otherwise noted in the firmware release note.

In order to download and debug HomePlug MAC software use of a null modem cable is required to make a serial connection as shown in Figure 20. The MAX2881 is used as a UART driver.

Table 8. UART Interface Configuration

Data Rate	115200 bps
Data Length	8 Bits
Stop Bit	1 Bit
Flow Control	None

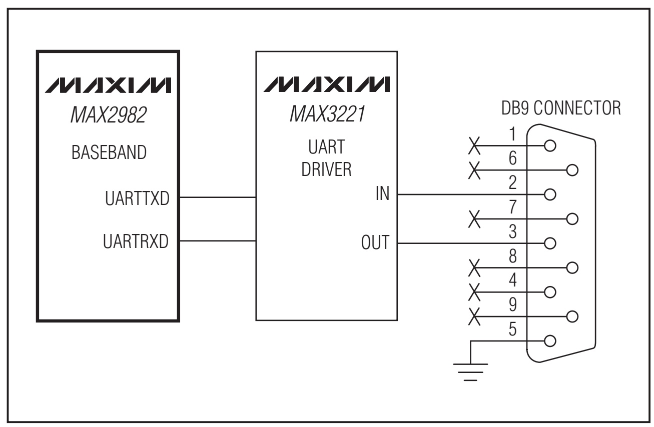


Figure 20. MAX2982 UART Interface with Driver and DB9 Connector

Applications Information

USB INTERFACE		
NAME	DIRECTION	DISABLED STATUS
USBDMNS	I/O	Connect to DGND using a 5.1MΩ resistor
USBDPLS	I/O	N.C.

Disabling Ethernet and MII/RMII/FIFO Interface

MII/RMII/FIFO INTERFACE		
NAME	DIRECTION	DISABLED STATUS
MIICRS	O	N.C.
MIITXEN	I	DGND
MIICLK	I	DGND
MIIDAT[7]	I/O	N.C.
MIIDAT[6]	I/O	N.C.
MIIDAT[5]	I/O	N.C.
MIIDAT[4]	I/O	N.C.
MIIDAT[3]	I/O	N.C.
MIIDAT[2]	I/O	N.C.
MIIDAT[1]	I/O	N.C.
MIIDAT[0]	I/O	N.C.
MIIRXER	O	N.C.
MIIRXDV	O	N.C.
BUFCSN	I	V_{DD33}
BUFRDN	I	V_{DD33}
BUFWRN	I	V_{DD33}
MIIMDC	I	DGND
MIIMDIO	I/O	N.C.

Configure UART I/O as Follows to Disable UART Interface

UART INTERFACE		
NAME	DIRECTION	DISABLED STATUS
UARTTXD	O	N.C.
UARTRXD	I	V_{DD33}

Note: *Disabling the UART interface disables MAC code update and FLASH programming through UART.*

Configure JTAG I/O as Follows to Disable JTAG Interface

JTAG INTERFACE		
NAME	DIRECTION	DISABLED STATUS
JTCK	I	Connect to V_{DD33} using a 10kΩ resistor
JTMS	I	Connect to V_{DD33} using a 10kΩ resistor
JTDO	O	N.C.
JRTCK	O	N.C.
JTDI	I	Connect to V_{DD33} using a 10kΩ resistor
JTRSTN	I	Connect to V_{DD33} using a 10kΩ resistor

Interfacing the MAX2982 to the MAX2981 Analog Front-End (AFE)

The interface to the MAX2981 AFE devices uses a bidirectional bus to pass the digital data to and from the DAC and ADC. Handshake lines help accomplish the data transfer as well as the operation of the AFE. Figure 21 shows the interface signals. See the MAX2981 data sheet for AFE pin configuration/description. Table 9 shows the MAX2982 to MAX2981 signal interface.

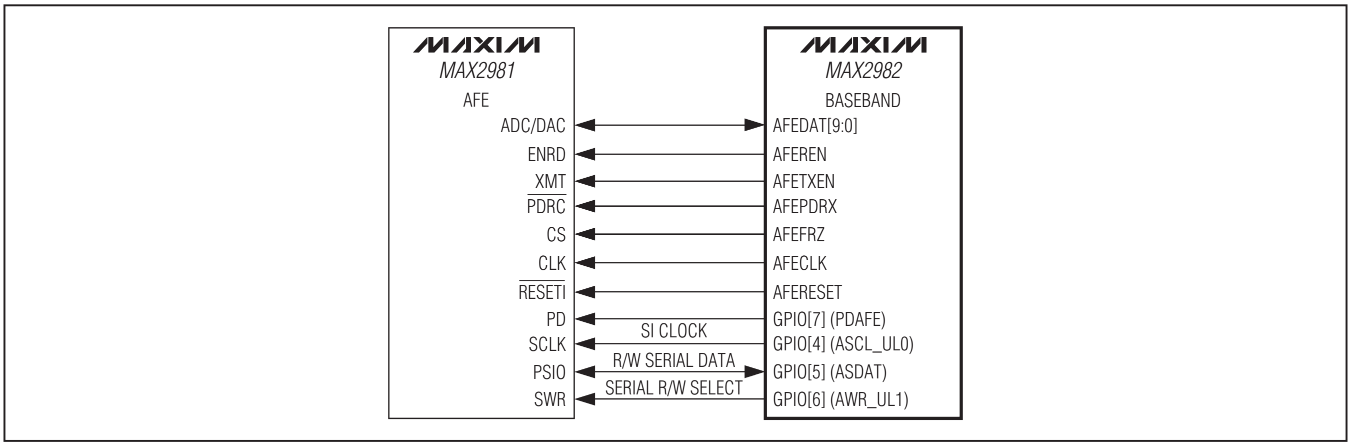
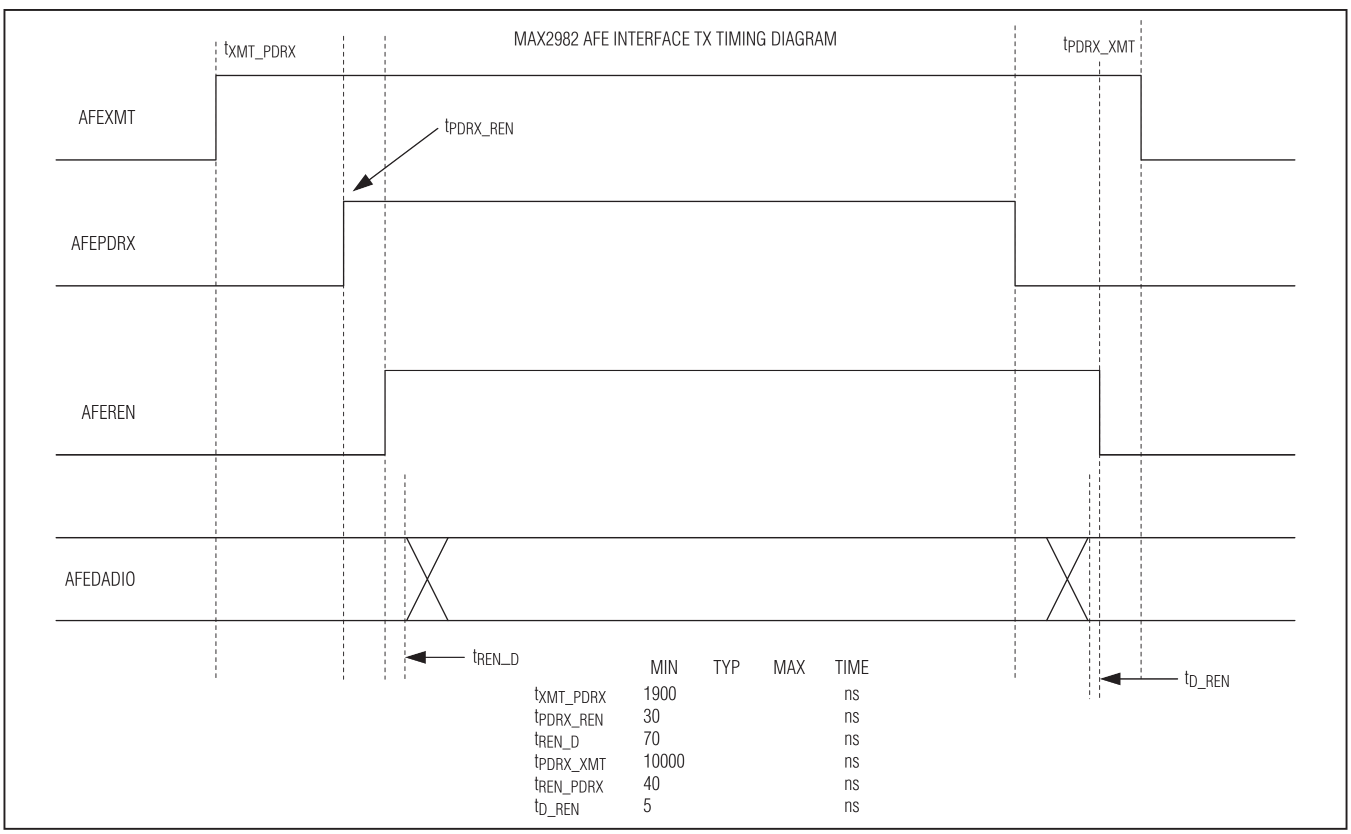


Figure 21. MAX2981 AFE Interface to MAX2982



	MIN	TYP	MAX	TIME
t_{XMT_PDRX}	1900			ns
t_{PDRX_REN}	30			ns
t_{REN_D}	70			ns
t_{PDRX_XMT}	10000			ns
t_{REN_PDRX}	40			ns
t_{D_REN}	5			ns

Figure 22. AFE TX Timing Diagram

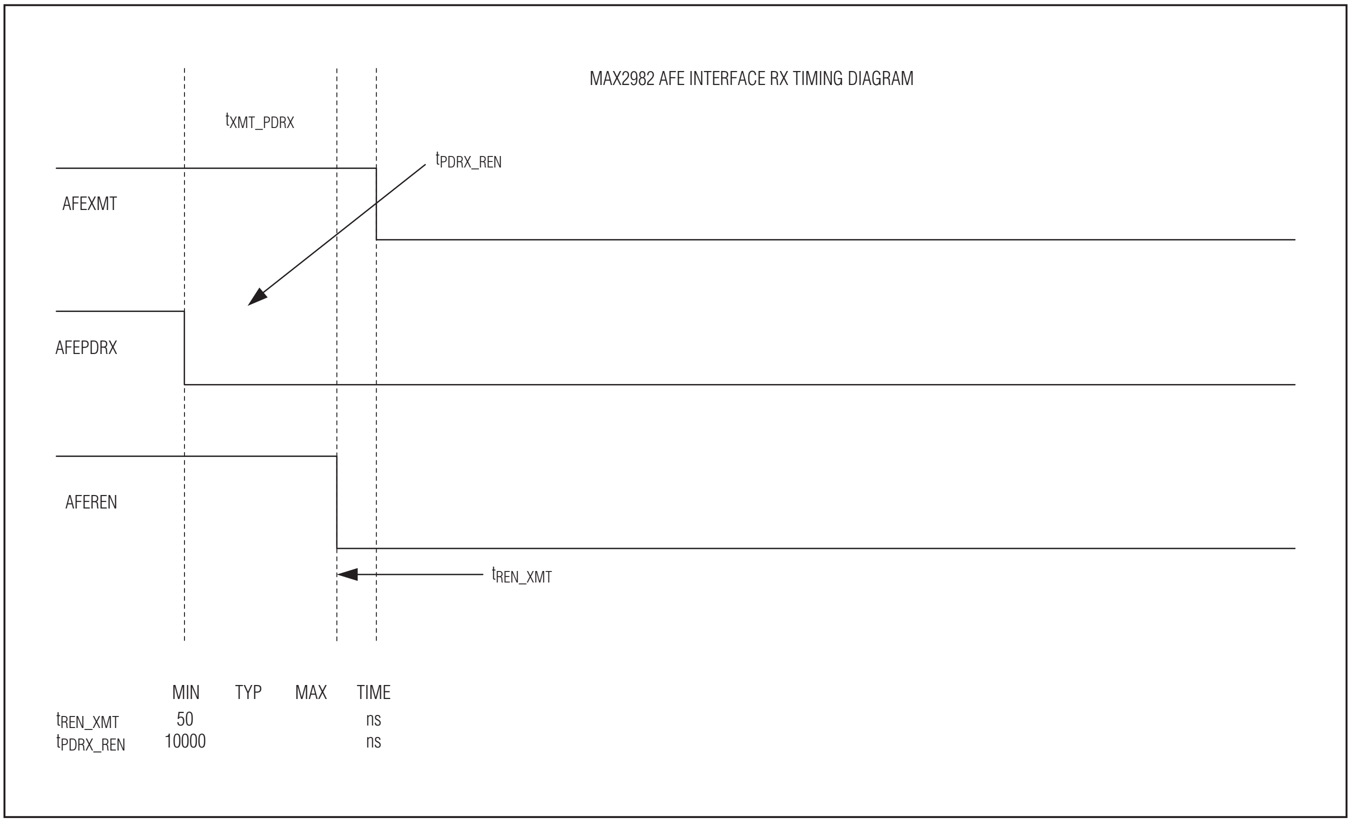


Figure 23. AFE RX Timing Diagram

Table 9. MAX2982 to AFE Signal interface

NAME	DATA LINES	I/O	DESCRIPTION
AFETXEN	1	O	**AFE Transmit Enable.** The AFETXEN signal is used to enable the transmitter of the AFE. When AFETXEN and AFEREN are high, data sent through the AFEDAD[9:0] to the DAC and then into the power line.
AFEREN	1	O	**Setting Bus Direction.** The AFEREN signal sets the direction of the data bus AFEDAD[9:0]. When high, data can be sent from the MAX2982 to the DAC in the AFE, and when low, data is sent from the ADC to the MAX2982.
AFEPDRX	1	O	**AFE Receiver Power-Down.** When the AFE is in transmit mode, the AFEPDRX signal goes high, the receiver section of the AFE is powered down. The MAX2981 features a transmit power-savings mode which reduces current dissipation from 280mA to 155mA. To use this power-saving mode, lower AFEPDRX 10µs prior to the end of a transmission. If this mode is not required, connect AFEPDRX to AFETXEN and AFEREN. In this case, the MAX2981 consumes 280mA.
AFEDAD[9:0]	10	I/O	**AFE 10-Bit ADC and DAC Bus.** AFEDAD[9:0] is the 10-bit bidirectional bus that connects the MAX2982 to the AFE DAC and ADC. The direction of the bus is controlled by AFEREN described above.

Table 9. MAX2982 to AFE Signal interface (continued)

NAME	DATA LINES	I/O	DESCRIPTION
AFEFRZ	1	O	**AFE Receive AGC Control.** The AFEFRZ signal controls the AGC circuit in the receive path in the AFE. When this signal is low, the gain circuit on the input signal continuously adapts for maximum sensitivity. This signal is raised high when the MAX2982 detects a valid preamble. After the AFEFRZ signal is raised high, it continues to adapt for an additional short period of time, then it locks the currently adapted level on the incoming signal. The MAX2982 holds AFEFRZ high while receiving a transmission, and then lowers for continuous adaptation for maximum sensitivity of other incoming signals.
AFECLK	1	O	**AFE Clock** is a 50MHz clock generated for the MAX2981 AFE
AFERESET	1	O	**AFE Reset.** To perform a reset on the MAX2981 AFE, AFECLK must be free running and AFERESET must be low for a minimum of 100ns. A reset must be performed at power-up.
GPIO[6] (AWR_UL1)	1	O	AFE Serial-Interface Read/Write Select
GPIO[5] (ASDAT)	1	I/O	AFE Serial-Interface Data (Write/Read)
GPIO[4] (ASCL_UL0)	1	O	AFE Serial-Interface Clock
GPIO[7] (PDAFE)	1	O	AFE Power-Down

MAC Boot Options

The MAX2982 on-chip ROM is programmed with a booting application to decrypt and load encrypted MAC firmware into on-chip RAM for execution from an external source. The source is determined by the boot mode selected. Standard HomePlug 1.0 firmware or LORA firmware and a number of other boot images are available. The selection of boot modes is controlled through boot pins GPIO[21:23] (see Table 11), which are sensed during the MAX2982 startup process. There are three boot options:

1) Downloading encrypted flash-resident code

   The image can be downloaded from two supported serial peripheral interface (SPI) flash devices (AT45DB011B/M25P10-A). The image is stored in flash encrypted. A few words at the start of flash memory contain information such as the address of location in which the code image is stored.

2) The encrypted code image in flash is updated using Trivial File Transfer Protocol (TFTP) application.

   TFTP is a standard protocol to transfer files. A TFTP application can be used to upload the encrypted code image to the MAX2982 through one of the upper-layer interfaces (ETH/MII/RMII/FIFO). To invoke the MAX2982 TFTP boot mode, the boot pins must be set according to Table 11 before reset. In this mode, the MAX2982 bootloader expects to receive the image from one of the upper-layer interfaces. The default TFTP server IP address is 10.1.254.250 if no flash device is present. This parameter can be modified and programmed into the external flash. If the integrity of the received image is ok and the external flash device is available, the image in flash will be updated and executed. Any errors that happened during the TFTP session will be reported to the TFTP client.

3) Simple code download through UART.

   The MAX2982 is configurable to accept code images from the UART. The first four bytes of the image specify the memory location in SRAM to which the binary image is copied (0x2020000–0x203FFFF). The next four bytes specify the length of the image (excluding eight header and four tail bytes). The specified length cannot be greater than 128KB (size of SRAM) and must be nonzero. Otherwise, the boot restarts simple code download through UART after issuing an appropriate error message to the host. The last four bytes of the image are the checksum. This is the NOT value of XOR of all words in binary image. After the image is loaded, the last four bytes are read as the image checksum. This value is compared against the value calculated over the loaded image. If these two values are identical then the image is launched by jumping to the target (destination) address, otherwise, the boot restarts simple code download through the UART.

Five GPIOs are used to determine the boot mode. Table 10 shows the corresponding settings (PU: pulled up, PD: pulled down, X: don't care). Pullup and pulldown resistors are 10kΩ. ISCL_FT0 and IWCS_FT1 are used for flash operations. These two are outputs in flash operations but are inputs in the system boot process.

If an error occurs during the boot process, the error code is indicated on the LED outputs: LED0_ BP0, LED1_ BP1, and LED2_ BP2 according to Table 11. Pullup/pulldown resistors for LEDs are 1kΩ or less.

The states of GPIOs and initialization inputs during the boot process are shown in Table 10. See the *Pin Description* for more information.

GPIO Usage by MAX2982 Firmware

The MAX2982 firmware makes special use of GPIOs as described in Table 12. GPIOs are utilized in input, output, or both directions.

Table 10. Boot Modes

CODE DOWNLOAD	BOOT GPIOs					
	FLASH TYPE	GPIO[23] (HPACT_BP2)	GPIO[22] (HPLINK_BP1)	GPIO[21] (HPCOL_BP0)	GPIO[8] (ISCL)	GPIO[10] (IWCS)
Encrypted image download from flash	Flash type is SPI (AT45DBxxx)	0	1	0	PU	PU
	Flash type is SPI (M25P10-A)	1	1	0	PU	PU
Encrypted image download via Ethernet or MII interface using TFTP	Flash type is SPI (AT45DBxxx)	0	0	1	PU	PU*
	Flash type is SPI (M25P10-A)	1	0	1	PU	PU*
Code download through UART	Flash Type is SPI** (AT45DBxxx)	0	0	0	X	PU*
	Flash type is SPI (M25P10-A)	1	0	0		

**If IWCS is pulled down instead of pulled up to indicate that there is no flash device connected. If this is the case and if LED0_ BP0 = LED1_ BP1 = 0, then ISCL GPIO must be pulled up.*

***External flash used to store code image and configuration parameters.*

Table 11. Boot Error Codes

LED2_BP2	LED1_BP1	LED0_BP0	BOOT STATUS
0	0	1	The flash does not contain a valid image
0	1	0	The size of image is more than 128KB
0	1	1	The base address of image is out of the allowed range
1	0	0	Checksum error
1	0	1	No flash is available
1	1	0	Invalid boot mode
1	1	1	No error
0	0	0	

Upper-Layer Interface Settings

The MAX2982 supports different upper-layer interfaces described in Table 13.

UL2 is used in input direction only to set bit 2 of the upper-layer interface. AWR_UL1 and ASCL_UL0 are all dual-purpose GPIOs. At input direction AWR_UL1 and ASCL_UL0 set upper-layer interface bits 0 and 1. At output direction, AFE inputs SWR (MAX2981) and SCLK (MAX2981 Pin 22) are driven by these GPIOs.

Temperature Sensor

The MAX2982 includes an analog temperature sensor that measures the die temperature to enable temperature monitoring and provides an output voltage proportional to degrees Celsius (see the *Typical Operating Characteristics*). The temperature sensor provides ±5°C accuracy from -50°C to +125°C. The temperature sensor output is resistive with an impedance of typically 185kΩ.

Table 12. GPIO Pins Used by MAX2982 Firmware

GPIO	FUNCTION NAME	DESCRIPTION
GPIO[23]	HPACT_BP2	Output: Drive AFE interface activity LED
		Input: Boot pin 2
GPIO[22]	HPLINK_BP1	Output: Drive AFE interface link status LED
		Input: Boot pin 1
GPIO[21]	HPCOL_BP0	Output: Drive AFE interface collision LED
		Input: Boot pin 0
GPIO[10]	IWCS_FT1	Output: Flash interface chip select
		Input: Nonvolatile memory bit 1
GPIO[9]	ISDAT	Output: Flash interface data (write)
		Input: Flash interface data (read)
GPIO[8]	ISCL_FT0	Output: Flash interface serial clock
		Input: Nonvolatile memory, bit 0
GPIO[7]	PDAFE	Output: AFE power-down
		Input: None
GPIO[6]	AWR_UL1	Output: AFE serial-interface write
		Input: Upper interface select, bit 1
GPIO[5]	ASDAT	Output: AFE serial interface data (write)
		Input: AFE serial interface data (read)
GPIO[4]	ASCL_UL0	Output: AFE serial interface clock
		Input: Upper-layer interface select, bit 0
GPIO[3]	UL2	Output: None
		Input: Upper-layer interface select, bit 2

Table 13. Upper-Layer Interface Settings

INTERFACE	UL2 (GPIO3)	UL1 (GPIO6)	UL0 (GPIO4)
MII	0	0	1
RMII	0	1	0
FIFO	0	1	1
ETH (MII)	1	0	0
ETH (RMII)	1	0	1
Reserved	0	0	0
Reserved	1	1	1

Industrial Broadband Power-Line Modem

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2982GCD/V+	-40°C to +105°C	128 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automative-qualified part.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
128 LQFP	C128+1	**21-0086**	**90-0143**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—