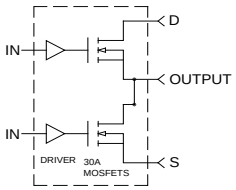
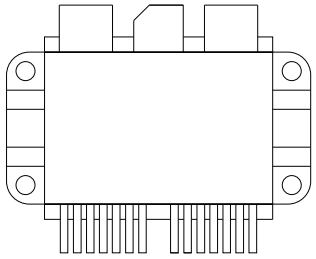
DRF1400

500V, 30A, 30MHz

MOSFET Half Bridge Hybrid

The DRF1400 is a half bridge hybrid containing two high power gate drivers and two power MOSFETs. It was designed to provide the system designer increased flexibility, higher performance and lowered cost over a non-integrated solution. This low parasitic approach, coupled with the Schmitt trigger input, Kelvin signal ground, anti-Ring function Invert and Non-invert select pin provide improved stability and control in Kilowatt to Multi-Kilowatt, High Frequency ISM applications.





FEATURES

- **Switching Frequency: DC TO 30MHz**
- **Inverting Non-Inverting Select**
- **Low Pulse Width Distortion**
- **Single Power Supply (Per Section)**
- **1V CMOS Schmitt Trigger Input 1V Hysteresis**
- **Switching Speed 3-4ns**
- **B_{Vds} = 500V**
- **I_{ds} = 30A avg. Per-section**
- **$R_{ds(on)} \leq .24$ Ohm**
- **P_D = 550W Per-section**
- **RoHS Compliant**

TYPICAL APPLICATIONS

- **Class D Half Bridge RF Generetors**
- **Switch Mode Power Amplifiers**
- **HV Pulse Generators**
- **Ultrasound Transducer Drivers**
- **Acoustic Optical Modulators**

Driver Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
V_{DD}	Supply Voltage	15	V
IN, FN	Input Single Voltages	-.7 to +5.5	
$I_{O\,PK}$	Output Current Peak	8	A
T_{JMAX}	Operating Temperature	175	°C

Driver Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Supply Voltage	8	12	15	V
IN	Input Voltage	3		5	
$IN_{(R)}$	Input Voltage Rising Edge		3		ns
$IN_{(F)}$	Input Voltage Falling Edge		3		
I_{DDQ}	Quiescent Current		2		mA
I_O	Output Current		8		A
C_{oss}	Output Capacitance		2500		pF
C_{iss}	Input Capacitance		3		
R_{IN}	Input Parallel Resistance		1		mΩ
$V_{T(ON)}$	Input, Low to High Out	0.8		1.1	V
$V_{T(OFF)}$	Input, High to Low Out	1.9		2.2	
T_{DLY}	Time Delay (throughput)		38		ns
t_r	Rise Time		5		ns
t_f	Fall Time		5		
T_D	Prop. Delay		35		

MOSFET Absolute Maximum Ratings (Per-Section) DRF1400

Symbol	Parameter	Min	Typ	Max	Unit
BV_{DSS}	Drain Source Voltage	500			V
I_D	Continuous Drain Current T_{HS} = 25°C			30	A
$R_{DS(on)}$	Drain-Source On State Resistance		0.24		Ω

Dynamic Characteristics (Per-Section)

Symbol	Parameter	Min	Typ	Max	Unit
C_{iss}	Input Capacitance		1800		pF
C_{oss}	Output Capacitance		335		
C_{rss}	Reverse Transfer Capacitance		75		

Thermal Characteristics (Total Package)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance	.06	°C/W
$R_{\theta JHS}$	Junction to Heat Sink Thermal Resistance	.134	
T_{JSTG}	Storage Junction Temperature	-55 to 150	°C
P_D	Maximum Power Dissipation @ T_{SINK} = 25°C	1.1	KW
P_{DC}	Total Power Dissipation @ T_C = 25°C	2.5	

Section A and B Output Switching Performance

Symbol	Characteristic	Min	Typ	Max	Typ
T_{ON}	Leading Edge 10% to 90%	2	3	4	ns
T_{OFF}	Trailing Edge 10% to 90%	45	TBD	49	
$T_{DLY(ON)}$	Total Throughput Delay Time, ON	47	TBD	45	
$T_{DLY(OFF)}$	Total Throughput Delay Time, OFF	49	50	51	
$\Delta T_{DLY(ON)}$	Delta T_{ON} Delay between Section A and B	-0.5	0	1.5	
$\Delta T_{DLY(OFF)}$	Delta T_{OFF} Delay between Section A and B	0	0.6	1.3	

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

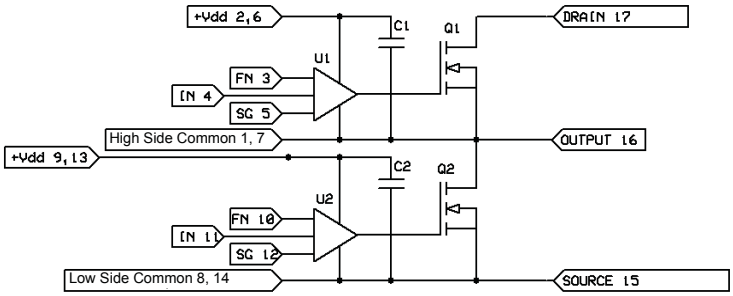


Figure 1, DRF1400 Test Circuit Diagram

The DRF1400 is configured as a Half Bridge Hybrid incorporating two independent channels consisting of a driver, a high voltage MOSFET and by-pass capacitors. The function of the by-pass capacitors C1 and C2 is to reduce the internal parasitic loop inductance. This coupled with the tight geometry of the hybrid allows optimal gate drive to the MOSFET. This low parasitic approach coupled with the Schmitt trigger input (IN), Kelvin signal ground (SG) and the Anti-Ring function; provide improved stability and control in Kilowatt to Multi-Kilowatt high frequency applications. The IN pin should be referenced to the Kelvin Ground (SG) and is applied to a Schmitt Trigger. The SG pin is a Kelvin return for the IN pin only. The signal is then applied to the intermediate drivers and level shifters; this section contains proprietary circuitry designed specifically for ring abatement. To further increase the utility of the device the driver die and the MOSFET die are adjacent die selected. This provides a very close match in the turn on and propagation delays.

None of the inputs to U1 or U2 of the DRF1400 are isolated for direct connection to a ground referenced power supply or control circuitry. **Isolation appropriate to the application is the responsibility of the end user.** It is imperative that high output currents be restricted to the Drain (17), Source (15) Output (16) and the C3 Bypass (18, 19) connection pins by design. See DRF100 for more information on Driver IC used in the device.

The Function (FN, pin 3 or pin 9) is the invert or non-invert select Pin, it is Internally held high.

Truth Table * Referenced to SG		
FN (pin 3)	**IN (pin 4)**	**MOSFET**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**

Truth Table * Referenced to SG		
FN (pin 9)	**IN (pin 10)**	**MOSFET**
HIGH	**HIGH**	**ON**
HIGH	**LOW**	**OFF**
LOW	**HIGH**	**OFF**
LOW	**LOW**	**ON**

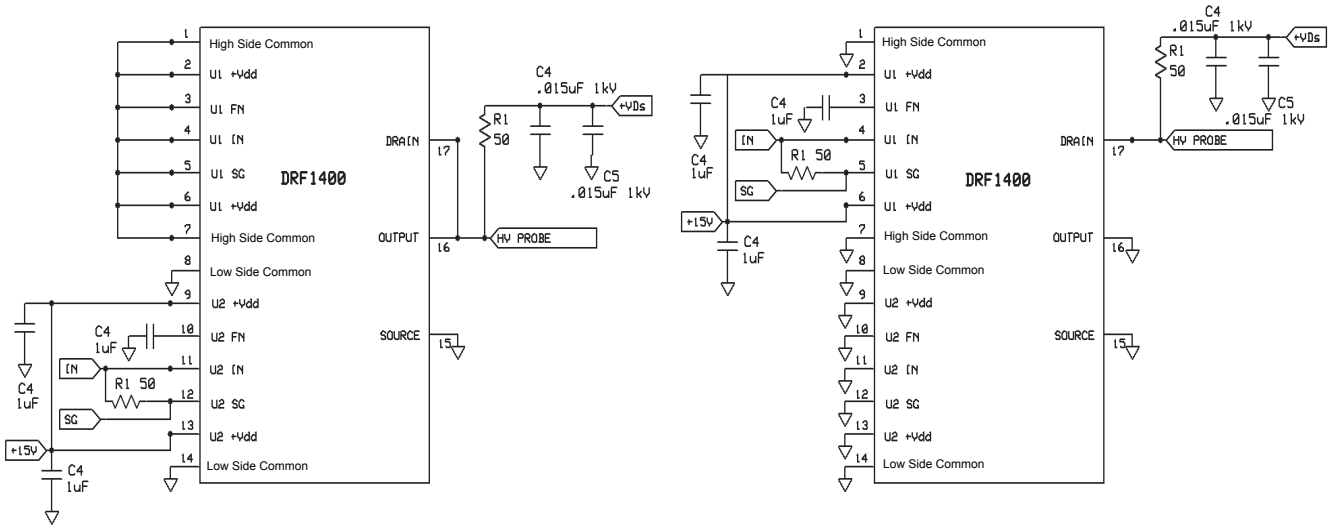
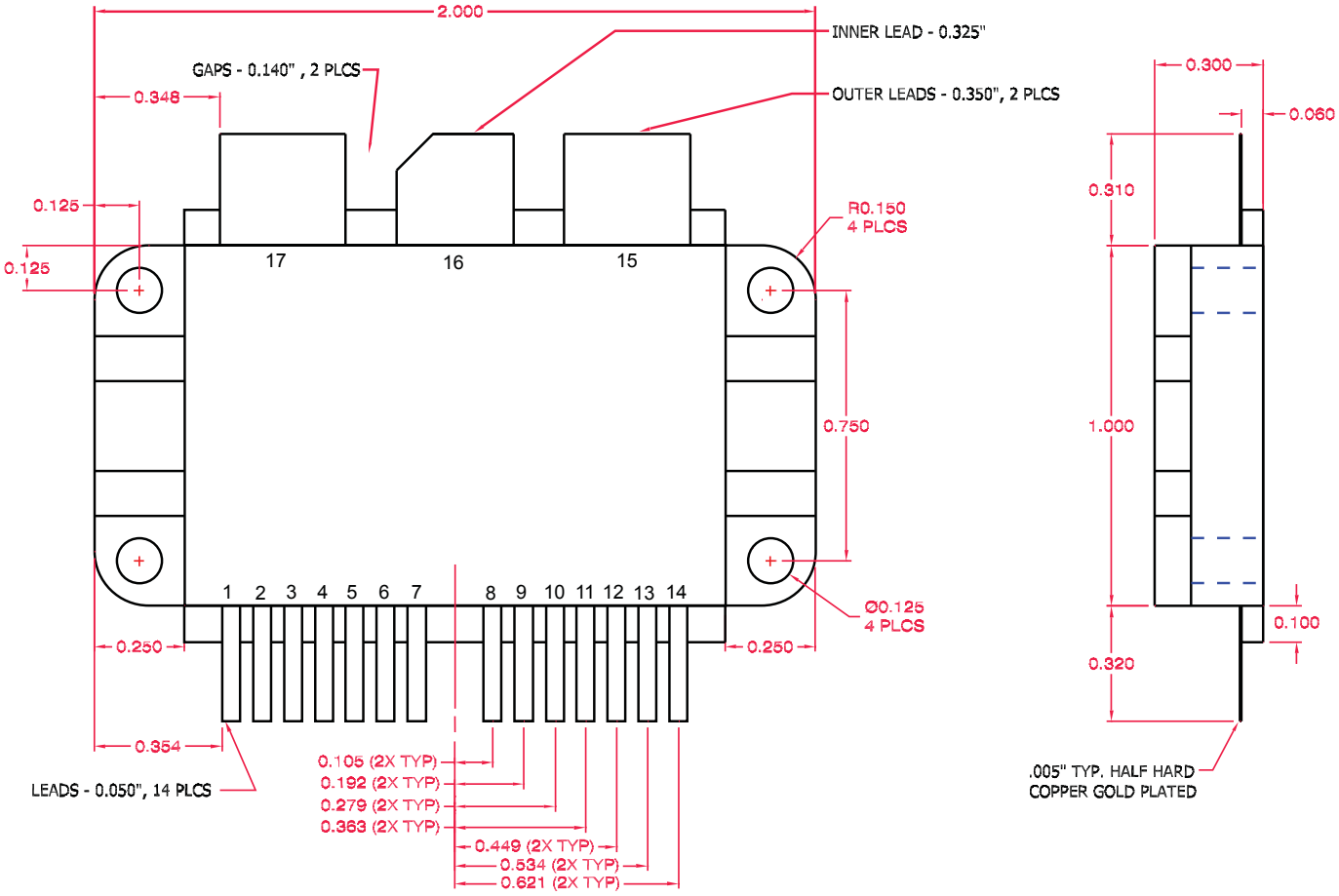


Figure 2, DRF1400 Test Circuit

The test circuit illustrated in Figure 2 was used to evaluate the DRF1400. The input control signal is applied via IN and SG pins using RG188. This provides excellent noise immunity and control of the signal ground currents. The $+V_{DD}$ inputs (pins 2, 6, 8 and 12) should be heavily by-passed by 1uF capacitors as close to the pins as possible. The capacitors used for this function must be capable of supporting the RMS currents and frequency of the gate load. A 50 Ohm (RL) load is used to evaluate the output performance.

Pin Assignments	
Pin 1	High Side GND
Pin 2	U1 +Vdd
Pin 3	U1 FN
Pin 4	U1 IN
Pin 5	U1 SG
Pin 6	U1 +Vdd
Pin 7	High Side GND
Pin 8	Low Side GND
Pin 9	U2 +Vdd
Pin 10	U2 FN
Pin 11	U2 IN
Pin 12	U2 SG
Pin 13	U2 +Vdd
Pin 14	Low Side GND
Pin 15	Source
Pin 16	Output
Pin 17	Drain



All dimensions are ± .005

Figure 4, DRF1400 Mechanical Outline