PIC16C63A/65B/73B/74B Data Sheet Errata

The PIC16C63A/65B/73B/74B parts you have received conform functionally to the Device Data Sheet (DS30605**C**), except for the anomalies described below.

None.

Clarifications/Corrections to the Data Sheet:

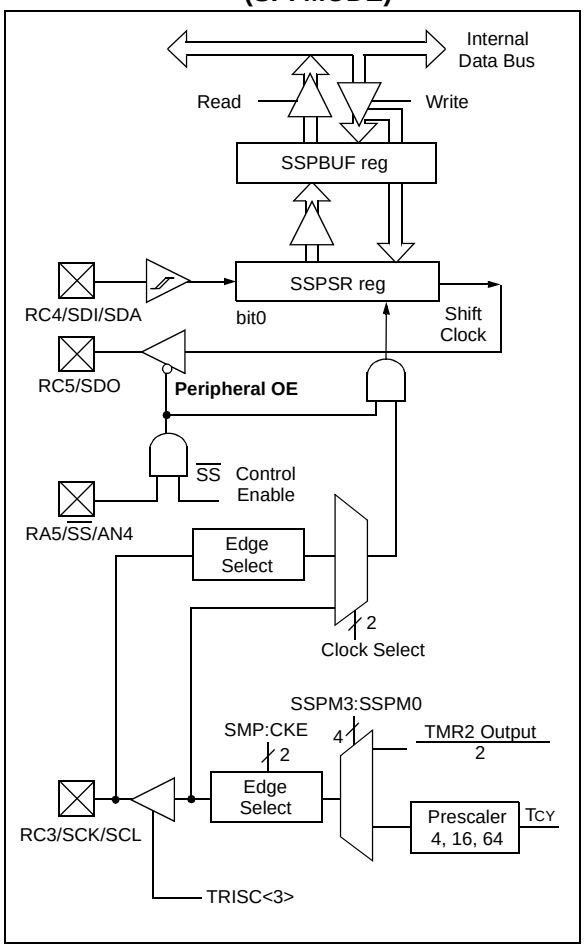
In the Device Data Sheet (DS30605**C**), the following clarifications and corrections should be noted.

1. Module: SSP (SPI™ Mode)

In Section 10.2 (“SPI Mode”), Figure 10-1 and the note box immediately beneath it have been amended to better demonstrate the Peripheral OE line of the SSP module and describe its relationship to the TRISC<5> bit of PORTC.

Changes are indicated in **bold**.

FIGURE 10-1: SSP BLOCK DIAGRAM (SPI MODE)



Note 1: When the SPI module is in Slave mode with SS pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the SS pin is set to VDD.

2: If the SPI is used in Slave mode with CKE = '1', then SS pin control must be enabled.

3: **When the SPI is in Slave mode with SS pin control enabled (SSPCON<3:0> = 0100), the state of the SS pin can affect the state read back from the TRISC<5> bit. The Peripheral OE signal from the SSP module into PORTC, controls the state that is read back from the TRISC<5> bit (see Section 5.3 for information on PORTC). If Read-Modify-Write instructions, such as BSF, are performed on the TRISC register while the SS pin is high, this will cause the TRISC<5> bit to be set, thus disabling the SDO output.**

2. Module: Packaging (Pinout and Product Identification)

PIC16C63A and PIC16C73B devices are now offered in 28-pin near chip-scale micro lead frame packages (commonly known as “QFN”). This packaging type has been added to the product line since the latest revision of the Device Data Sheet.

The addition of this option requires the following additions to the Device Data Sheet. The referenced figures and tables follow this text.

1. The “Pin Diagram” on page 2 of the Data Sheet is amended with the addition of the 28-pin QFN pinout, shown in Figure 1.
2. Table 3-1 of Section 3.0 (“Architectural Overview”) is replaced with an updated version that adds a column for QFN pin assignments. All new information is indicated in **bold**.
3. Section 18.1 (“Package Marking Information”) is amended to include a marking template and example for 28-pin QFN devices. These are shown in Figure 2.
4. Section 18.0 (“Package Information”) is amended to include the mechanical drawings of the 28-pin QFN package. These are shown in Figure 3 and Figure 4, respectively.
5. Table B-1 (“Device Differences”) is amended to include the 28-pin QFN for the PIC16C63A and PIC16C73B devices.

FIGURE 1: PINOUT DIAGRAM FOR PIC16C63A AND PIC16C73B, 28-PIN QFN

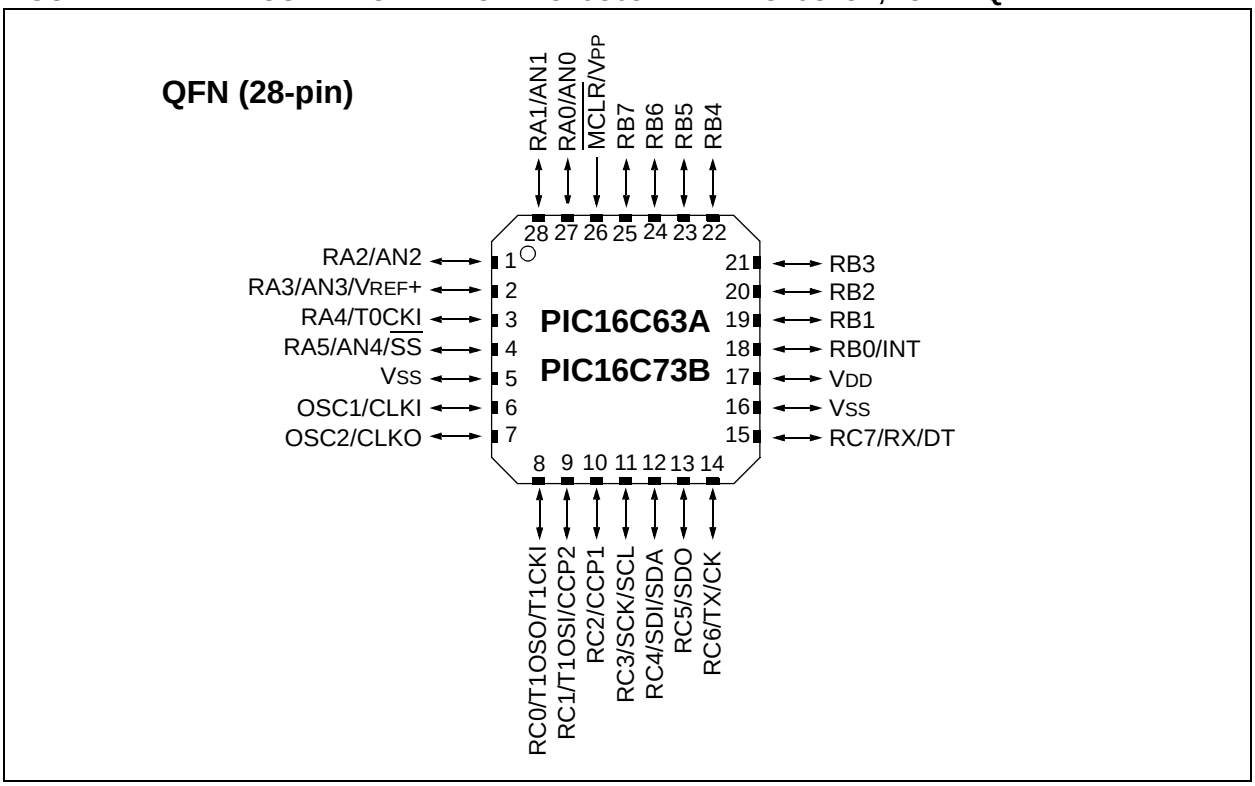


FIGURE 2: PACKAGE MARKING TEMPLATE FOR PIC16C63A AND PIC16C73B, 28-PIN QFN

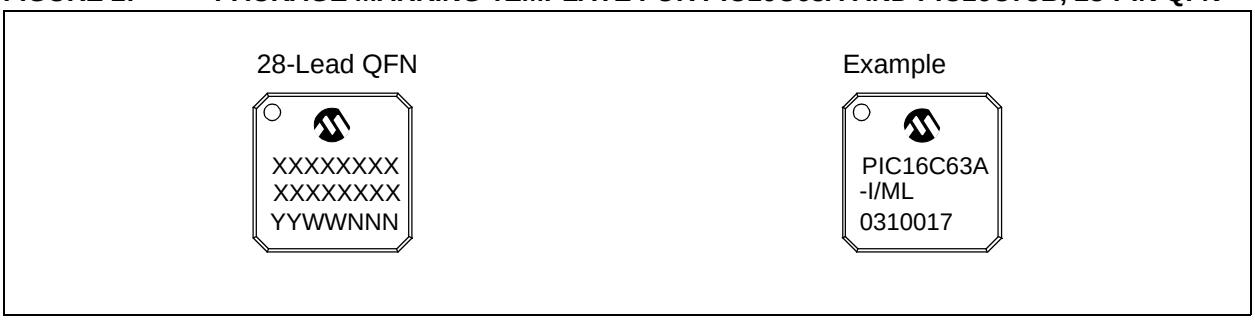


TABLE 3-1: PIC16C63A/73B PINOUT DESCRIPTION

Pin Name	DIP Pin#	SOIC Pin#	QFN Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKIN	9	9	**6**	I	ST/CMOS(3)	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	10	10	**7**	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, the OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	1	1	**26**	I/P	ST	Master clear (RESET) input or programming voltage input. This pin is an active low RESET to the device.
						PORTA is a bidirectional I/O port.
RA0/AN0(4)	2	2	**27**	I/O	TTL	RA0 can also be analog input 0(4).
RA1/AN1(4)	3	3	**28**	I/O	TTL	RA1 can also be analog input 1(4).
RA2/AN2(4)	4	4	**1**	I/O	TTL	RA2 can also be analog input 2(4).
RA3/AN3/VREF(4)	5	5	**2**	I/O	TTL	RA3 can also be analog input 3 or analog reference voltage(4).
RA4/T0CKI	6	6	**3**	I/O	ST	RA4 can also be the clock input to the Timer0 module. Output is open drain type.
RA5/SS/AN4(4)	7	7	**4**	I/O	TTL	RA5 can also be analog input 4(4) or the slave select for the synchronous serial port.
						PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.
RB0/INT	21	21	**18**	I/O	TTL/ST(1)	RB0 can also be the external interrupt pin.
RB1	22	22	**19**	I/O	TTL	
RB2	23	23	**20**	I/O	TTL	
RB3	24	24	**21**	I/O	TTL	
RB4	25	25	**22**	I/O	TTL	Interrupt-on-change pin.
RB5	26	26	**23**	I/O	TTL	Interrupt-on-change pin.
RB6	27	27	**24**	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming clock.
RB7	28	28	**25**	I/O	TTL/ST(2)	Interrupt-on-change pin. Serial programming data.
						PORTC is a bidirectional I/O port.
RC0/T1OSO/T1CKI	11	11	**8**	I/O	ST	RC0 can also be the Timer1 oscillator output or Timer1 clock input.
RC1/T1OSI/CCP2	12	12	**9**	I/O	ST	RC1 can also be the Timer1 oscillator input or Capture2 input/Compare2 output/PWM2 output.
RC2/CCP1	13	13	**10**	I/O	ST	RC2 can also be the Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	14	14	**11**	I/O	ST	RC3 can also be the synchronous serial clock input/output for both SPI and I^2C modes.
RC4/SDI/SDA	15	15	**12**	I/O	ST	RC4 can also be the SPI Data In (SPI mode) or data I/O (I^2C mode).
RC5/SDO	16	16	**13**	I/O	ST	RC5 can also be the SPI Data Out (SPI mode).
RC6/TX/CK	17	17	**14**	I/O	ST	RC6 can also be the USART Asynchronous Transmit or Synchronous Clock.
RC7/RX/DT	18	18	**15**	I/O	ST	RC7 can also be the USART Asynchronous Receive or Synchronous Data.
VSS	8, 19	8, 19	**16**	P	—	Ground reference for logic and I/O pins.
VDD	20	20	**17**	P	—	Positive supply for logic and I/O pins.

Legend: I = input O = output I/O = input/output P = power
— = Not used TTL = TTL input ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

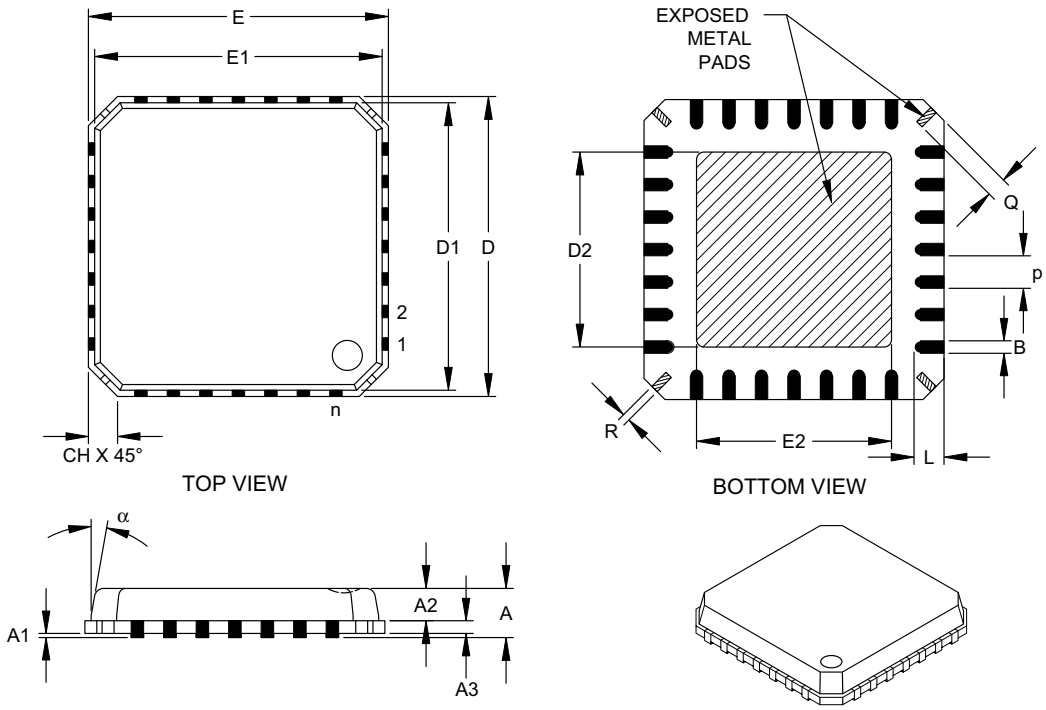
2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

4: A/D module is not available in the PIC16C63A.

FIGURE 3: 28-PIN QFN PACKAGE (DRAWING 1, PACKAGING)

28-Lead Plastic Quad Flat No Lead Package (ML) 6x6 mm Body, Punch Singulated (QFN)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A		.033	.039		0.85	1.00
Molded Package Thickness	A2		.026	.031		0.65	0.80
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3		.008 REF			0.20 REF	
Overall Width	E		.236 BSC			6.00 BSC	
Molded Package Width	E1		.226 BSC			5.75 BSC	
Exposed Pad Width	E2	.140	.146	.152	3.55	3.70	3.85
Overall Length	D		.236 BSC			6.00 BSC	
Molded Package Length	D1		.226 BSC			5.75 BSC	
Exposed Pad Length	D2	.140	.146	.152	3.55	3.70	3.85
Lead Width	B	.009	.011	.014	0.23	0.28	0.35
Lead Length	L	.020	.024	.030	0.50	0.60	0.75
Tie Bar Width	R	.005	.007	.010	0.13	0.17	0.23
Tie Bar Length	Q	.012	.016	.026	0.30	0.40	0.65
Chamfer	CH	.009	.017	.024	0.24	0.42	0.60
Mold Draft Angle Top	α			12°			12°

*Controlling Parameter

Notes:

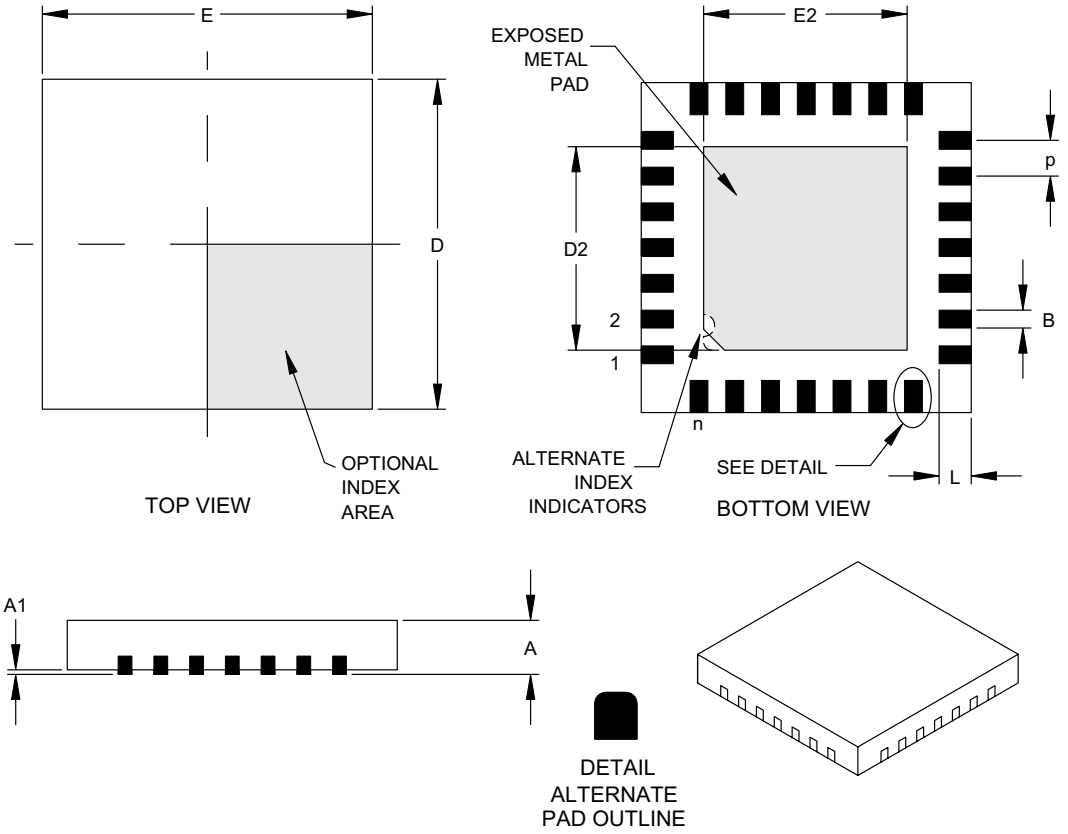
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: mMO-220

Drawing No. C04-114

FIGURE 4: 28-PIN QFN PACKAGE (DRAWING 2, PACKAGING)

28-Lead Plastic Quad Flat No Lead Package (ML) 6x6 mm Body, Saw Singulated (QFN)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0.00	0.02	0.05
Overall Width	E	.232	.236	.240	5.90	6.00	6.10
Exposed Pad Width	E2	.140	.146	.152	3.55	3.70	3.85
Overall Length	D	.232	.236	.240	5.90	6.00	6.10
Exposed Pad Length	D2	.140	.146	.152	3.55	3.70	3.85
Lead Width	B	.009	.011	.013	0.23	0.28	0.33
Lead Length	L	.020	.022	.024	0.50	0.55	0.60

*Controlling Parameter

Notes:

JEDEC equivalent: mMO-220

Drawing No. C04-105

3. Module: RESET

Section 13.4.1 (“POWER-ON RESET (POR)”) has been amended to clarify the minimum specifications required for $\overline{MCLR}$ in order to RESET the PIC16CXXX. The following paragraphs and figure have been added:

If a $\overline{MCLR}$ pulse occurs that is less that the minimum specification (parameter #30), improper device operation can occur.

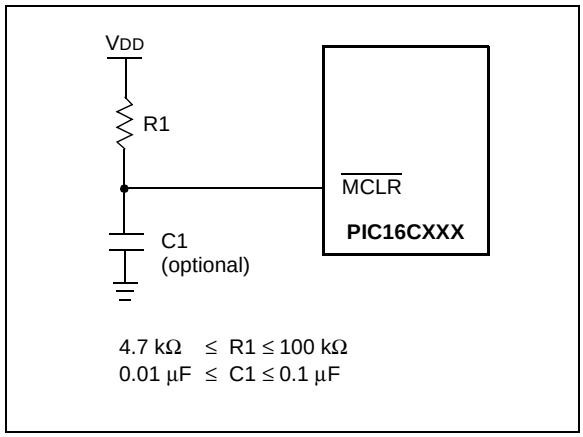
If the minimum specification cannot be met, then an external circuit must be used to ensure that any pulse width less than the specification will be filtered before it reaches the $\overline{MCLR}$ pin.

A possible circuit to remedy this is shown in Figure 5. This circuit works by delaying the $\overline{MCLR}$ release following a power-up. If no delay is required, the capacitor may be omitted.

An alternative would be to use a supervisory circuit to control $\overline{MCLR}$.

Design validation should be performed to verify that the application works as expected.

FIGURE 5: $\overline{MCLR}$ EXTERNAL CIRCUIT



REVISION HISTORY

Rev A Document (7/2003)
First revision of this document. Device Data Sheet Clarification issues 1 (SSP), 2 (Packaging) and 3 (RESET).

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