

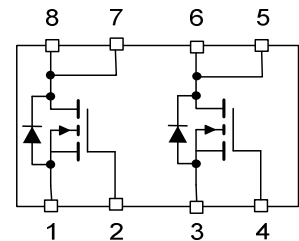
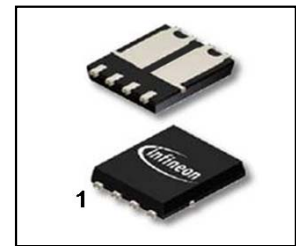
**OptiMOS™-T2 Power-Transistor**

**Features**

- Dual N-channel Normal Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

**Product Summary**

$V_{DS}$	100	V
$R_{DS(on),max}^{3)}$	61	mΩ
$I_D$	16	A

**PG-TDSON-8-10**


Type	Package	Marking
IPG16N10S4-61A	PG-TDSON-8-10	4N1061

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=10\text{ V}$	16	A
		$T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}^{1)}$	11	
Pulsed drain current <sup>1)</sup> one channel active	$I_{D,pulse}$	-	64	
Avalanche energy, single pulse <sup>1,3)</sup>	$E_{AS}$	$I_D=8\text{ A}$	33	mJ
Avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	-	10	A
Gate source voltage	$V_{GS}$	-	±20	V
Power dissipation one channel active	$P_{tot}$	$T_C=25\text{ °C}$	29	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>1)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$	-	-	-	5.2	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	100	-	
		6 cm <sup>2</sup> cooling area <sup>2)</sup>	-	60	-	

**Electrical characteristics, at  $T_j=25^\circ\text{C}$ , unless otherwise specified**

#### Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=9\mu A$	2.0	2.8	3.5	
Zero gate voltage drain current <sup>4)</sup>	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V, T_j=25^\circ\text{C}$	-	0.01	1	$\mu A$
		$V_{DS}=100V, V_{GS}=0V, T_j=125^\circ\text{C}^2)$	-	1	100	
Gate-source leakage current <sup>3)</sup>	$I_{GSS}$	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance <sup>3)</sup>	$R_{DS(on)}$	$V_{GS}=10V, I_D=16A$	-	53	61	m $\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>1)</sup>**

Input capacitance <sup>3)</sup>	$C_{iss}$	$V_{GS}=0V, V_{DS}=25V,$ $f=1MHz$	-	374	490	pF
Output capacitance <sup>3)</sup>	$C_{oss}$		-	120	156	
Reverse transfer capacitance <sup>3)</sup>	$C_{rss}$		-	10	20	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50V, V_{GS}=10V,$ $I_D=16A, R_G=11\Omega$	-	3	-	ns
Rise time	$t_r$		-	1	-	
Turn-off delay time	$t_{d(off)}$		-	5	-	
Fall time	$t_f$		-	5	-	

**Gate Charge Characteristics<sup>1, 3)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=50V, I_D=16A,$ $V_{GS}=0 \text{ to } 10V$	-	2	2.6	nC
Gate to drain charge	$Q_{gd}$		-	1.3	2.6	
Gate charge total	$Q_g$		-	5.4	7	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V

**Reverse Diode**

Diode continuous forward current <sup>1)</sup> one channel active	$I_S$	$T_C=25^\circ C$	-	-	16	A
Diode pulse current <sup>1)</sup> one channel active	$I_{S,pulse}$		-	-	64	
Diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_F=16A,$ $T_j=25^\circ C$	-	1.0	1.3	V
Reverse recovery time <sup>1)</sup>	$t_{rr}$	$V_R=50V, I_F=I_S,$ $di_F/dt=100A/\mu s$	-	50	-	ns
Reverse recovery charge <sup>1, 3)</sup>	$Q_{rr}$		-	70	-	nC

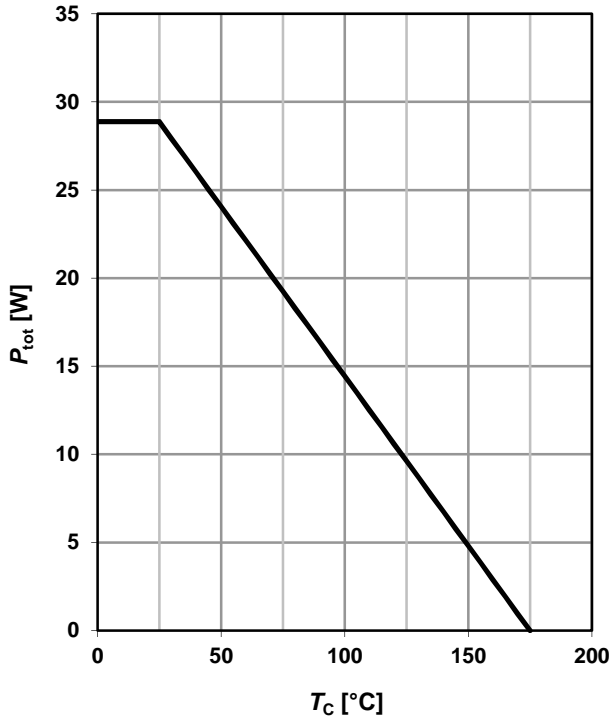
<sup>1)</sup> Specified by design. Not subject to production test.

<sup>2)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

<sup>3)</sup> Per channel

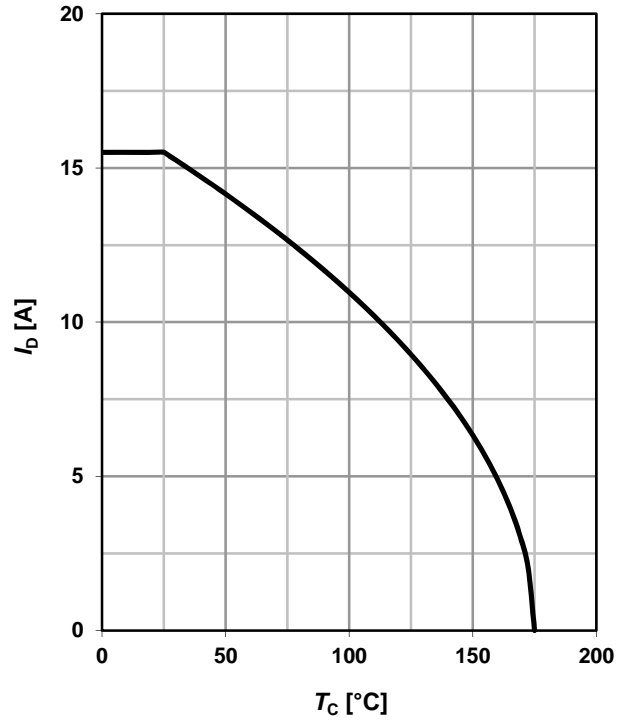
**1 Power dissipation**

$P_{tot} = f(T_C); V_{GS} \geq 6\text{ V}; \text{one channel active}$



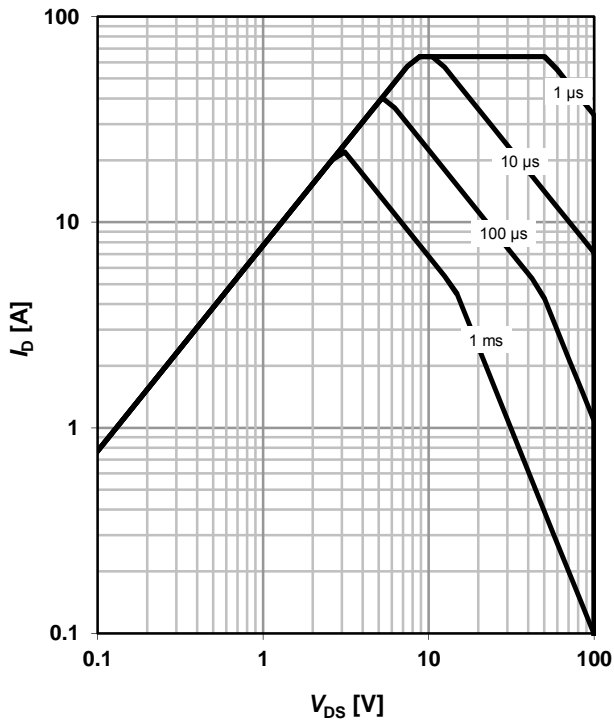
**2 Drain current**

$I_D = f(T_C); V_{GS} \geq 6\text{ V}; \text{one channel active}$



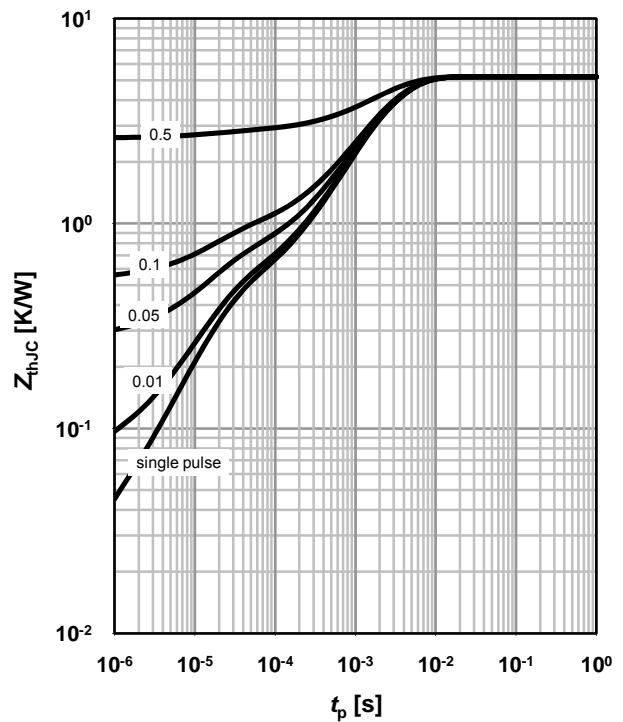
**3 Safe operating area**

$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0; \text{one channel active}$   
parameter:  $t_p$



**4 Max. transient thermal impedance**

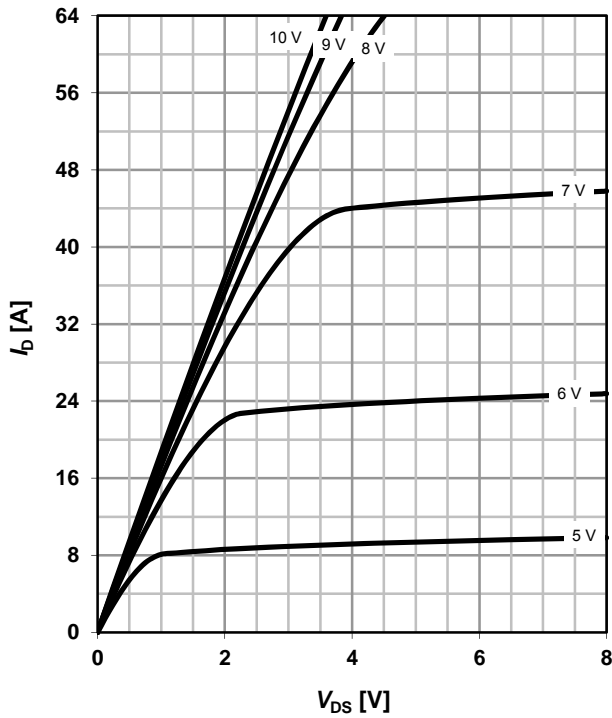
$Z_{thJC} = f(t_p)$   
parameter:  $D = t_p/T$



**5 Typ. output characteristics<sup>5)</sup>**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

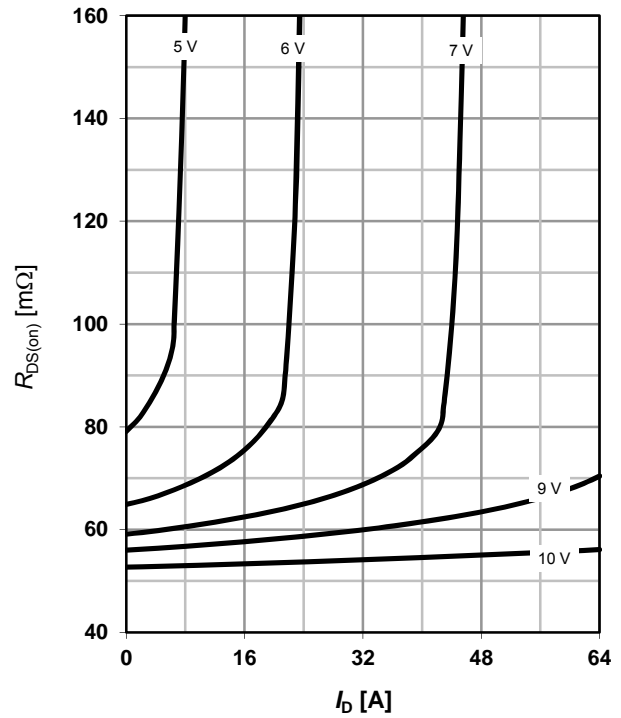
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance<sup>5)</sup>**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

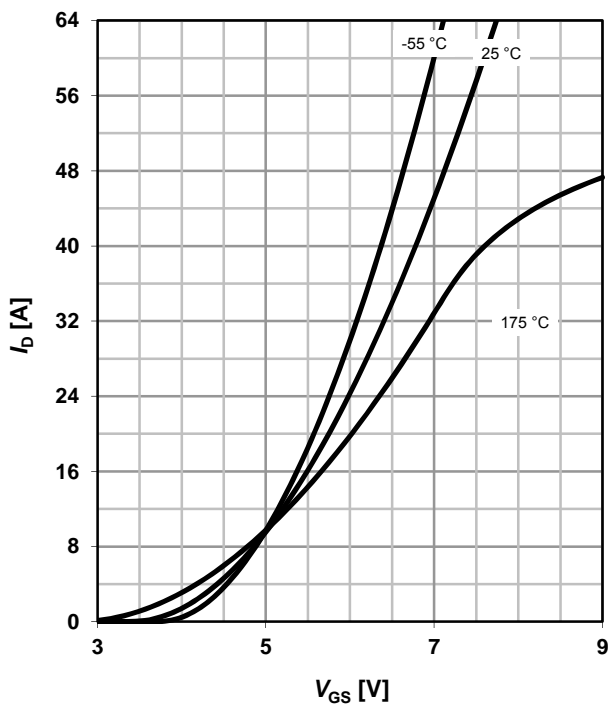
parameter:  $V_{GS}$



**7 Typ. transfer characteristics<sup>5)</sup>**

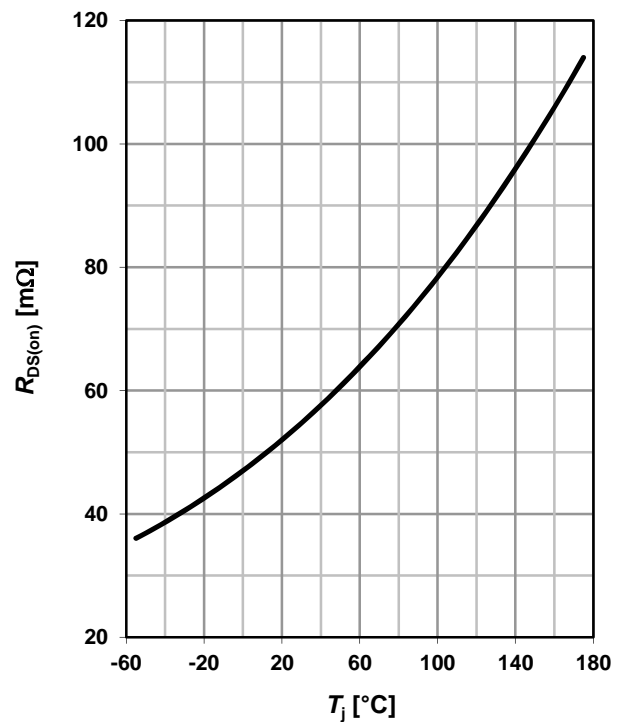
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter:  $T_j$



**8 Typ. drain-source on-state resistance<sup>5)</sup>**

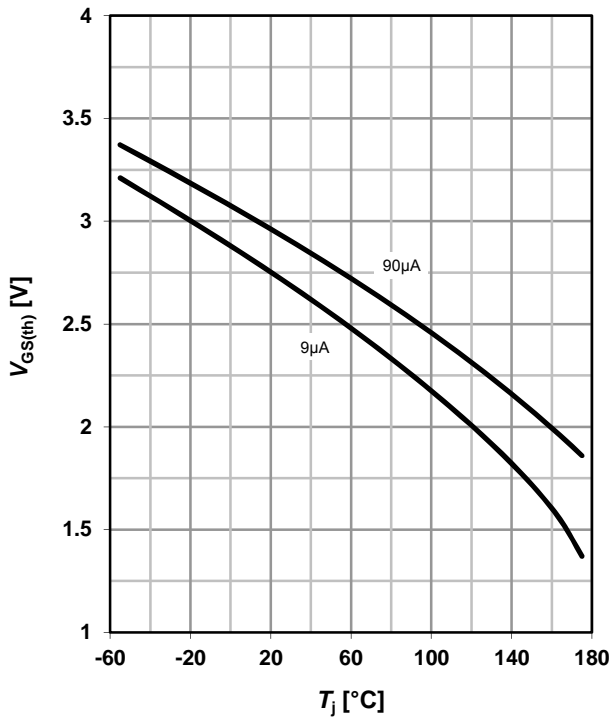
$R_{DS(on)} = f(T_j); I_D = 16\text{ A}; V_{GS} = 10\text{ V}$



**9 Typ. gate threshold voltage**

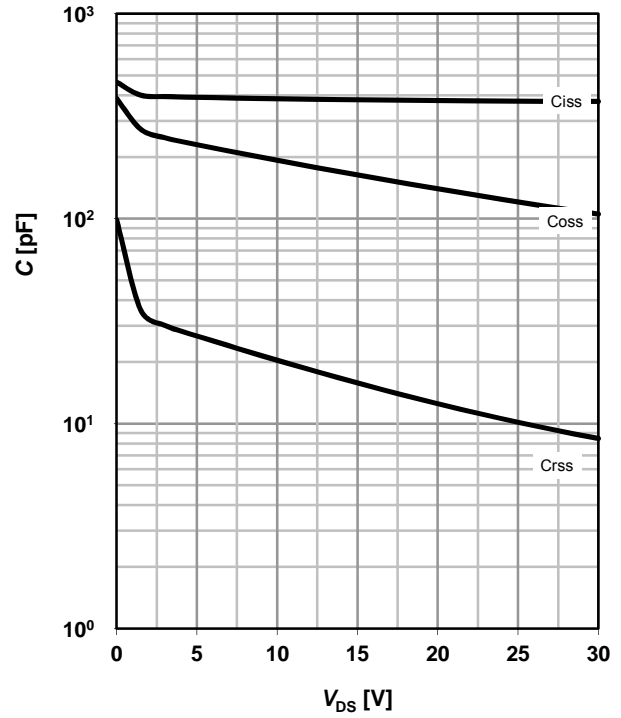
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter:  $I_D$



**10 Typ. Capacitances<sup>5)</sup>**

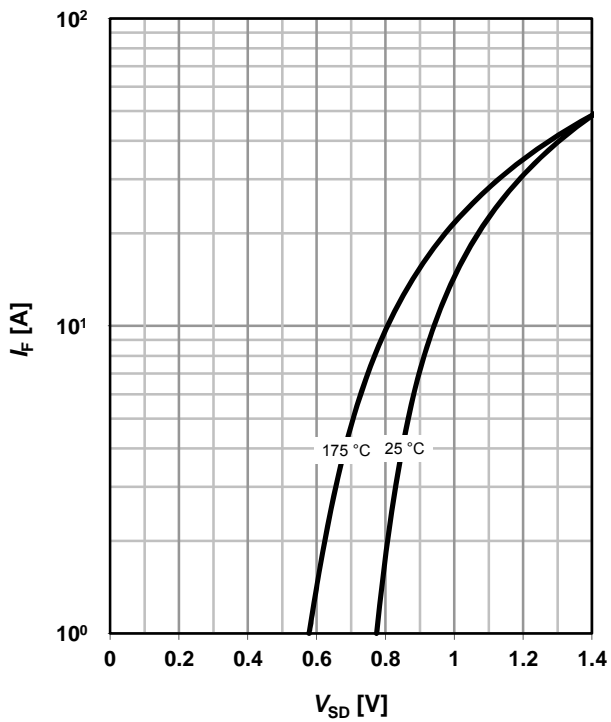
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**11 Typical forward diode characteristics<sup>5)</sup>**

$I_F = f(V_{SD})$

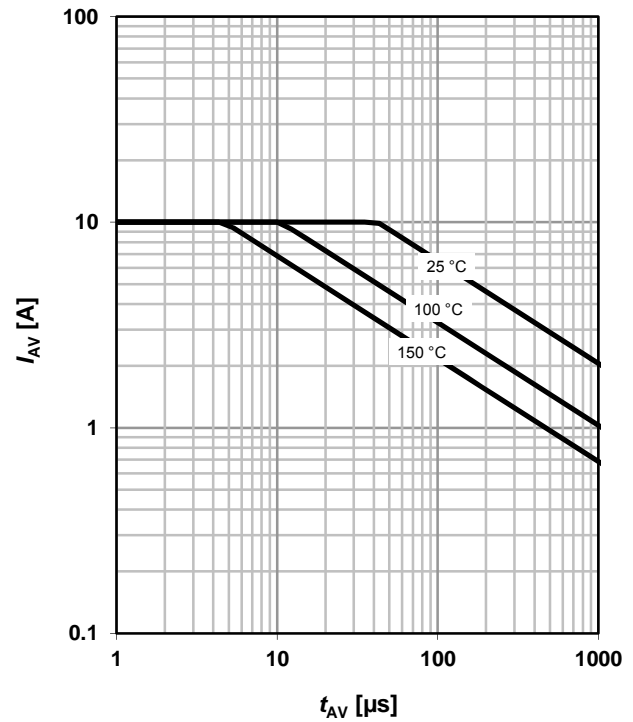
parameter:  $T_j$



**12 Avalanche characteristics<sup>5)</sup>**

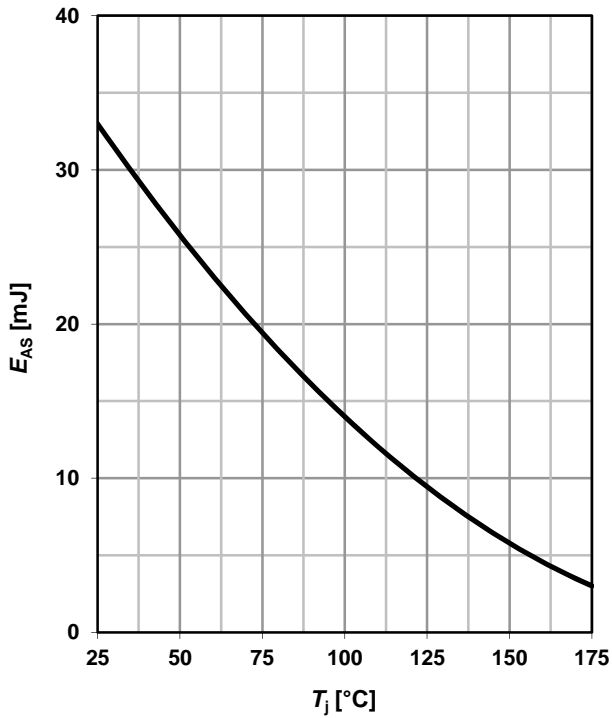
$I_{AS} = f(t_{AV})$

parameter:  $T_{j(start)}$



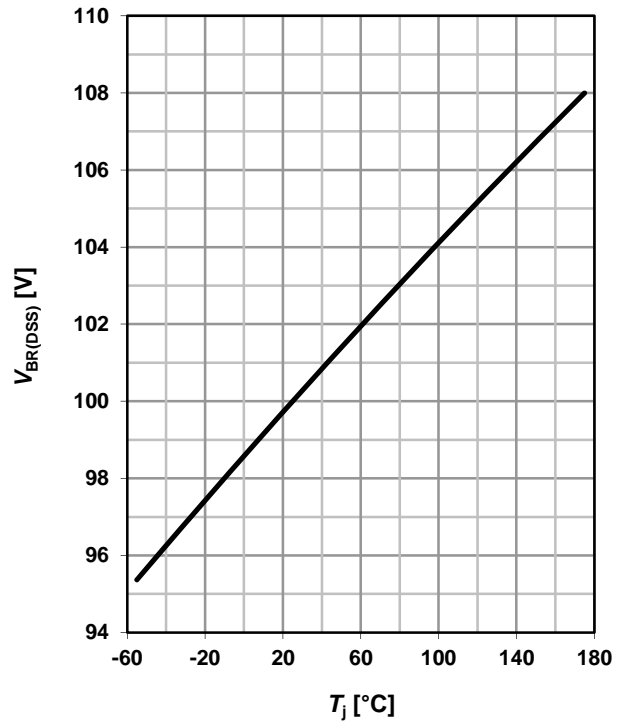
**13 Avalanche energy<sup>5)</sup>**

$E_{AS} = f(T_j), I_D = 8A$



**14 Drain-source breakdown voltage**

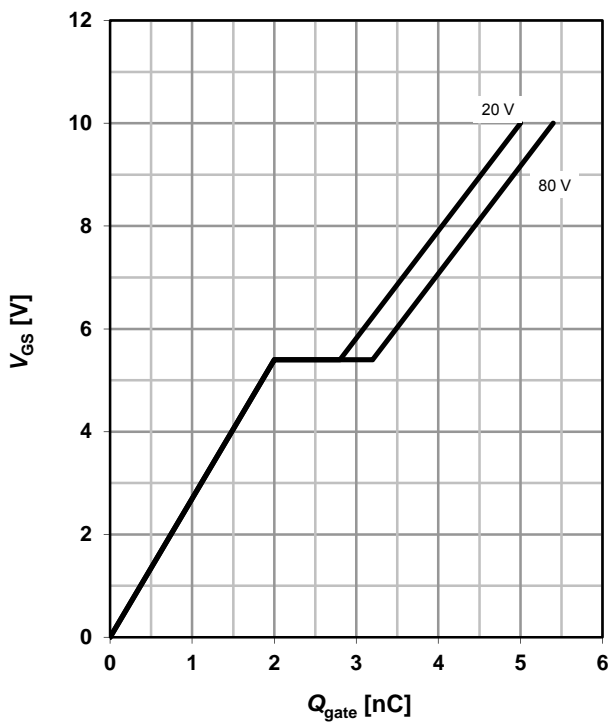
$V_{BR(DSS)} = f(T_j); I_D = 1\text{ mA}$



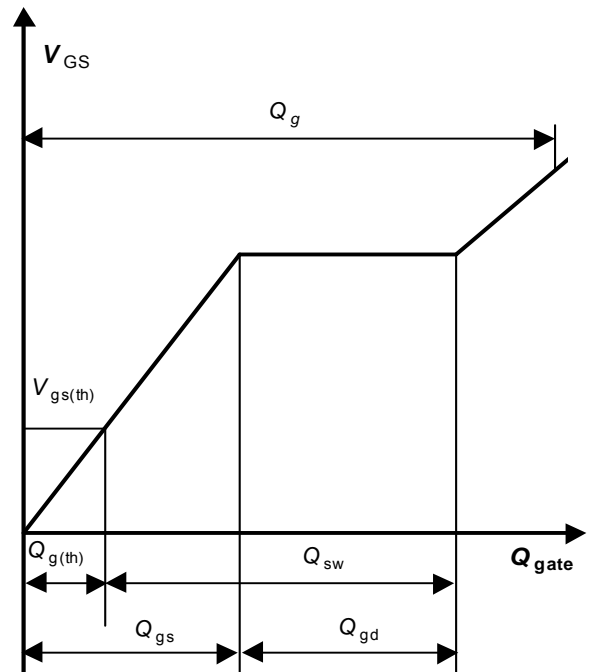
**15 Typ. gate charge<sup>5)</sup>**

$V_{GS} = f(Q_{gate}); I_D = 16\text{ A pulsed}$

parameter:  $V_{DD}$



**16 Gate charge waveforms**



**Published by**  
**Infineon Technologies AG**  
**81726 Munich, Germany**

**© Infineon Technologies AG 2011**  
**All Rights Reserved.**

#### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

#### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### **Warnings**

Due to technical requirements, components may contain dangerous substances.  
For information on the types in question, please contact the nearest Infineon Technologies Office.  
Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life.  
If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.



## Revision History

Version	Date	Changes
Revision 1.0	04.03.2013	Final Data Sheet