CLOCK RECOVERY PLL

MK1575-01

Description

The MK1575-01 is a clock recovery Phase-Locked Loop (PLL) designed for clock synthesis and synchronization in cost sensitive applications. The device is optimized to accept a low-frequency reference clock to generate a high-frequency data or graphics pixel clock. External loop filter components allow tailoring of loop frequency response characteristics. For low jitter / phase noise requirements refer to the MK2069 products.

Features

- Long-term output jitter <2 nsec over 10 µsec period
- External PLL clock feedback path enable “zero delay” I/O clock skew configuration
- Selectable internal feedback divider provides popular telecom and video clock frequencies (see tables below)
- Can optionally use external feedback divider to generate other output frequencies.
- Single 3.3 V supply, low-power CMOS
- Power-down mode and output tri-state (pin $\overline{OE}$)
- Packaged in 16-pin TSSOP
- Available in Pb (lead) free package
- Industrial temperature range available

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Pre-Configured Input/Output Frequency Combinations:

Telecom T/E Clock Modes (rising edge aligned):

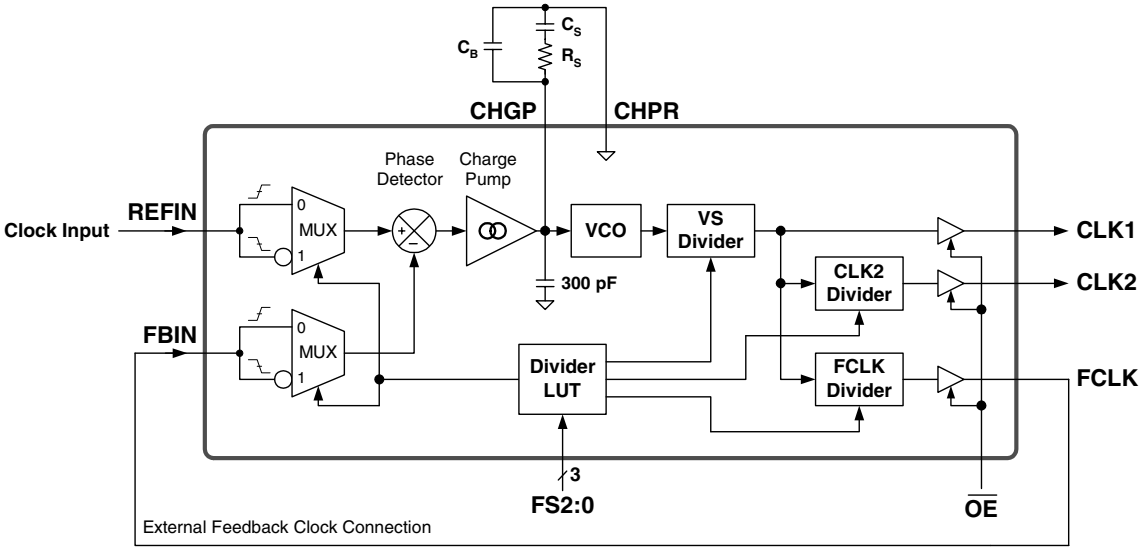
Addr FS2:0	Input Clock	Output Clocks (MHz)		Clock Type
		CLK1	CLK2	
000	8 kHz	3.088	1.544	T1
001	8 kHz	16.384	2.048	E1
010	8 kHz	34.368	17.184	E3
011	8 kHz	44.736	22.368	T3

Video Clock Modes (falling edge aligned):

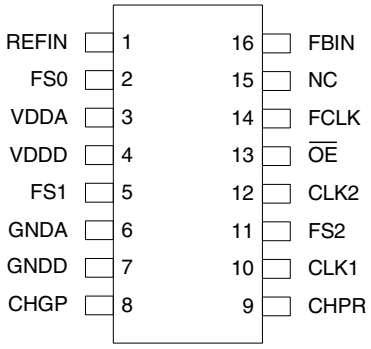
Addr FS2:0	Input Clock (kHz)	Output Clocks (MHz)		Clock Type
		CLK1	CLK2	
100	15.625	54	27	PAL 601
101	15.734	54	27	NTSC 601
110	15.625	35.468	17.734	PAL $4xf_{SC}$
111	15.734	28.636	14.318	NTSC $4xf_{SC}$

Block Diagram

The standard external clock feedback configuration is shown. Use this configuration for the pre-configured input/output frequency combinations listed above.



Pin Assignment



16 pin 4.40 mil body, 0.65 mil pitch TSSOP

Pin Descriptions

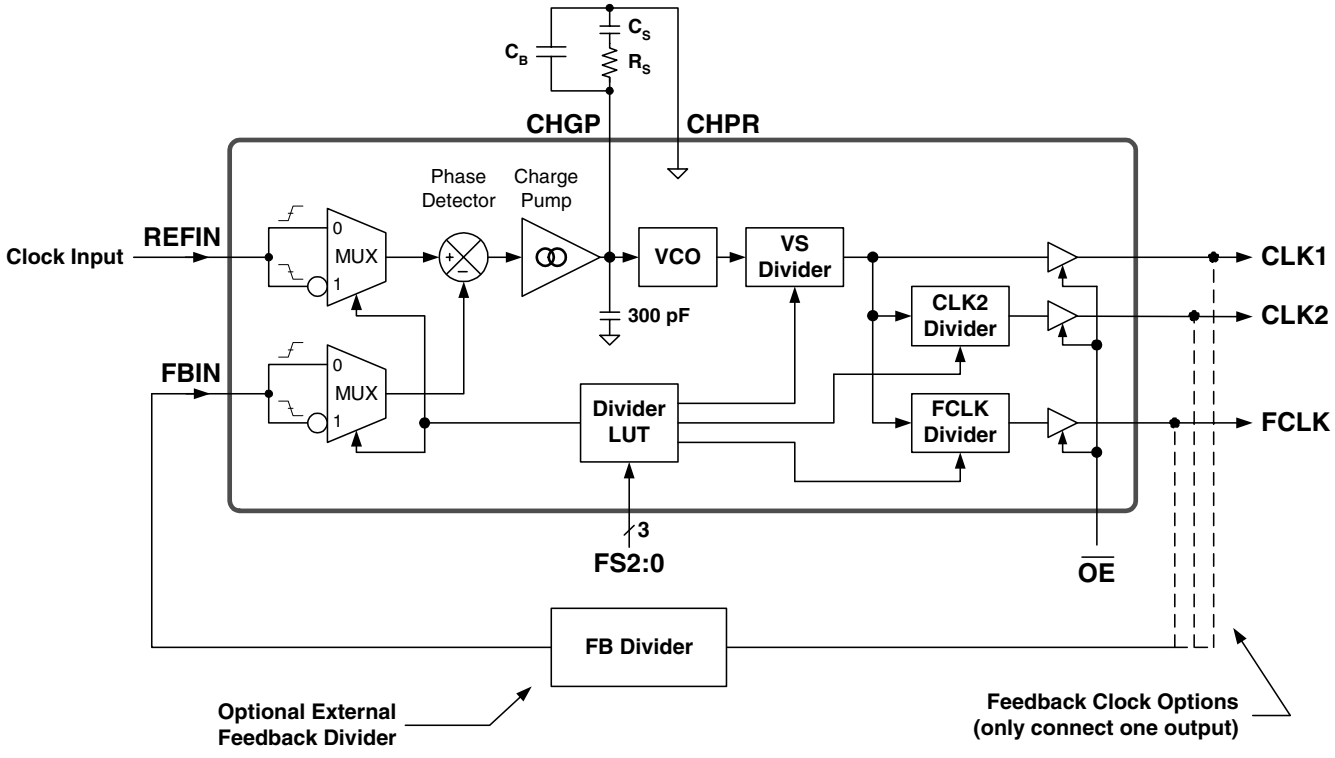
Pin Number	Pin Name	Pin Type	Pin Description
1	REFIN	Input	Reference clock input. Connect the input clock to this pin. Can be Rising or Falling edge triggered as per Detailed Mode Selection Table, page 3.
2	FS0	Input	Frequency Selection Input bit 0, selects internal divider values as per Detailed Mode Selection Table, page 3.
3	VDDA	Power	Power supply connection for internal VCO and other analog circuits.
4	VDDD	Power	Power supply connection for internal digital circuits and output buffers.
5	FS1	Input	Frequency Selection Input bit 1, selects internal divider values as per Detailed Mode Selection Table, page 3.
6	GNDA	Ground	Ground connection for internal VCO and other analog circuits.
7	GNDD	Ground	Ground connection for internal digital circuits and output buffers.
8	CHGP	—	Loop filter connection, active node.
9	CHPR	—	Loop filter connection, reference node. Do not connect to ground.
10	CLK1	Output	Output clock 1.
11	FS2	Input	Frequency Selection Input bit 2, selects internal divider values as per Detailed Mode Selection Table, page 3.
12	CLK2	Output	Output clock 2.
13	$\overline{OE}$	Input	Output Enable, tristates CLK1, CLK2, FCLK and powers down PLL when high. Internal pull-up.
14	FCLK	Output	Feedback clock output, connect to FBIN for the pre-configured frequency combinations listed in the tables on page 1.
15	NC	—	No internal connection, connect to ground.
16	FBIN	Input	Feedback clock input. Connect to CLK1, CLK2, FCLK, or the output of an external feedback divider, depending on application. Refer to document text for more information.

Detailed Mode Selection Table

Refer to this table when not using the standard external clock feedback configuration shown on page 1.

Address FS2:0	Internal Divider Settings			FBIN, REFIN Clock Edge	CLK1 Output Frequency Range
	VS Divider	CLK2 Divider	FCLK Divider		
000	64	2	386	Rising	1.5 - 5 MHz
001	16	8	2048	Rising	6 - 20 MHz
010	8	2	4296	Rising	12 - 40 MHz
011	4	2	5592	Rising	24 - 80 MHz
100	4	2	3456	Falling	24 - 80 MHz
101	4	2	3432	Falling	24 - 80 MHz
110	8	2	2270	Falling	12 - 40 MHz
111	8	2	1820	Falling	12 - 40 MHz

Block Diagram, Showing Device Configuration Options



Functional Description

The MK1575-01 is a PLL (phase-locked loop) based clock generator that generates output clocks synchronized to an input reference clock. The device can be used in the standard configuration as described on page 1, or optionally can use an external divider in the clock feedback path to produce other frequency multiplication factors.

External components are used to control the PLL loop response. The use of external loop components enables a lower PLL loop bandwidth which is needed when accepting low frequency input clocks such as those listed in the tables on page 1.

PLL Clock Feedback Options

FCLK to FBIN

This is the standard configuration that is used for the pre-configured input / output frequency combinations listed on page 1. By including an external divider in the feedback path ("FB Divider" in the Block Diagram of page 3) the output clock frequency can be increased. Refer to the Output Frequency Calculation table below.

CLK1 to FBIN

When no external feedback divider is used, this option configures the device as a zero-delay buffer and the frequency of CLK1 is the same as the input reference clock. Including an external divider in the feedback path will increase the output clock frequency. Refer to the Output Frequency Calculation table below.

CLK2 to FBIN

Like the above configuration, this option configures the device as a zero-delay buffer when no external feedback divider is used, and the frequency of CLK2 is the same as the input reference clock. Including an external divider in the feedback path will increase the output clock frequency. Refer to the Output Frequency Calculation table below.

Frequency and Bandwith Calculations

Feedback Path Option	Output Clock Frequency				
	CLK1	CLK2	FCLK	VCO Frequency	"N" Factor
FCLK to FBIN	$f_{IN} \times FB \times FCLK$	$f_{IN} \times FB \times \frac{FCLK}{CLK2}$	$f_{IN} \times FB$	$f_{IN} \times FB \times FCLK^2 \times VS$	$VS \times FCLK \times FB$
CLK1 to FBIN	$f_{IN} \times FB$	$\frac{f_{IN} \times FB}{CLK2}$	$\frac{f_{IN} \times FB}{FCLK}$	$f_{IN} \times FB \times VS$	$VS \times FB$
CLK2 to FBIN	$f_{IN} \times FB \times CLK2$	$f_{IN} \times FB$	$f_{IN} \times FB \times \frac{CLK2}{FCLK}$	$f_{IN} \times FB \times CLK2^2 \times VS$	$VS \times CLK2 \times FB$

Notes:
1) FB = 1 when no feedback divider is used.
2) Refer to the Detail Mode Selection Table on page 3 for possible divider combinations.
3) The VCO frequency needs to be considered in all applications (see table below).
4) The external loop filter also needs to be considered.
5) Minimum VCO frequency = 96 MHz.
6) Maximum VCO frequency = 320 MHz.
7) To minimize output jitter, use the highest possible VCO frequency allowed by the application.

Setting PLL Loop Bandwidth and Damping Factor

The frequency response of the MK1575-01 PLL may be approximated by the following equation:

$$\text{Normalized PLL Bandwidth} = \frac{(R_S \cdot K_O \cdot I_{CP})}{2\pi \cdot N}$$

The associated damping factor is calculated as follows:

$$\text{Damping factor, } \zeta = \frac{R_S}{2}\sqrt{\frac{K_O \cdot I_{CP} \cdot C_S}{N}}$$

Where:

K_O = VCO gain in Hz/Volt (use 340 MHz/V)

I_{cp} = Charge pump current, 12.5 µA

N = Total feedback divide from VCO, (Refer to N Value table, below)

C_S = External loop filter capacitor in Farads

R_S = Loop filter resistor in Ohms

The above bandwidth equation calculates the “normalized” loop bandwidth which is approximately equal to the - 3dB bandwidth. This approximate calculation does not take into account the effects of damping factor or the third pole imposed by C_P. It does, however, provide a useful approximation of filter performance.

To prevent jitter on the output clocks due to modulation of the PLL by the input reference frequency, the following general rule should be observed:

$$\text{PLL Bandwidth} \leq \frac{f_{\text{Phase Detector}}}{20}$$

In general, the loop damping factor should be 0.7 or greater to ensure output stability. For video applications, a low damping factor (0.7 to 1.0) is generally desired for fast genlocking. For telecom applications, a higher damping factor is usually desirable. A higher damping factor will create less passband gain peaking which will minimize the gain of network clock wander amplitude. A higher damping factor may also increase output clock jitter when there is excess digital noise in the system application, due to the reduced ability of the PLL to respond to, and therefore compensate for, phase noise ingress.

Notes on setting the value of C_P

As another general rule, the following relationship should be maintained between components C1 and C2 in the external loop filter:

$$C_P = \frac{C_S}{20}$$

Where:

$$C_P = C_B + 300\ \text{pF}$$

C_B = External bypass capacitor in Farads

Note that the MK1575-01 contains an internal 300 pF filter cap which is connected in parallel with external device C_B. This helps to reduce output clock jitter. In some applications external device C_B will not be required.

C_P establishes a second pole in the PLL loop filter. For higher damping factors (>1), calculate the value of C_P based on a C_S value that would be used for a damping factor of 1. This will minimize baseband peaking and loop instability that can lead to output jitter.

C_P also helps to damp VCO input voltage modulation caused by the charge pump correction pulses. A C_P value that is too low will result in increased output phase noise at the phase detector frequency due to this. In extreme cases where input jitter is high, charge pump current is high, and C_P is too small, the VCO input voltage can hit the supply or ground rail resulting in non-linear loop response.

The best way to set the value of C_P is to use the External Loop Filter Solver located on the IDT web site.

Loop Filter Capacitor Type

Clock Jitter and input-to-output skew performance of the MK1575-01 can be affected by loop filter capacitor type. Cost vs. performance trade-offs can be made when choosing capacitor types. Performance differences are best determined through experimentation.

Recommended capacitors can be found at http://www.icst.com/products/telecom/

Example Loop Filter Component Values for Pre-Configured Frequency Combinations Listed on Page 1.

Addr	Input Frequency	Output Frequency (MHz)		N Factor	R_S	C_S	C_B	Loop BW (-3dB)	Loop Damp	Passband Peaking	Notes
		CLK1	CLK2								
000	8 kHz	3.088	1.544	24704	15 kΩ	1 µF	2.2 nF	363 Hz	2.5	0.19 dB	1
000	8 kHz	3.088	1.544	24704	6.8 kΩ	10 µF	4.7 nF	199 Hz	4.46	0.06 dB	2
001	8 kHz	16.384	2.048	32768	18 kΩ	1 µF	2.2 nF	425 Hz	3.24	0.12 dB	1
001	8 kHz	16.384	2.048	32768	8.2 kΩ	10 µF	4.7 nF	181 Hz	4.67	0.05 dB	2
010	8 kHz	34.368	17.184	34368	18 kΩ	1 µF	2.2 nF	405 Hz	3.16	0.13 dB	1
010	8 kHz	34.368	17.184	34368	8.2 kΩ	10 µF	4.7 nF	173 Hz	4.56	0.06 dB	2
011	8 kHz	44.736	22.368	22368	12 kΩ	1 µF	1 nF	390 Hz	2.62	0.17 dB	1
011	8 kHz	44.736	22.368	22368	6.8 kΩ	10 µF	4.7 nF	219 Hz	4.69	0.05 dB	2
100	15.625 kHz	54	27	13824	10 kΩ	0.068 µF	3.3 nF	758 Hz	0.72	2.16 dB	3
101	15.734 kHz	54	27	13728	10 kΩ	0.068 µF	3.3 nF	760 Hz	0.73	2.15 dB	3
110	15.625 kHz	35.468	17.734	18160	10 kΩ	0.068 µF	3.3 nF	760 Hz	0.73	2.15 dB	3
111	15.734 kHz	28.636	14.318	14560	10 kΩ	0.068 µF	4.7 nF	721 Hz	0.7	2.42 dB	3

Notes:

1) This loop filter selection is optimized for cost and component size. It provides stable clock outputs and moderate input reference jitter attenuation. This configuration could be used when producing an internal system clock, one which will not be used as a data transmit clock when locked to a recovered data clock.

2) This loop filter selection is optimized for low pass-band peaking. This configuration should be used when generating data transmit clock that is locked to a recovered data clock. This will ensure that the data clock conforms with Belcore GR-1244-CORE wander transfer specifications.

3) A loop bandwidth of 700 Hz and damping factor of 0.7 is typical for video genlock applications. This combination assures minimal Hsync frequency modulation of the pixel clock yet genlocking.

4) Example vendors and part numbers for above capacitor selections:

0.15 µF Panasonic ECP-U1C154MA5 (SMT film type, 1206 size, available from DigiKey)

0.68 µF	Panasonic ECP-U1C684MA5 (SMT film type, 1206 size, available from DigiKey)
10 µF	MuRata GRM42-2X5R106K10
10 nF	Panasonic ECH-U1C103JB5 (SMT film type, 805 size, available from DigiKey)
33 nF	Panasonic ECH-U1C333JB5 (SMT film type, 1206 size, available from DigiKey)

Input-to-Output Skew Induced by Loop Filter Leakage

Leakage across the loop filter, due to PCB contamination or poor quality loop filter capacitors, can increase input-to-output clock skew error. Concern regarding input-to-output skew error is usually limited to “zero delay” configurations, where CLK1 or CLK2 is directly connected to FBIN. In sever cases of loop filter leakage, however, output clock jitter can also be increased.

The capacitors C_S and C_P in the external loop filter maintain the VCO frequency control voltage between charge pump pulses, which by design coincide with phase detector events. VCO frequency or phase adjustments are made by these charge pump pulses, pumping current into (or out of) the external loop filter capacitors to adjust the VCO control voltage as needed. Like the capacitors, the CHGP pin (pin 8) is a high-impedance PLL node; the charge pump is a current source, which is high impedance by definition, and the VCO input is also high impedance.

During normal (locked) operation, in the event of current leakage in the loop filter, the charge pump will need to deliver equal and opposite charge in the form of longer charge pump pulses. The increased length of the charge pump pulse will be translated directly to increased input-to-output clock skew. This can also result in higher output jitter due to higher reference clock feedthrough (where the reference clock is f_{REFIN}), depending on the loop filter attenuation characterisitcs.

The Input-to-Output skew parameters in the DC Electrical Specifications assume minimal loop filter leakage. Additional skew due to loop filter leakage may be calculated as follows:

$$\text{Leakage Induced I/O Skew (sec)} = \frac{I_{Leakage}}{I_{CP} \times F_{REFIN}}$$

Avoiding PLL Lockup

In some applications, the MK1575-01 VCO can “lock up” at it’s maximum operating frequency. To avoid this problem observe the following rules:

1) Do not open the clock feedback path with the MK1575-01 enabled. If the MK1575-01 is enabled and does not get a feedback clock into pin FBIN, the output frequency will be forced to the maximum value by the PLL.

If an external divider is in the feedback path and it has a delay before becoming active, hold the $\overline{OE}$ pin high until the divider is ready to work. This could occur, for example, if the divider is implemented in a FPGA.

Holding $\overline{OE}$ high powers down the MK1575-01 and dumps the charge off the loop filter.

2) If an external divider is used in the feedback path, use a circuit that can operate well beyond the intended output clock frequency.

Power Supply Considerations

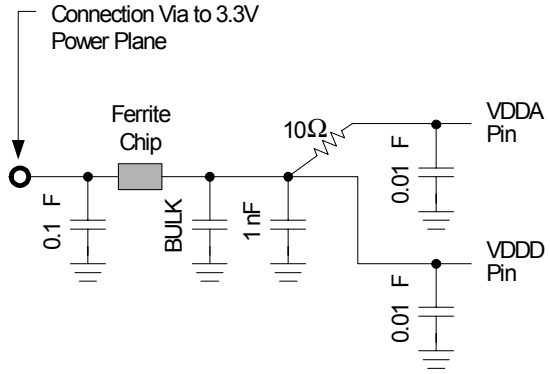
As with any integrated clock device, the MK1575-01 has a special set of power supply requirements:

- The feed from the system power supply must be filtered for noise that can cause output clock jitter. Power supply noise sources include the system switching power supply or other system components. The noise can interfere with device PLL components such as the VCO or phase detector.
- Each VDD pin must be decoupled individually to prevent power supply noise generated by one device circuit block from interfering with another circuit block.
- Clock noise from device VDD pins must not get onto the PCB power plane or system EMI problems may result.

This above set of requirements is served by the circuit illustrated in the Optimum Power Supply Connection, below. The main features of this circuit are as follows:

- Only one connection is made to the PCB power plane.
- The capacitors and ferrite chip (or ferrite bead) on the common device supply form a lowpass 'pi' filter that remove noise from the power supply as well as clock noise back toward the supply. The bulk capacitor should be a tantalum type, 1 µF minimum. The other capacitors should be ceramic type.
- The power supply traces to the individual VDD pins should fan out at the common supply filter to reduce interaction between the device circuit blocks.
- The decoupling capacitors at the VDD pins should be ceramic type and should be as close to the VDD pin as possible. There should be no vias between the decoupling capacitor and the supply pin.

Optimum Power Supply Connection



Series Termination Resistor

Output clock PCB traces over 1 inch should use series termination to maintain clock signal integrity and to reduce EMI. To series terminate a 50Ω trace, which is a commonly used PCB trace impedance, place a 33Ω resistor in series with the clock line as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following printed circuit board layout recommendations should be observed.

1) Each 0.01µF power supply decoupling capacitor should be mounted as close to the VDD pin as possible. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite chip and bulk decoupling from the device is less critical.

2) The loop filter components (R_Z, C_S and C_B) must also be placed close to the CHGP and VIN pins. C_B should be closest to the device. Coupling of noise from other system signal traces should be minimized by keeping traces short and away from active signal traces. Use of vias should be avoided.

3) To minimize EMI the 33Ω series termination resistor, if needed, should be placed close to the clock output.

4) Because each input selection pin includes an internal pull-up device, those inputs requiring a logic high state ("1") can be left unconnected. The pins requiring a logic low state ("0") can be grounded.

Loss of Reference Clock

If a loss occurs on the REFIN clock, the output frequency will decrease at a rate of

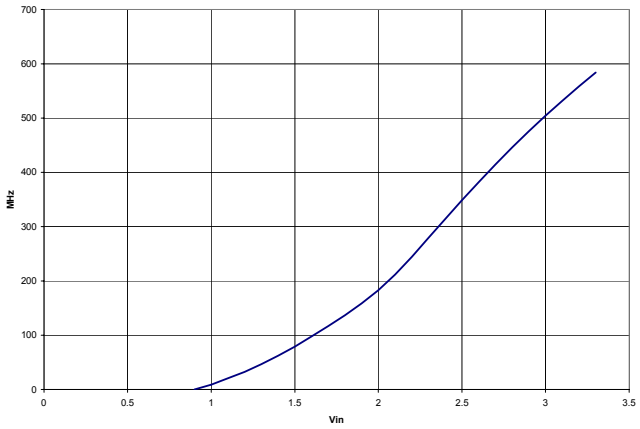
$$\frac{df}{dt} = \frac{4250}{C \times VS} \quad \text{Hz/s}$$

where:
C = C1 + C2
VS = value of VS divider (from the table on page 3)

If the input is held low, the output will stop high or low, or might toggle at several Hz.

Low Frequency Operation

The output frequency can be extended below 1.5 MHz by adding a divider in the output path. In this configuration, it is desirable to take the feedback signal from CLK1 rather than the output of the divider. However, if zero delay operation is required, the feedback signal must come from the divider output.



MK1575-01 Typical VCO Transfer Curve

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the MK1575-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature (industrial version)	-40 to +85° C
Ambient Operating Temperature (commercial version)	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (industrial version)	-40		+85	°C
Ambient Operating Temperature (commercial version)	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Supply Current	IDD	Clock outputs unloaded, VDD = 3.3 V		10		mA
Supply Current in Power Down	I_{DD}	$\overline{OE}$ = VDD		100		µA
Charge Pump Current	I_{CP}			12.5		µA
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	V_{IH} = VDD	-10		+10	µA
Input Low Current	I_{IL}	V_{IL} = 0	-10		+10	µA
Input Capacitance, except X1	C_{IN}			7		pF
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output High Voltage	V_{OH}	I_{OH} = -8 mA CLK1, CLK2	2.0			V
		I_{OH} = -4 mA FCLK	2.0			V
Output Low Voltage	V_{OL}	I_{OL} = 8 mA CLK1, CLK2			0.4	V
		I_{OL} = 4 mA FCLK			0.4	V
Short Circuit Current	I_{OS}	CLK1, CLK2		±43		mA
		FCLK		±18		mA
Nominal Output Impedance	Z_{OUT}			20		Ω

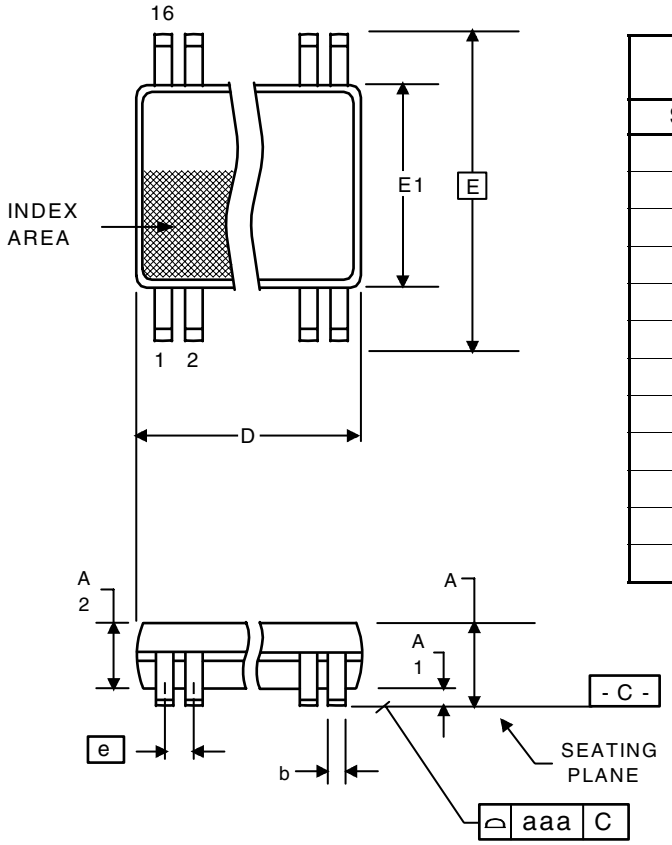
AC Electrical Characteristics

Unless stated otherwise, VDD = 3.3V ±5%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency (into pins REFIN or FBIN)	f_{REF}				20	MHz
Internal VCO Frequency	f_{VCO}		96		320	MHz
Output Frequency	f_{CLK}				80	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V		.6	1.1	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V		.6	1.1	ns
Output Clock Duty Cycle	t_{DC}	At VDD/2	45	50	55	%
Jitter, Absolute Peak-to-peak	t_J	Single cycle measurement; Deviation from mean		150		ps
Long Term Timing Jitter, pk-pk	t_{JLT}	10 µS trigger delay		1.7	3.0	ns
VCO Gain	K_O			340		MHz/V

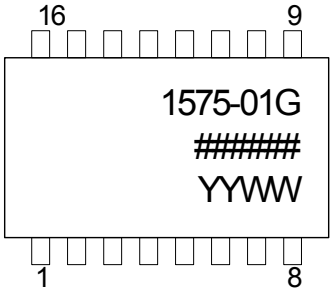
Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95, MO-153

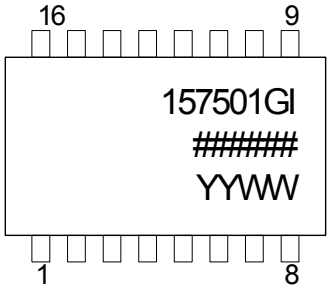


	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°
aaa	--	0.10	--	0.004

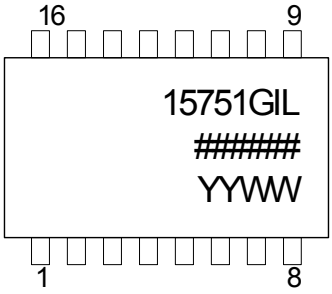
Marking Diagram (commercial)



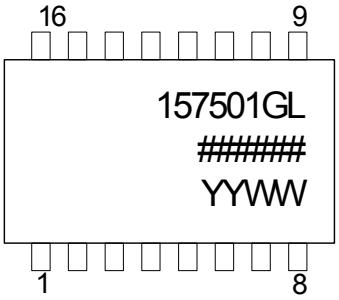
Marking Diagram (industrial)



Marking Diagram (Pb free, industrial)



Marking Diagram (Pb free, commercial)



Notes:

1. ###### is the lot number.
2. YYWW is the last two digits of the year and the week number that the part was assembled.
3. “L” designates Pb (lead) free package.
4. “I” designates industrial temperature grade.
5. Bottom marking: (origin). Origin = country of origin of not USA.

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
MK1575-01G*	see Marking Diagrams above	Tubes	16-pin TSSOP	0 to + 70° C
MK1575-01GTR*		Tape and Reel	16-pin TSSOP	0 to + 70° C
MK1575-01GLF		Tubes	16-pin TSSOP	0 to + 70° C
MK1575-01GLFTR		Tape and Reel	16-pin TSSOP	0 to + 70° C
MK1575-01GI*		Tubes	16-pin TSSOP	-40 to + 85° C
MK1575-01GITR*		Tape and Reel	16-pin TSSOP	-40 to + 85° C
MK1575-01GILF		Tubes	16-pin TSSOP	-40 to + 85° C
MK1575-01GILFTR		Tape and Reel	16-pin TSSOP	-40 to + 85° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

Parts that are ordered with a "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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