



# STN3PF06

## P-CHANNEL 60V - 0.18Ω - 3A SOT-223 STripFET™ II POWER MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STN3PF06	60 V	< 0.20 Ω	2.5 A

- TYPICAL R<sub>DS(on)</sub> = 0.18 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED

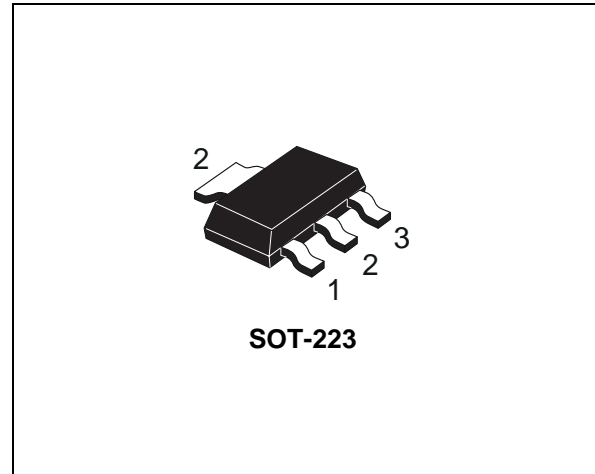
### DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility

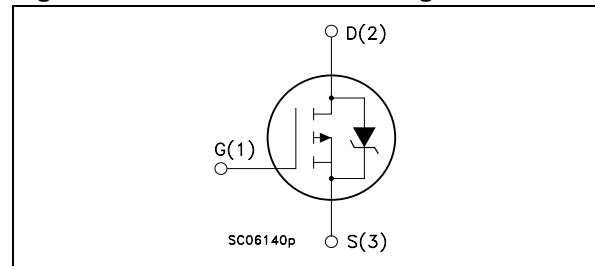
### APPLICATIONS

- DC-DC & DC-AC CONVERTERS
- DC MOTOR CONTROL (DISK DRIVES, etc.)

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STN3PF06	N3PF06	SOT-223	TAPE REEL

**Table 3: ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	60	V
V <sub>GS</sub>	Gate- source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	2.5	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	1.5	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	10	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W
	Derating Factor	0.02	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	6	V/ns
E <sub>AS</sub> (2)	Single Pulse Avalanche Energy	558	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 150	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

- (●) Pulse width limited by safe operating area.  
 (1) I<sub>SD</sub> ≤ 3A, di/dt ≤ 350A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>  
 (2) Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 3A, V<sub>DD</sub> = 25V

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

## STN3PF06

**Table 4: THERMAL DATA**

Rthj-pcb	Thermal Resistance Junction-PCB(1 inch <sup>2</sup> copper board)*	38	°C/W
Rthj-pcb	Thermal Resistance Junction-PCB (min. footprint)*	100	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	260	°C

(\*) When Mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

## ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

**Table 5: OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20V			±100	nA

**Table 6: ON (5)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	2		4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 1.25 A		0.18	0.20	Ω

**Table 7: DYNAMIC**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (5)	Forward Transconductance	V <sub>DS</sub> = 15 V I <sub>D</sub> = 1.25 A		1.5		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V f = 1 MHz V <sub>GS</sub> = 0		850		pF
C <sub>oss</sub>	Output Capacitance			230		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			75		pF

**ELECTRICAL CHARACTERISTICS** (continued)

**Table 8: SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30\text{ V}$ $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure )		20 40		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 48\text{ V}$ $I_D = 12\text{ A}$ $V_{GS} = 10\text{ V}$		16 4.0 6.0	21	nC nC nC

**Table 9: SWITCHING OFF**

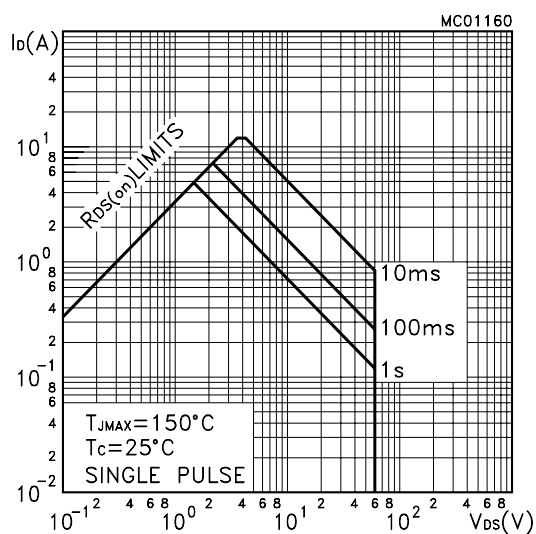
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 30\text{ V}$ $I_D = 6\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		40 17		ns ns

**Table 10: SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$ (1)	Source-drain Current Source-drain Current (pulsed)				2.5 10	A A
$V_{SD}$ (2)	Forward On Voltage	$I_{SD} = 2.5\text{ A}$ $V_{GS} = 0$			1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 12\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		100 260 5.2		ns $\mu\text{C}$ A

(1) Pulse width limited by safe operating area.  
(2) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %.

**Figure 3: Safe Operating Area**



**Figure 4: Thermal Impedance**

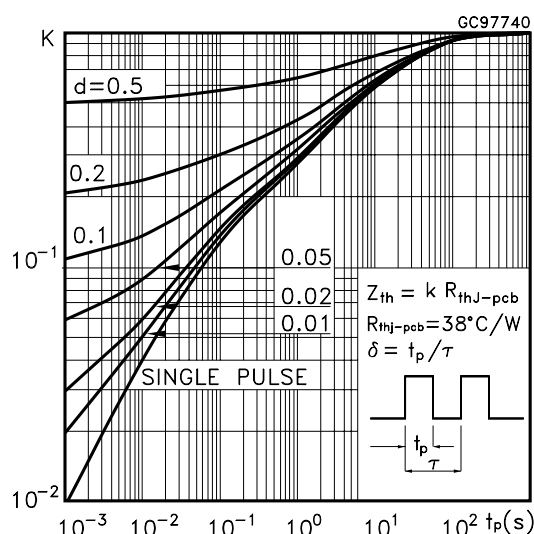


Figure 5: Output Characteristics

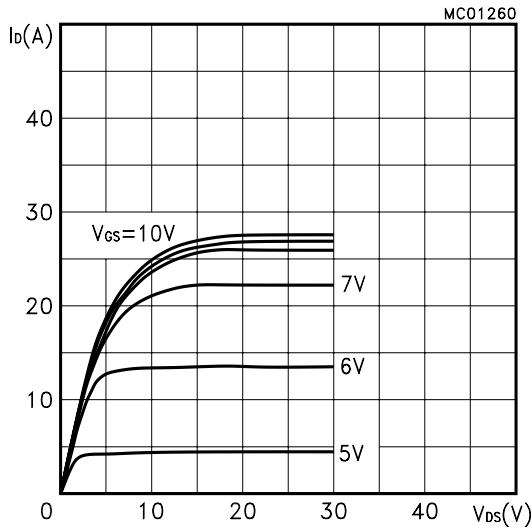


Figure 6: Transfer Characteristics

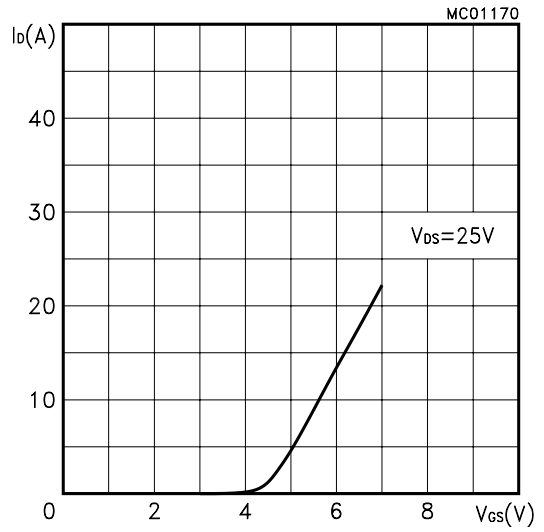


Figure 7: Transconductance

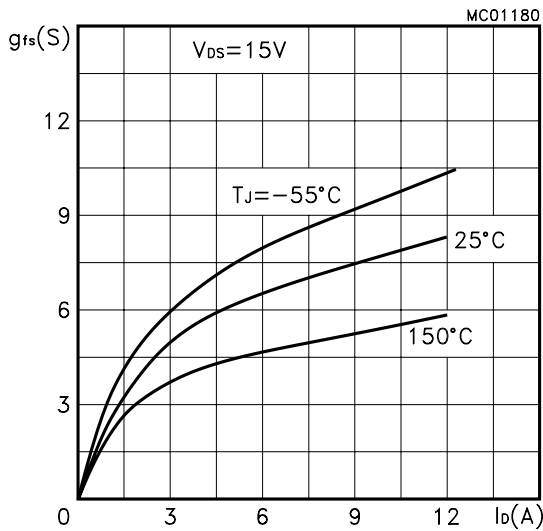


Figure 8: Static Drain-source On Resistance

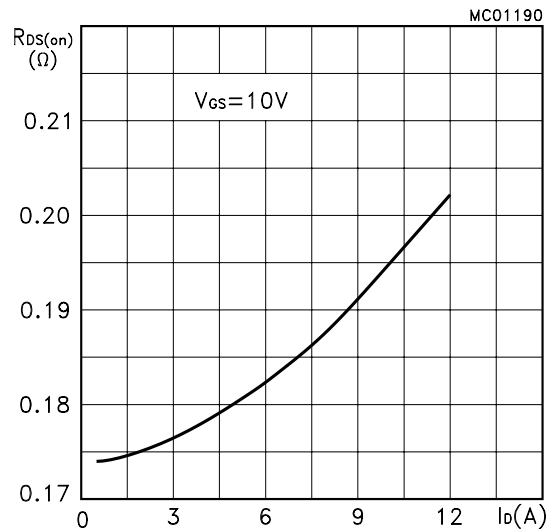


Figure 9: Gate Charge vs Gate-source Voltage

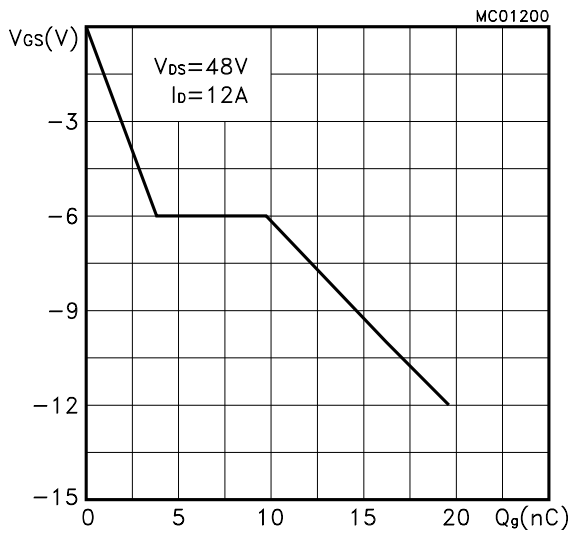
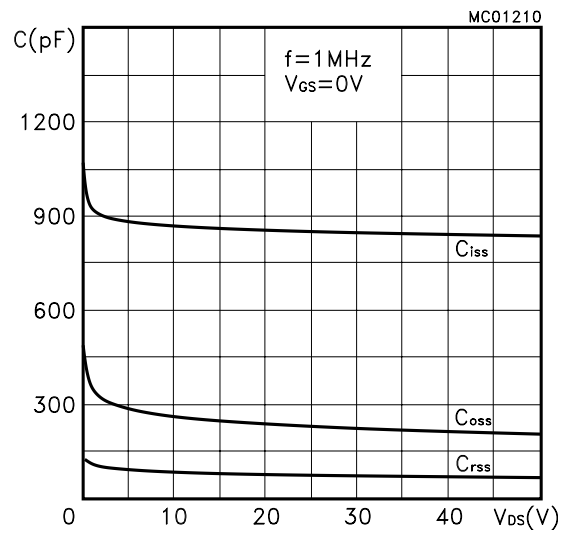
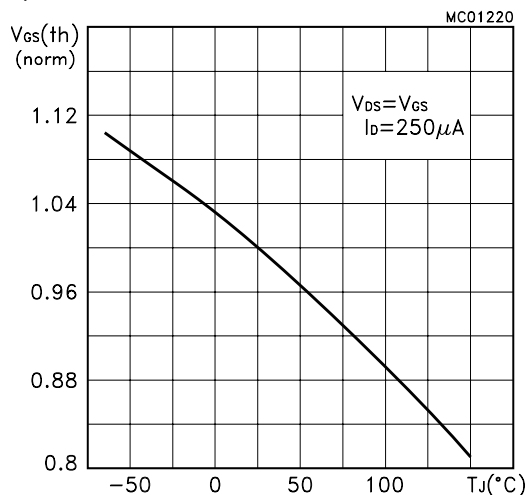


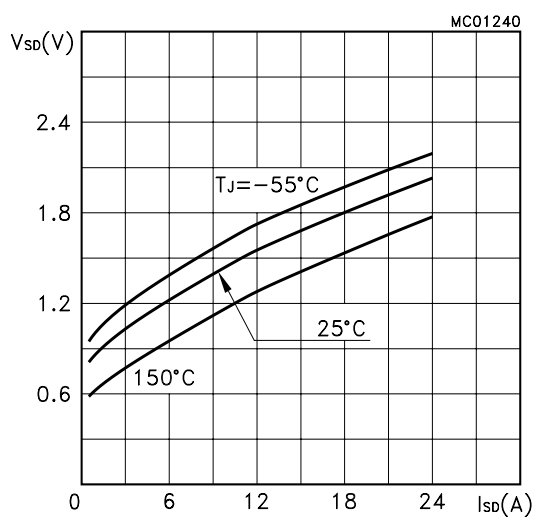
Figure 10: Capacitance Variations



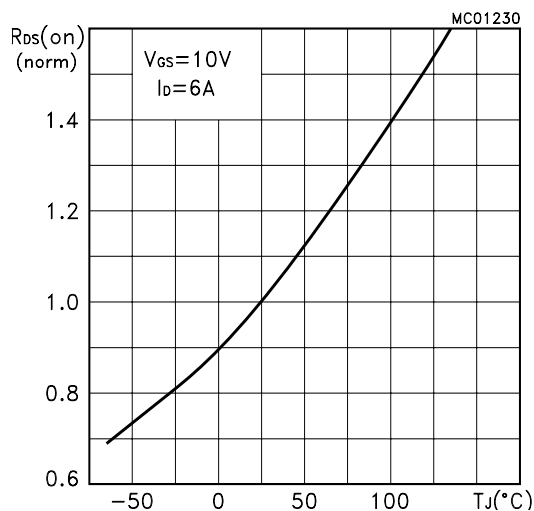
**Figure 11:** Normalized Gate Threshold Voltage vs Temperature



**Figure 13:** Source-drain Diode Forward Characteristics



**Figure 12:** Normalized on Resistance vs Temperature



**Figure 14:** Normalized Breakdown Voltage vs Temperature.

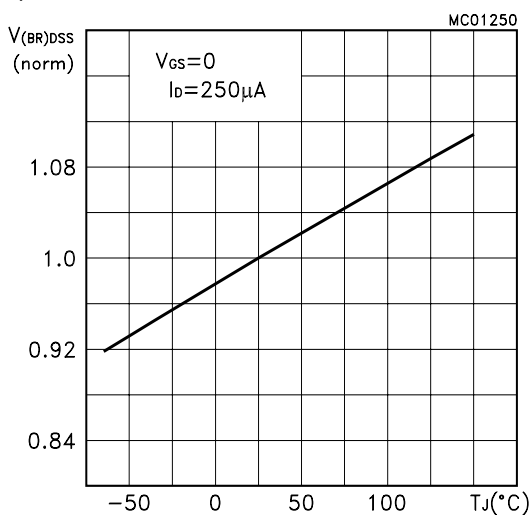


Figure 15: Unclamped Inductive Load Test Circuit

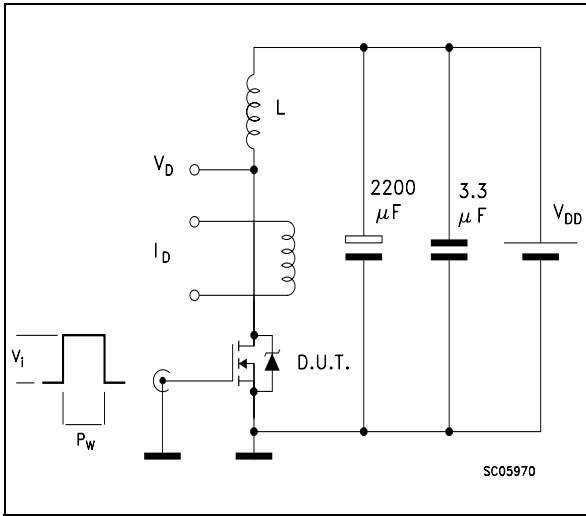


Figure 16: Unclamped Inductive Waveform

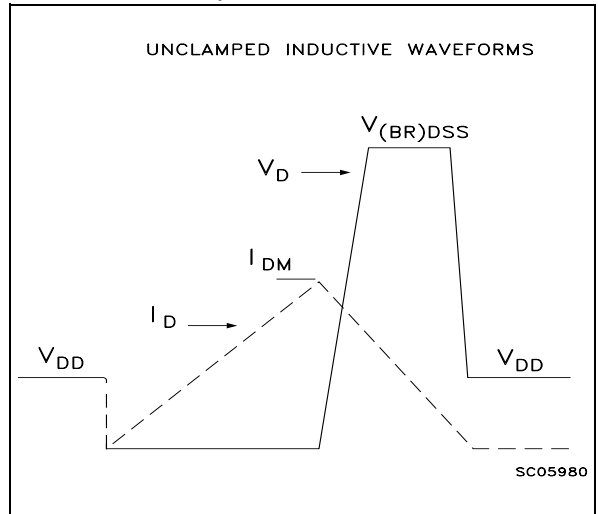


Figure 17: Switching Times Test Circuits For Resistive Load

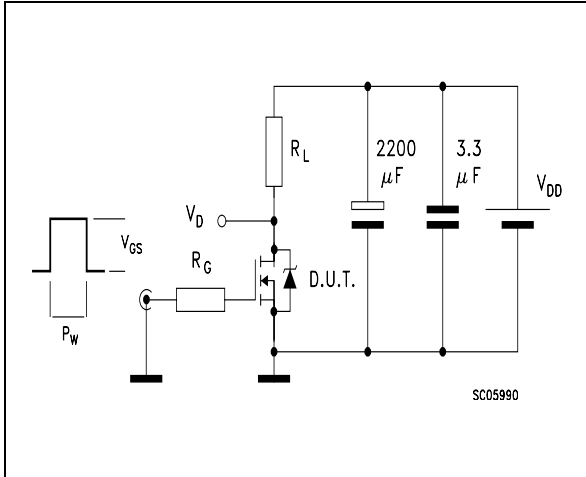


Figure 18: Gate Charge test Circuit

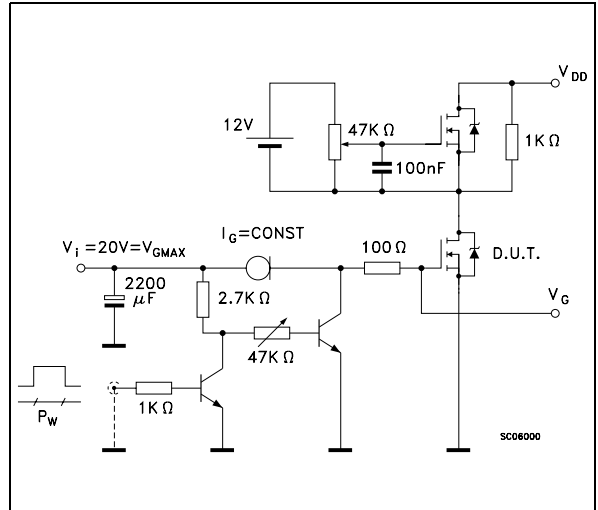
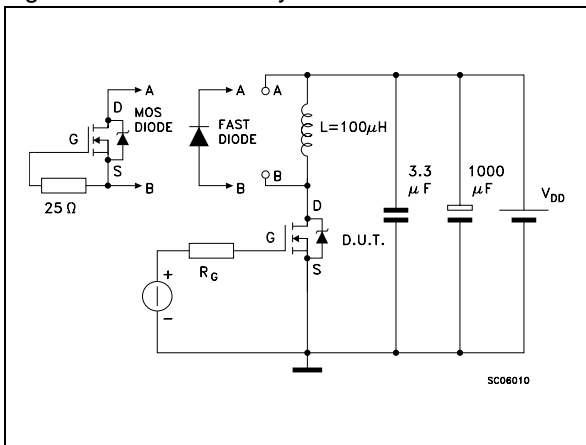
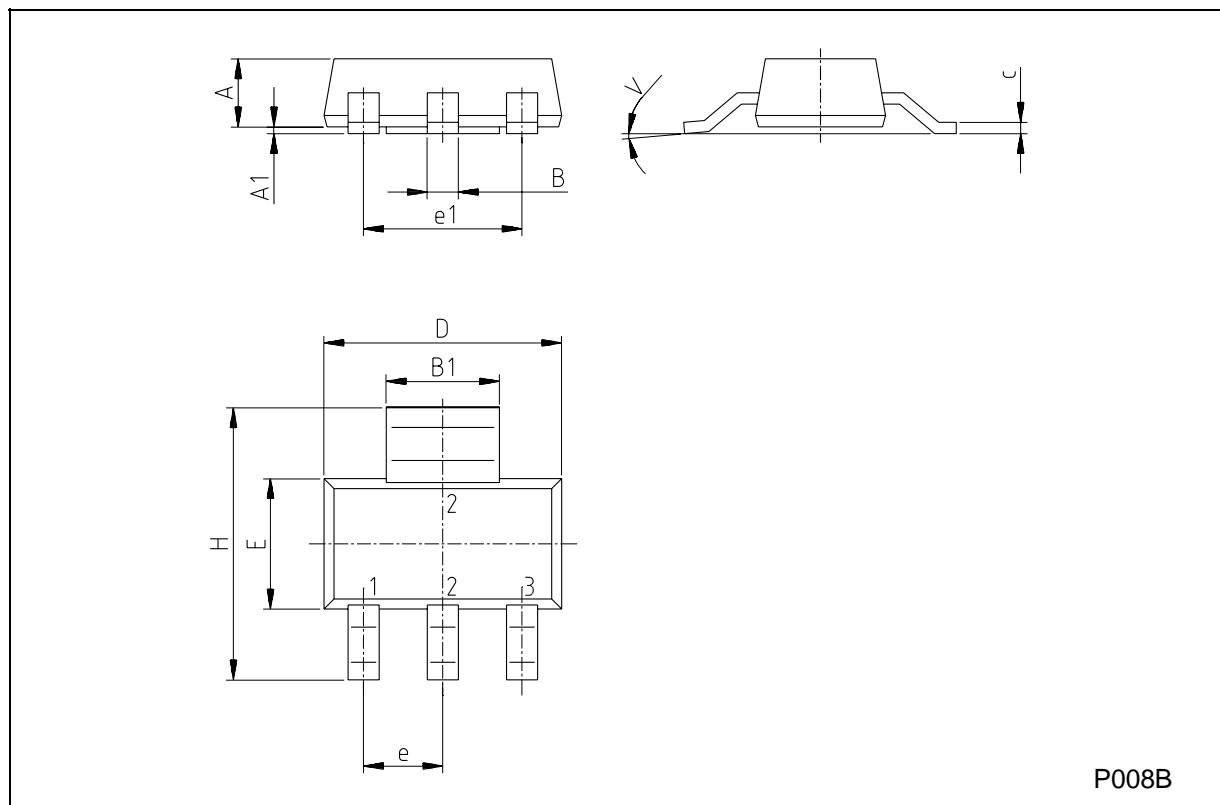


Figure 19: Test Circuit For Inductive Load Switching And Diode Recovery Times



## SOT-223 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.80			0.071
B	0.60	0.70	0.80	0.024	0.027	0.031
B1	2.90	3.00	3.10	0.114	0.118	0.122
c	0.24	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
e		2.30			0.090	
e1		4.60			0.181	
E	3.30	3.50	3.70	0.130	0.138	0.146
H	6.70	7.00	7.30	0.264	0.276	0.287
V			10°			10°
A1		0.02				



**Table 11:Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
Tuesday 18 January 2005	2.0	ADDED CURVES



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