KLI-2113

Linear CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KLI−2113 Image Sensor is a high dynamic range, multispectral, linear CCD image sensor ideally suited for demanding color scanner applications.

The imager consists of three parallel 2098-element photodiode arrays − one for each primary color. The KLI−2113 sensor offers high sensitivity, a high data rate, low noise, and negligible lag. Independent exposure control for each channel allows color balancing at the front end. CMOS-compatible 5 V clocks, and single 12 V DC supply are all that are required to drive the KLI−2113 sensor, simplifying the design of interface electronics.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	3 Channel, RGB Tri-linear CCD
Pixels Count	2098 × 3
Pixel Size	14 μm (H) × 14 μm (V)
Pixel Pitch	14 μm
Inter-Array Spacing	112 mm (8 Lines Effective)
Active Image Size	29.37 mm (H) × 0.24 mm (V) 29.4 mm (Diagonal)
Saturation Signal	170,000 e^-
Dynamic Range	76 dB
Responsivity (Wavelength) R, G, B (−RAA) R, G, B (−DAA)* Mono (−AAA, −AAB)	 62, 42, 37 V/μJ/cm^2 60, 40, 36 V/μJ/cm^2 66 V/μJ/cm^2
Output Sensitivity	11.5 μV/e^-
Dark Current	0.02 pA/Pixel
Dark Current Doubling Rate	9°C
Charge Transfer Efficiency	0.99999/Transfer
Photoresponse Non-Uniformity	5% Peak-Peak
Lag (First Field)	0.6%
Maximum Data Rate	20 MHz/Channel
Package	CERDIP (Sidebrazed, CuW)
Cover Glass	AR Coated, 2 Sides

* Configuration KLI-2113-DAA uses Gen1 color filter set and is not recommended for new designs.

NOTE: Parameters above are specified at T = 25°C and 2 MHz clock rates unless otherwise noted.

Figure 1. KLI−2113 Linear CCD Image Sensor

Features

- High Resolution
- Wide Dynamic Range
- High Sensitivity
- High Operating Speed
- High Charge Transfer Efficiency
- No Image Lag
- Electronic Exposure Control
- Pixel Summing Capability
- Up to 2.0 V Peak-Peak Output
- 5.0 V Clock Inputs
- Two-Phase Register Clocking
- On-Chip Dark Reference

Applications

- Digitization
- Machine Vision
- Mapping/Aerial
- Photography

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KLI−2113 IMAGE SENSOR

Part Number	Description	Marking Code
KLI−2113−AAA−ER−AA	Monochrome, No Microlens, CERDIP Package (Leadframe), Taped Clear Cover Glass with AR Coating (2 Sides), Standard Grade	KLI−2113 Lot Number Serial Number
KLI−2113−AAA−ER−AE	Monochrome, No Microlens, CERDIP Package (Leadframe), Taped Clear Cover Glass with AR Coating (2 Sides), Engineering Sample	
KLI−2113−AAB−ED−AA	Monochrome, No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KLI−2113 Lot Number Serial Number
KLI−2113−AAB−ED−AE	Monochrome, No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KLI−2113−RAA−ED−AA	Gen2 Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KLI−2113 Lot Number Serial Number
KLI−2113−RAA−ED−AE	Gen2 Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	
KLI−2113−DAA−ED−AA*	Gen1 Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KLI−2113 Lot Number Serial Number
KLI−2113−DAA−ED−AE*	Gen1 Color (RGB), No Microlens, CERDIP Package (Leadframe), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	

*Not recommended for new designs.

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KLI−2113−12−5−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

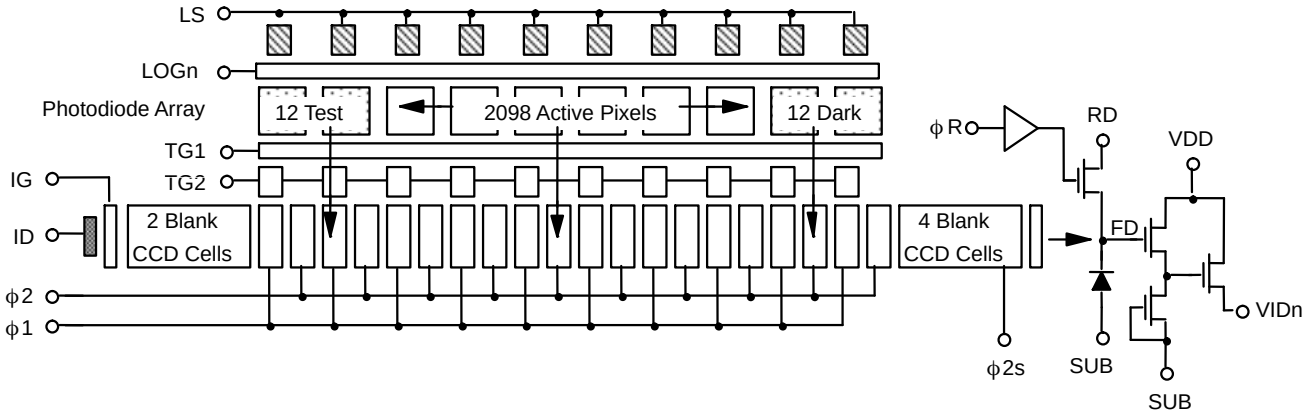


Figure 2. Single Channel Schematic

Exposure Control

Exposure control is implemented by selectively clocking the LOG gates during portions of the scanning line time. By applying a large enough positive bias to the LOG gate, the channel potential is increased to a level beyond the ‘pinning level’ of the photodiode. (The ‘pinning’ level is the maximum channel potential that the photodiode can achieve and is fixed by the doping levels of the structure.) With TG1 in an ‘off’ state and LOG strongly biased, all of the photocurrent will be drawn off to the LS drain. Referring to Figure 9, one notes that the exposure can be controlled by pulsing the LOG gate to a ‘high’ level while TG1 is turning ‘off’ and then returning the LOG gate to a ‘low’ bias level sometime during the line scan. The effective exposure (t_{EXP}) is the net time between the falling edge of the LOG gate and the falling edge of the TG1 gate (end of the line). Separate LOG connections for each channel are provided, enabling on-chip light source and image spectral color balancing. As a cautionary note, the switching transients of the LOG gates during line readout may inject an artifact at the sensor output. Rising edge artifacts can be avoided by switching LOG during the photodiode-to-CCD transfer period, preferably, during the TG1 falling edge. Depending on clocking speeds, the falling edge of the LOG should be synchronous with the ϕ1/ϕ2 shift register readout clocks. For very fast applications, the falling edge of the LOG gate may be limited by on-chip RC delays across the array. In this case, artifacts may extend across one or more pixels. Correlated double sampling (CDS) processing of the output waveform can remove the first order magnitude of such artifacts. In high dynamic range applications, it may be advisable to limit the LOG fall times to minimize the current transients in the device substrate and limit the magnitude of the artifact to an acceptable level.

Pixel Summing

The effective resolution of this sensor can be varied by enabling the pixel summing feature. A separate pin is provided for the last shift register gate labeled ϕ2s. This gate, when clocked appropriately, stores the summation of signal from adjacent pixels. This combined charge packet is then transferred onto the sense node. As an example, the sensor can be operated in 2-pixel summing mode (1,049 pixels), by supplying a ϕ2s clock which is a 75% duty cycle signal at 1/2 the frequency of the ϕ2 signal, and modifying the ϕR clock as depicted in Figure 10. Applications that require full resolution mode (2,098 pixels), must tie the ϕ2s pin to the ϕ2 pin. Refer to Figure 9 and Figure 10 for additional details.

Image Acquisition

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored in the photodiode itself and is isolated from the CCD shift registers during the integration period by the transfer gates TG1 and TG2, which are held at barrier potentials. At the end of the integration period, the CCD register clocking is stopped with the ϕ1 and ϕ2 gates being held in a ‘high’ and ‘low’ state respectively. Next, the TG gates are turned ‘on’ causing the charge to drain from the photo-diode into the TG1 storage region. As TG1 is turned back ‘off’, charge is transferred through TG2 and into the ϕ1 storage region. The TG2 gate is then turned ‘off’, isolating the shift registers from the accumulation region once again. Complementary clocking of the ϕ1 and ϕ2 phases now resumes for readout of the current line of data while the next line of data is integrated.

Charge Transport

Readout of the signal charge is accomplished by two-phase, complementary clocking of the Phase 1 and Phase 2 gates (ϕ1 and ϕ2) in the horizontal (output) shift register. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (4.75 V_{P-P} min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the ϕ2s clock. Resettable floating diffusions are used for the charge to voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta V_{FD} = \Delta Q / C_{FD}$, where ΔV_{FD} is the change in potential on the floating diffusion, ΔQ is the amount of charge, and C_{FD} is the capacitance of the floating diffusion node. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, ϕR.

Physical Description

Pin Description and Device Orientation

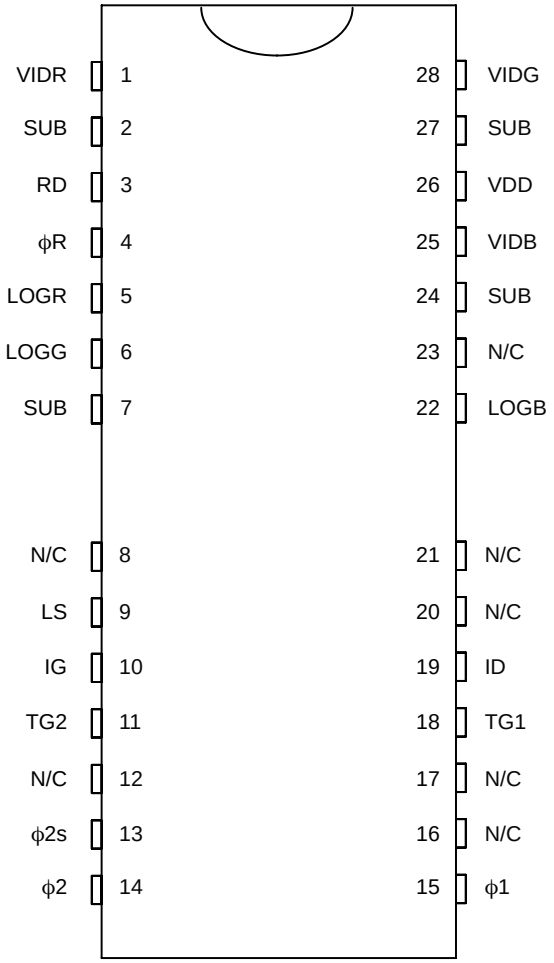


Figure 3. KLI−2113 Pinout

Table 4. PACKAGE PIN DESCRIPTION

Pin	Name	Description
1	VIDR	Red Output Video
2	SUB	Substrate
3	RD	Reset Drain
4	ϕR	Reset Clock
5	LOGR	Red Overflow Gate
6	LOGG	Green Overflow Gate
7	SUB	Substrate
8	N/C	No Connection
9	LS	Light Shield/Exposure Drain
10	IG	Input Gate/LOG Test Pin
11	TG2	Outer Transfer Gate
12	N/C	No Connection
13	ϕ2s	Phase2 Shift Register Summing Gate Clock
14	ϕ2	Phase2 Shift Register Clock

Pin	Name	Description
15	ϕ1	Phase1 Shift Register Clock
16	N/C	No Connection
17	N/C	No Connection
18	TG1	Inner Transfer Gate
19	ID	Input Diode Test Pin
20	N/C	No Connection
21	N/C	No Connection
22	LOGB	Blue Overflow Gate
23	N/C	No Connection
24	SUB	Substrate
25	VIDB	Blue Output Video
26	VDD	Amplifier Supply
27	SUB	Substrate
28	VIDG	Green Output Video

IMAGING PERFORMANCE

Typical Operational Conditions

Specifications given under nominal operating conditions @25°C ambient, f_{CLK} =2 MHz and nominal external VIDn load resistors unless otherwise specified.

Table 5. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Output Voltage	V_{SAT}	−	2.0	−	V_{P-P}	1, 7	Die[8]
Output Sensitivity	$\Delta V_O/\Delta N_e$	−	11.5	−	$\mu V/e^-$	7	Design[9]
Saturation Signal Charge	$N_{e,SAT}$	−	170k	−	e^-		Design[9]
Output Buffer Bandwidth	f_{-3dB}	−	75	−	MHz	@ C_{LOAD} = 10 pF	Design[9]
Dynamic Range	DR	−	76	−	dB	3	Design[9]
Dark Current	I_{DARK}	−	0.02	−	pA/Pixel	4	Die[8]
Charge Transfer Efficiency	CTE	−	0.99999	−	−	5	Design[9]
Lag	L	−	0.6	1	%	1st Field	Design[9]
DC Output Offset	V_{ODC}	6	7	9	V	7	Design[9]
Register Clock Capacitance	C_ϕ	−	500	−	pF	per Phase	Design[9]
Transfer Gate Capacitance	C_{TG}	−	400	−	pF		Design[9]
KLI−2113−RAA CONFIGURATION GEN2 COLOR							
Responsivity Red Channel Green Channel Blue Channel	R_{MAX}	 − − −	 62 42 37	 − − −	$V/\mu J/cm^2$		Design[9]
Peak Responsivity Wavelength Red Channel Green Channel Blue Channel	λR	 − − −	 650 540 460	 − − −	nm		Design[9]
Photoresponse Uniformity	PRNU	−	7	14	%p−p		Die[8]
KLI−2113−DAA CONFIGURATION GEN1 COLOR (Note 10)							
Responsivity Red Channel Green Channel Blue Channel	R_{MAX}	 − − −	 60 40 36	 − − −	$V/\mu J/cm^2$		Design[9]
Peak Responsivity Wavelength Red Channel Green Channel Blue Channel	λR	 − − −	 650 540 460	 − − −	nm		Design[9]
Photoresponse Uniformity	PRNU	−	5	10	%p−p		Die[8]
KLI−2113−AAA AND KLI−2113−AAB CONFIGURATION MONOCHROME							
Responsivity Monochrome, All Channels	R_{MAX}	−	66	−	$V/\mu J/cm^2$		Design[9]
Peak Responsivity Wavelength Monochrome, All Channels	λR	−	675	−	nm		Design[9]
Photoresponse Uniformity	PRNU	−	5	10	%p−p		Die[8]

1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded.
2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm.
3. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between ϕ1 and ϕ2 phases must be maintained to minimize clock noise.
4. Dark current doubles approximately every 9°C.
5. Measured per transfer. For total line h < $(0.99999)^{4256}$ = 0.96
6. Low frequency response across array with color filter array.
7. Decreasing external VIDn load resistors to improve signal bandwidth will decrease these parameters.
8. A parameter that is measured on every sensor during production testing.
9. A parameter that is quantified during the design verification activity.
10. Configuration KLI−2113−DAA uses Gen1 color filter set and is not recommended for new designs.

TYPICAL PERFORMANCE CURVES

(2 MHz Operation, Emitter Follower Buffered, 3/4 V_{SAT}, Dark to Bright Transition)

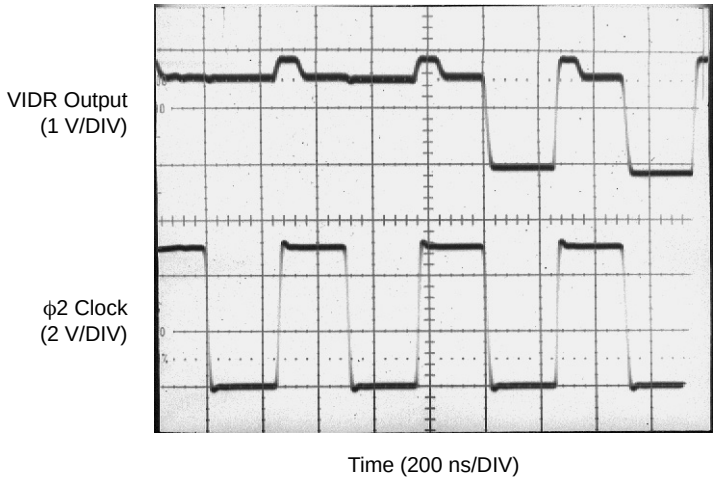


Figure 4. Output Waveforms

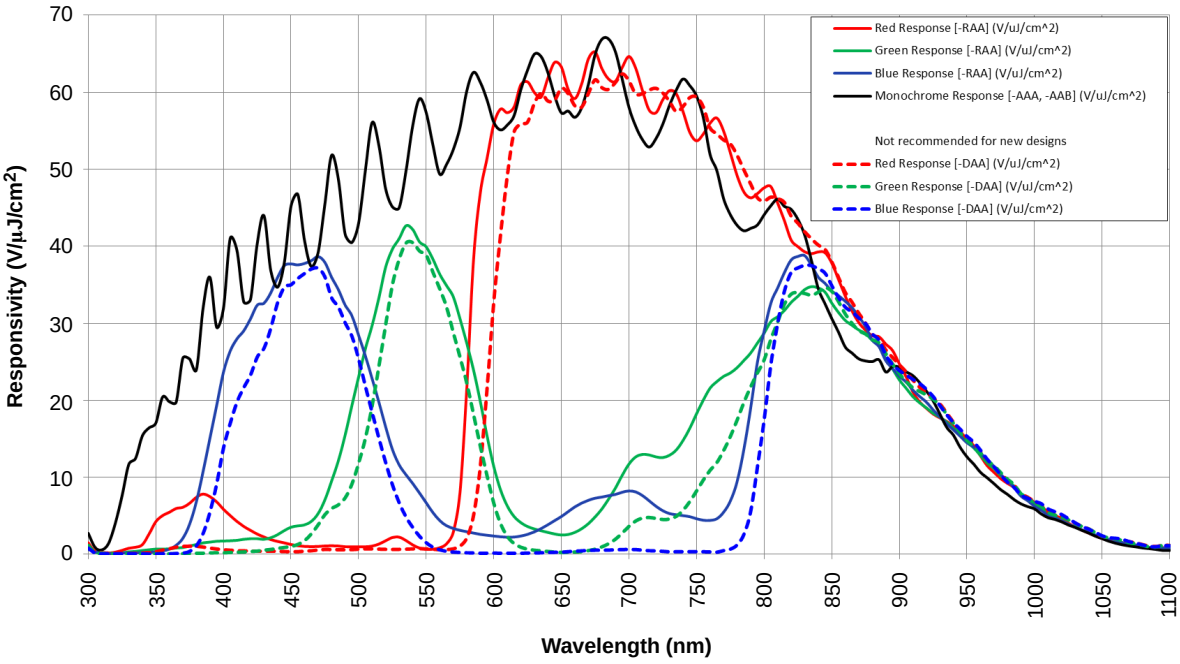


Figure 5. Typical Responsivity

DEFECT DEFINITIONS

Table 6. OPERATING CONDITION SPECIFICATIONS

(Test Conditions: T = 25°C, f_{CLK} = 2 MHz, t_{INT} = 1.066 ms)

Field	Defect Type	Threshold	Units	Notes	Number
Dark	Bright	8.0	mV	1, 2	0
Bright	Bright/Dark	10	%	1, 3	0
Bright	Exposure Control	4.0	mV	1, 4, 5	≤ 16

1. Defective pixels will be separated by at least one non-defective pixel within and across channels.
2. Pixels whose response is greater than the average response by the specified threshold. See Figure 6 below.
3. Pixels whose response is greater or less than the average response by the specified threshold. See Figure 6 below.
4. Pixels whose response deviates from the average pixel response by the specified threshold when operating in exposure control mode. See Figure 6 below.
5. Defect coordinates are available upon request.

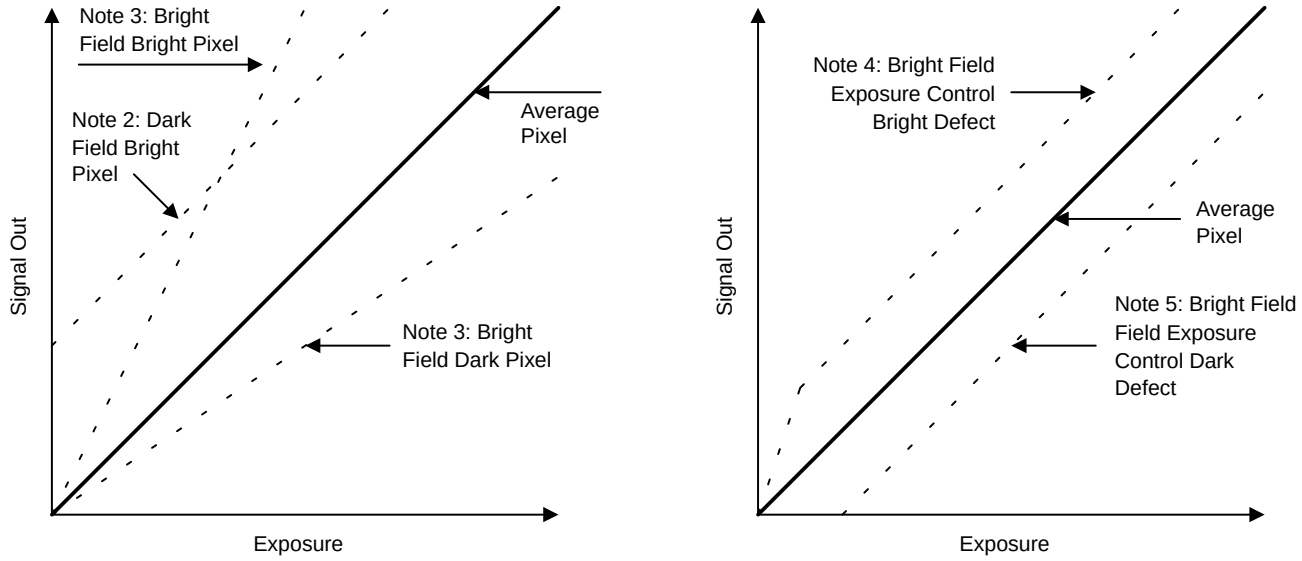


Figure 6. Illustration of Defect Classifications

OPERATION

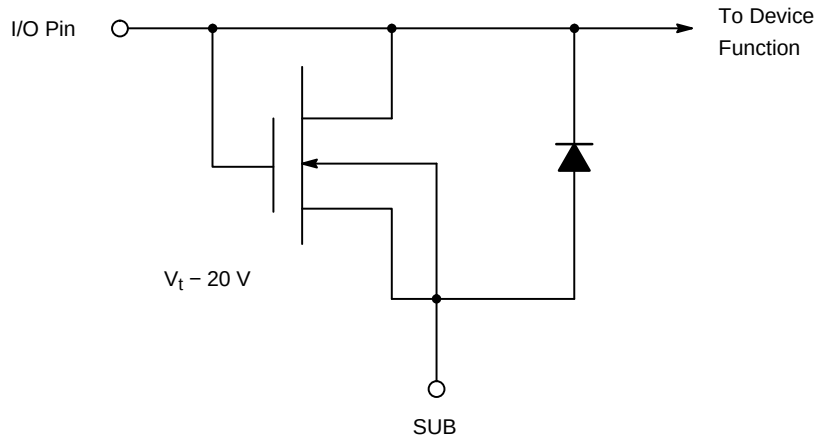
Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit	Notes
Gate Pin Voltage	V_{GATE}	−0.5	16	V	1, 2
Pin-to-Pin Voltage	$V_{PIN−PIN}$	−	16	V	1, 3
Diode Pin Voltage	V_{DIODE}	−0.5	16	V	1, 4
Output Bias Current	I_{DD}	−	−10	mA	5
Output Load Capacitance	$C_{VID,LOAD}$	−	15	pF	
CCD Clocking Frequency	f_C	−	20	MHz	6

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to substrate voltage.
2. Includes pins: ϕ1, ϕ2, ϕ2s, TG1, TG2, ϕR, IG, and LOGn.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, RD, VDD, LS and ID.
5. Care must be taken not to short output pins to ground during operation as this may cause serious damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the nominal (2 MHz) clocking frequency. VIDn load resistor values may need to be decreased as well to achieve required output bandwidths.

Device Input ESD Protection Circuit (Schematic)



CAUTION: To allow for maximum performance, this device contains limited I/O protection and may be sensitive to electrostatic induced damage. Devices should be installed in accordance with strict ESD handling procedures!

Figure 7. ESD Protection Circuit

DC Bias Operating Conditions

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
Substrate	V_{SUB}	−	0	−	V	
Reset Drain Bias	V_{RD}	11.5	12.0	12.5	V	
Output Buffer Supply	V_{DD}	11.5	12.0	12.5	V	
Light Shield/Drain Bias	V_{LS}	11.5	12.0	12.5	V	
Output Bias Current/Channel	I_{DDn}	−4.0	−6.0	−8.0	mA	1
Test Pin − Input Gate/LOG	V_{IG}	−	12.0	−	V	
Test Pin − Input Diode	V_{ID}	−	12.0	−	V	

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. See Figure 8.Choose values optimized for specific operating frequency, but R2 should not be less than 75 Ω.

Typical Output Bias/Buffer Circuit

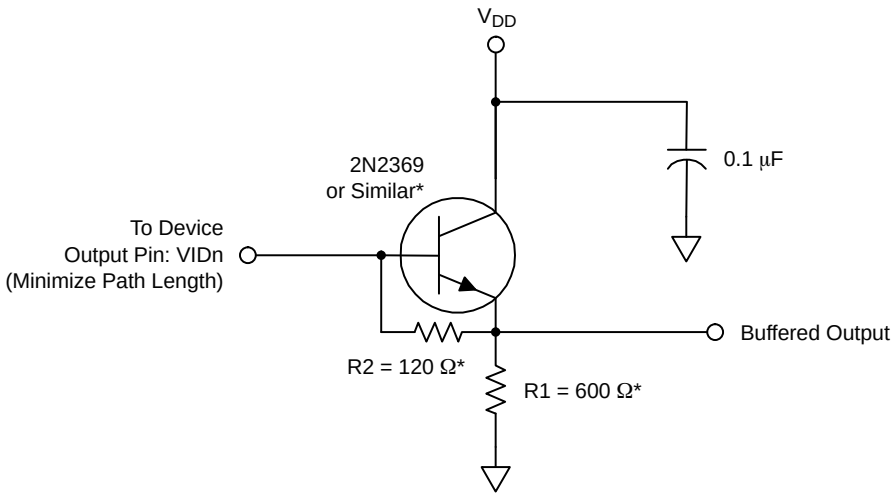


Figure 8. Typical Output Bias/Buffer Circuit

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Readout Clocks High	$V_{\phi 1H}$, $V_{\phi 2H}$, $V_{\phi 2sH}$	4.75	5.0	5.25	V	
CCD Readout Clocks Low	$V_{\phi 1L}$, $V_{\phi 2L}$, $V_{\phi 2sL}$	−0.1	0.0	0.1	V	
Transfer Clocks High	V_{TG1H}, V_{TG2H}	4.75	5.0	5.25	V	
Transfer Clocks Low	V_{TG1L}, V_{TG2L}	−0.1	0.0	0.1	V	
Reset Clock High	$V_{\phi RH}$	4.75	5.0	5.25	V	
Reset Clock Low	$V_{\phi RL}$	−0.1	0.0	0.1	V	
Exposure Clocks High	V_{LOG1H}, V_{LOG2H}	4.75	5.0	5.25	V	1
Exposure Clocks Low	V_{LOG1L}, V_{LOG2L}	−0.1	0.0	0.1	V	1

1. Tie pin to 0 V for applications where exposure control is not used.

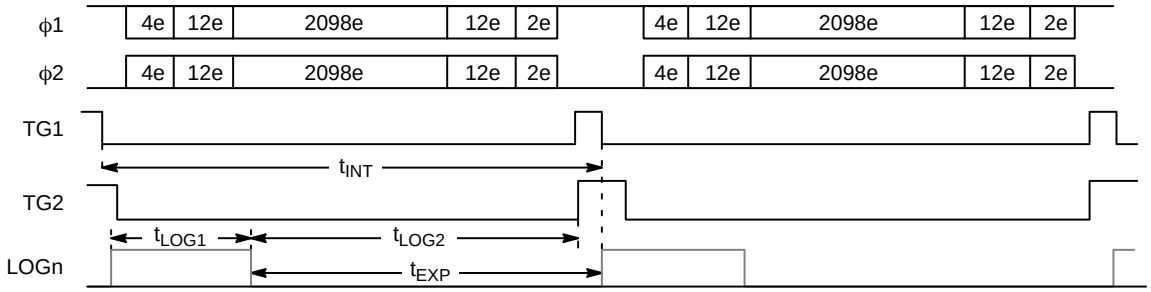
Table 10. AC TIMING LEVELS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
CCD Element Duration	$1e^-$ (= $1/f_{CLK}$)	50	50	−	ns	
Line/Integration Period	1L (= t_{INT})	0.108	1.066	−	ms	
PD−CCD Transfer Period	t_{PD}	1.0	−	−	μs	
Transfer Gate 1 Clear	t_{TG1}	500	−	−	ns	
Transfer Gate 2 Clear	t_{TG2}	500	−	−	ns	
LOGGate Duration	t_{LOG1}	1	−	−	μs	
LOGGate Clear	t_{LOG2}	1	−	−	μs	
Reset Pulse Duration	t_{RST}	9	−	−	ns	
Clamp to ϕ2 Delay	t_{CD}	5	−	−	ns	1
Sample to Reset Edge Delay	t_{SD}	5	−	−	ns	1
CCD Clock Rise Time	t_R	−	30	−	ns	Typical

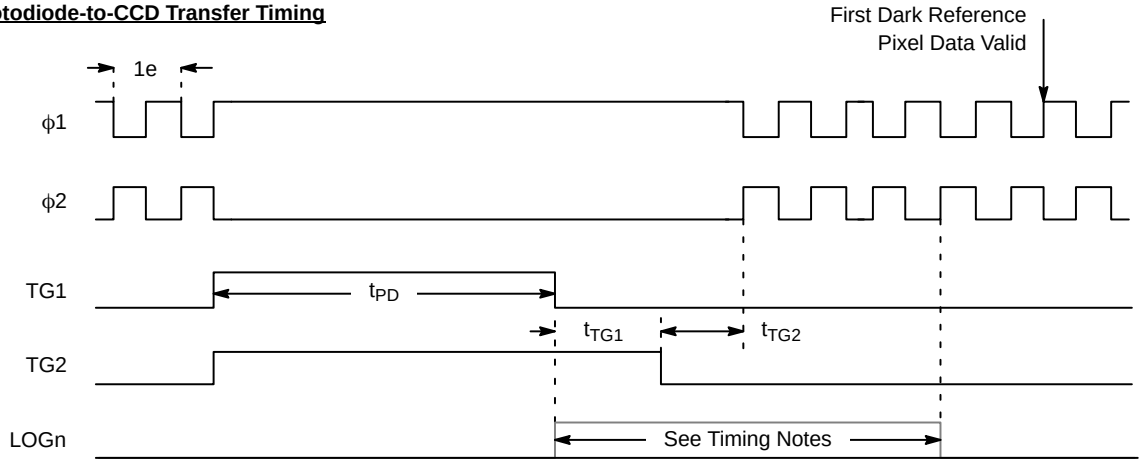
1. Recommended delays for Correlated Double Sampling of output.

TIMING

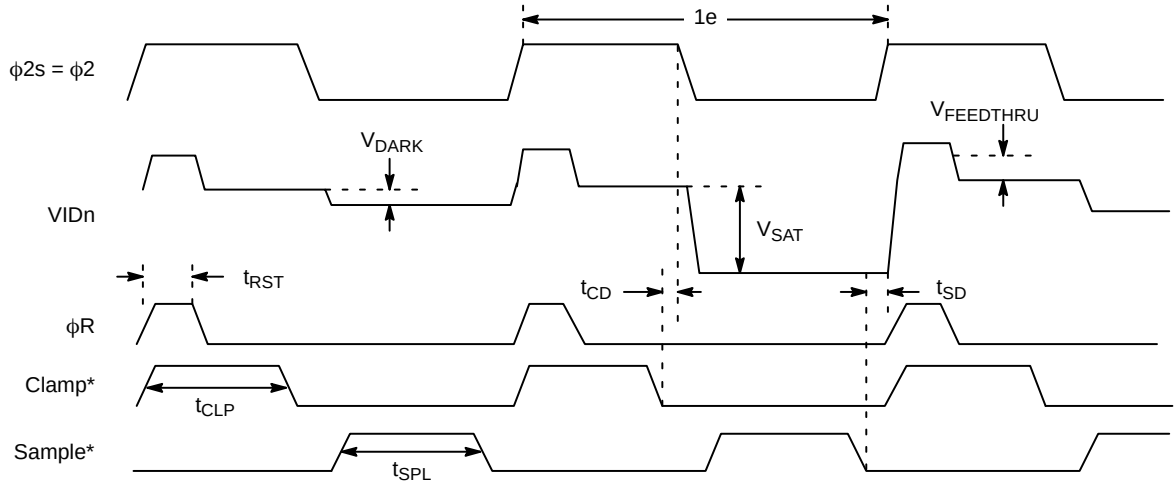
Line Timing



Photodiode-to-CCD Transfer Timing



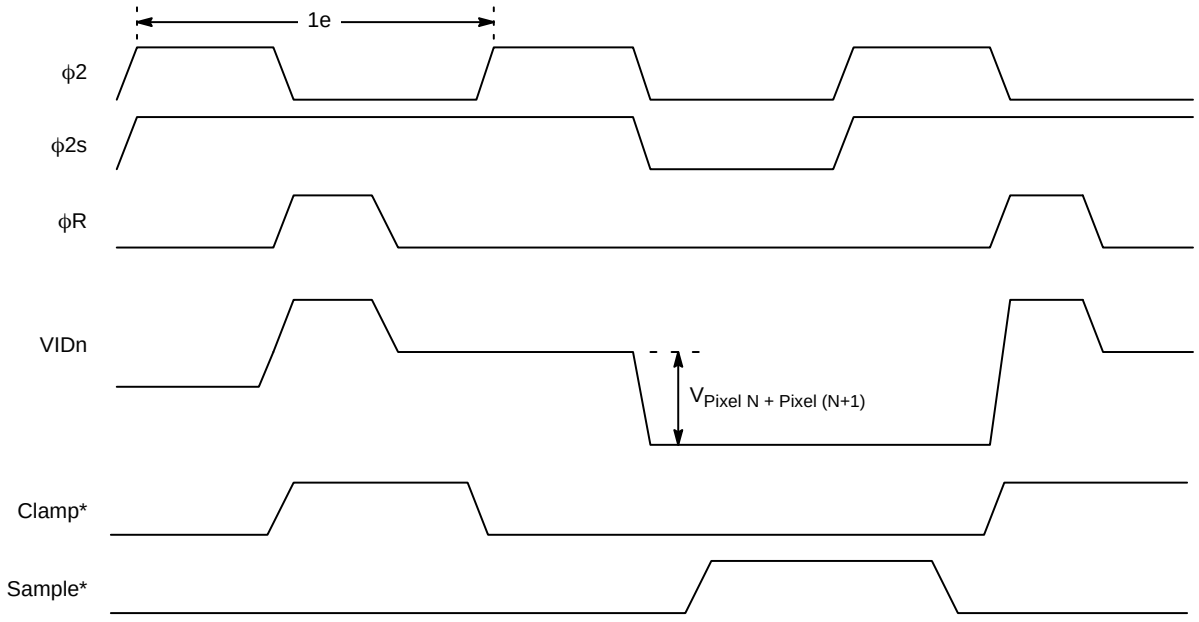
Output Timing (Full Resolution Mode)



* Required for Correlated Double Sampling.

Figure 9. Normal Mode Timing

Output Timing (2-Pixel Summing Mode)



* Required for Correlated Double Sampling.

Figure 10. Binning Mode Timing

MECHANICAL INFORMATION

Completed Assembly

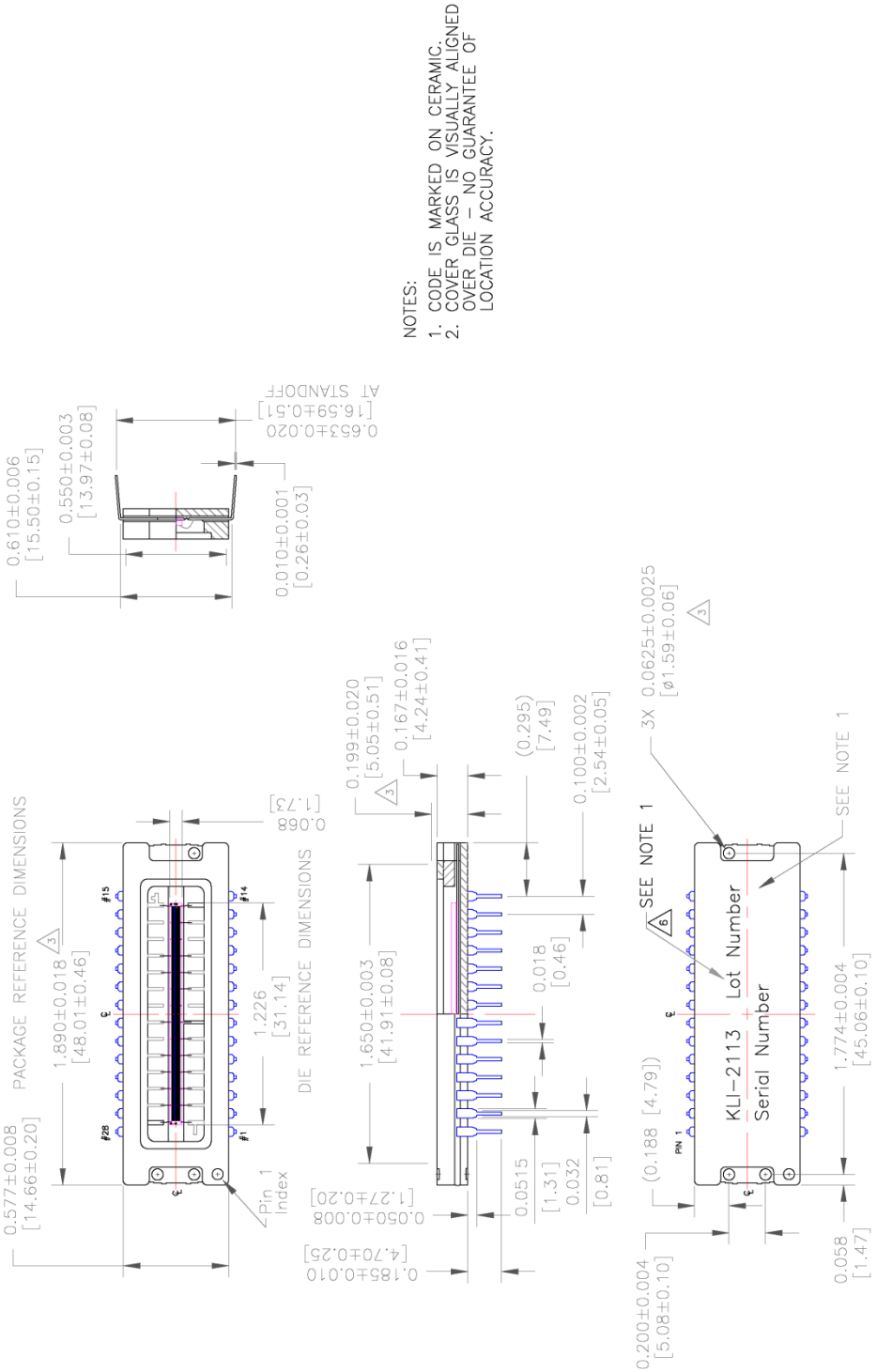


Figure 11. Completed Assembly Drawing (1 of 4)

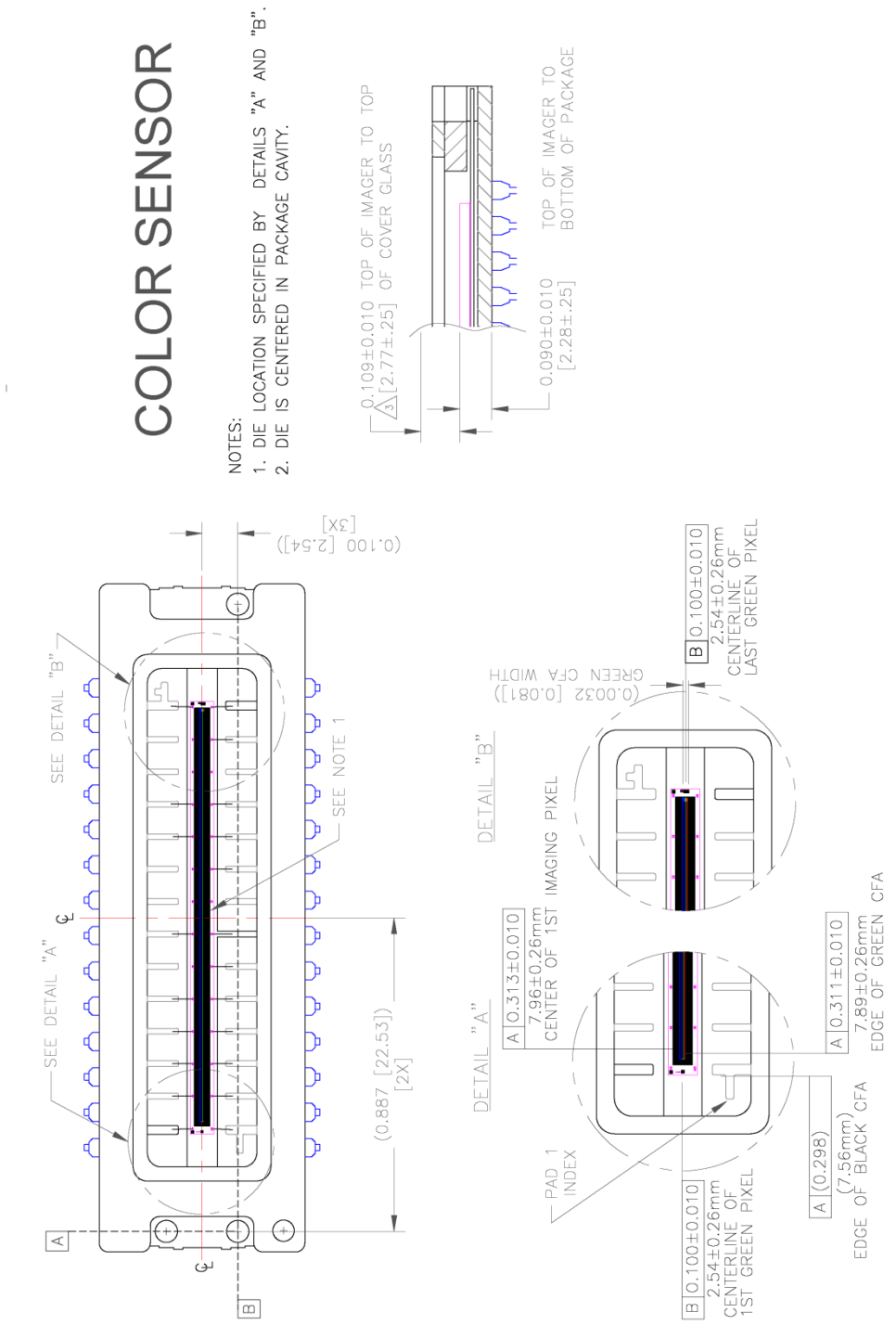


Figure 12. Completed Assembly Drawing (2 of 4)

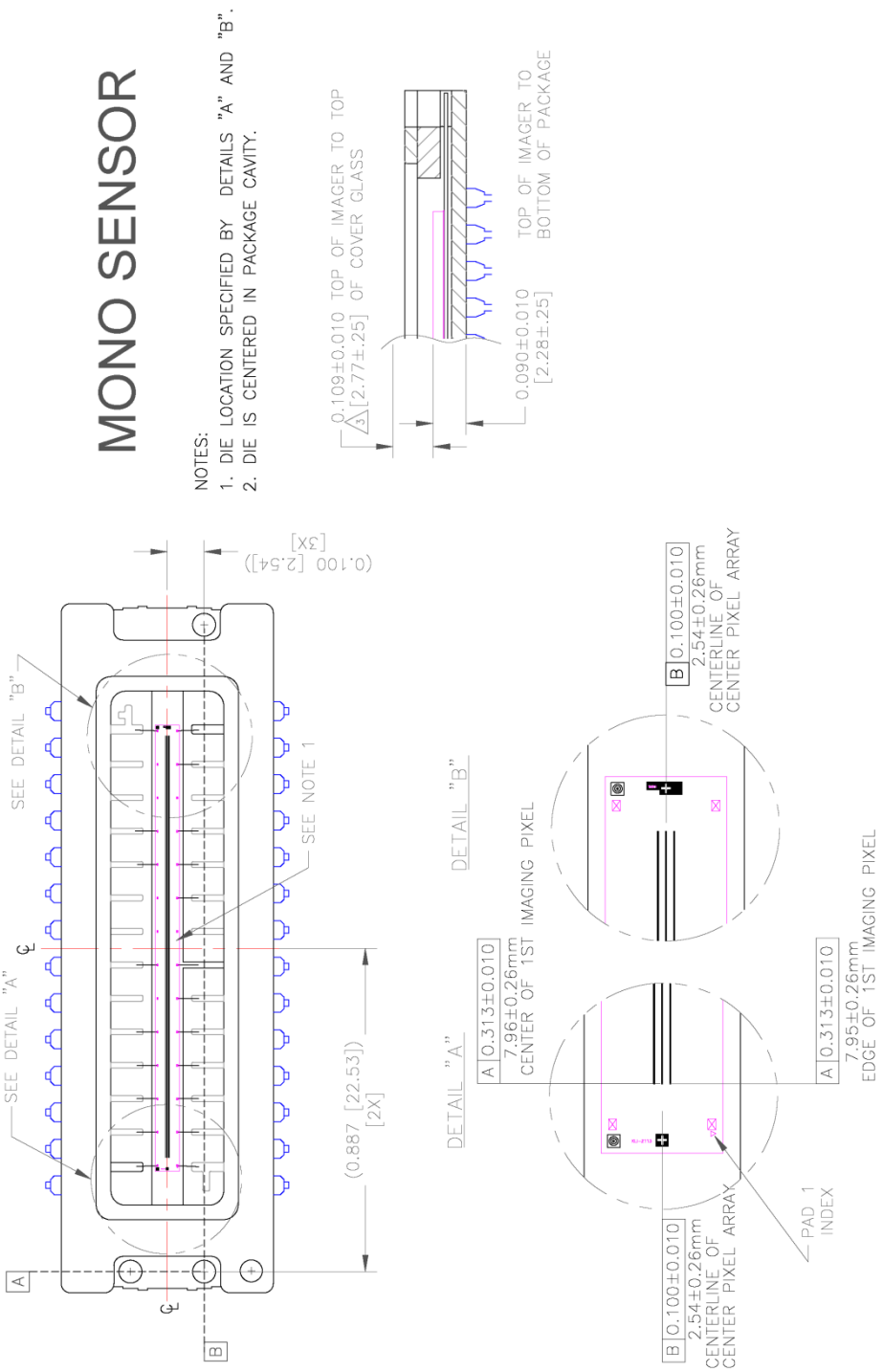


Figure 13. Completed Assembly Drawing (3 of 4)

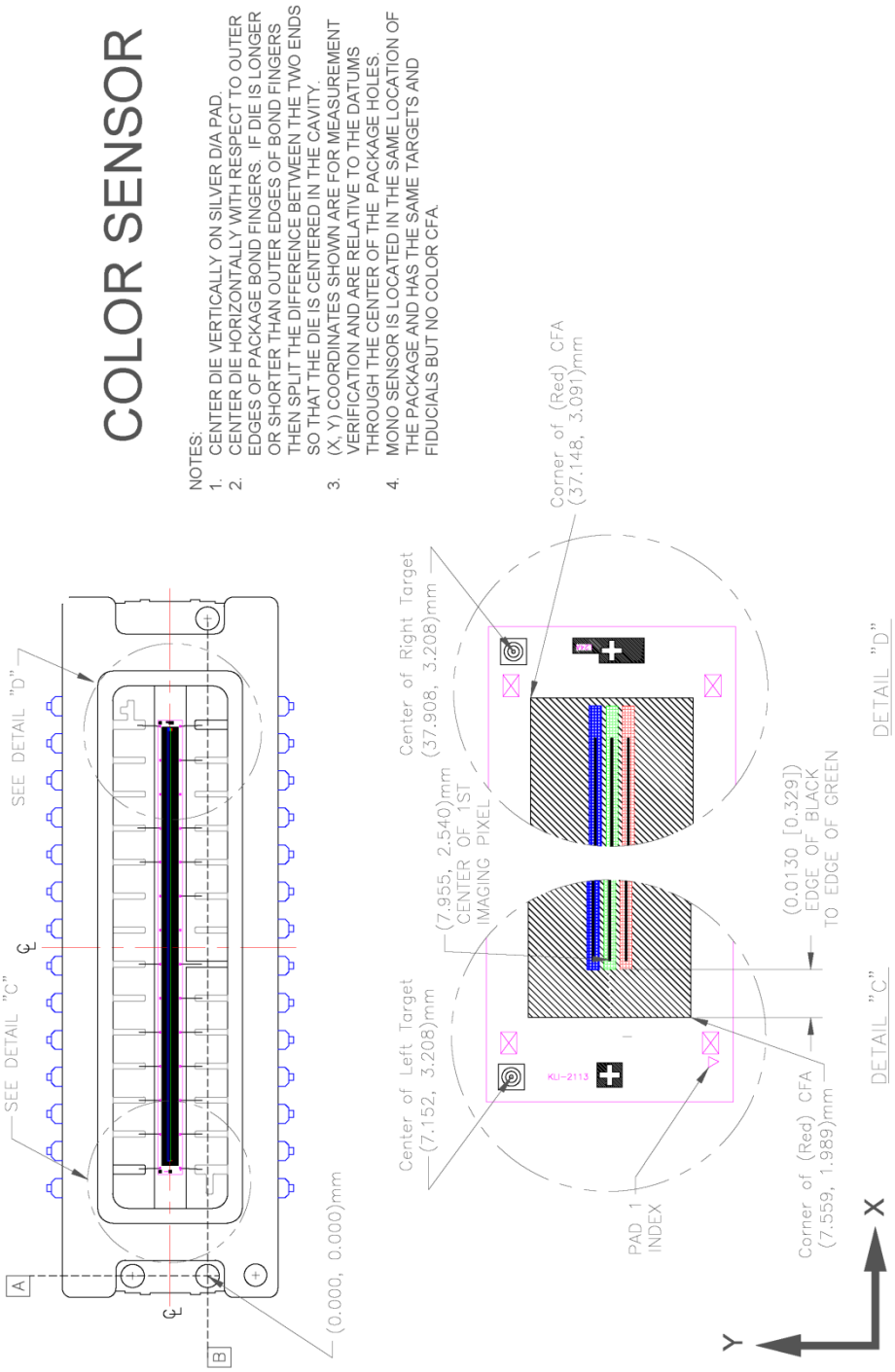


Figure 14. Completed Assembly Drawing (4 of 4)

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

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